UNDERSTANDING THE IMPACT OF BULK TRAPS ON GAN HEMT DC AND RF CHARACTERISTICS

By

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Dedicated to my parents, family, friends and Bhagwan Sri Sathya Sai Baba

ELECTRICAL ENGINEERING

ABSTRACT 1

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Dissertation under the direction of Professor Robert A. Reed

The demand for high power high frequency semiconductor devices has led to the development of microwave power devices using GaN and SiC. AlGaN/GaN HEMTs have shown power densities of 9.8 W/mm at 8 GHz. Although these results are very encouraging, significant work needs to be done to improve performance. It is generally recognized that trapping effects limit the performance of these devices. In this dissertation we study the impact of bulk traps on three distinct characteristics of these devices. These 3 mechanisms are: degradation in the IV characteristics, self-heating and gate-lag.

Displacement-damage induced degradation in AlGaN/AlN/GaN HEMTs with polarization charge induced 2DEGs is examined using simulations and experiments. Carrier removal in the unintentionally doped AlGaN layer changes the space charge in the structure and this changes the band bending. The band bending decreases the 2DEG density, which in turn reduces the drain current in the device. The effect of the defect energy levels on the 2DEG density is also studied. The interplay between band bending, mobility degradation, and the charged defects is analyzed and quantified.

Experiments and TCAD simulations are used to study the relationship between bulk traps, self-heating and mobility degradation in AlGaN/AlN/GaN HEMTs. Bulk traps in the GaN channel region and other regions of the device degrade the 2DEG density and the mobility in the device. This in turn degrades the performance of the device. Mobility degradation is closely coupled with the self-heating in the device. The interplay between bulk traps, mobility degradation and self-heating is analyzed and quantified.

Experiments and simulations showing the impact of proton irradiation induced bulk traps on gate lag in AlGaN/AlN/GaN HEMTs are analyzed. Pre-existing donor-like surface traps in the gate-drain and source-gate access regions cause the majority of the gate-lag in the device. The simulations indicate that these traps at the AlGaN/Nitride surface are very close to the valence band. Gate lag increases with increased bulk traps. This is due to the reduction in the 2DEG density as a result of band bending and mobility degradation. The experiments and simulations did not indicate any substantial hot electron induced current collapse due to bulk traps.

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CHAPTER 1

INTRODUCTION

1.1 Overview of the work

The HEMT (high electron mobility transistor), also known as a MODFET (modulation doped field effect transistor), exploits the differences in band gap between dissimilar semiconductor materials such as GaN and AlGaN or GaAs and AlGaAs. These devices provide higher frequency operation than MESFETs (metal semiconductor field effect transistor), while maintaining the low noise performance and high power rating. At present, frequencies of 100 GHz have been achieved in the GaN and GaAs material systems [1]. The high frequency behavior is due to a separation of the mobile electrons from the donor atoms at the interface between the AlGaAs and GaAs and AlGaN and GaN layers, respectively. The electrons are trapped in a quantum well in which motion is possible only parallel to the interface.

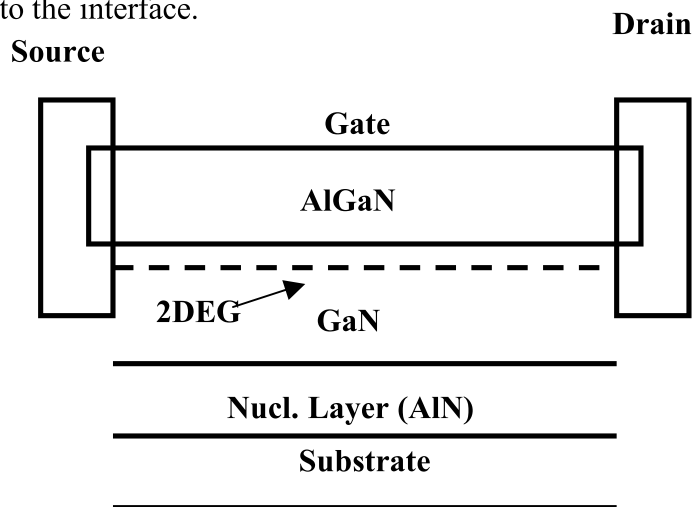


Fig. 1. Basic GaN HEMT structure.

Here we speak of a two-dimensional electron gas (2DEG) or plasma of very high mobility. In GaAs HEMTs, mobility is ~9000 $cm^2/(V.s)$, and in GaN devices, mobility is about 1200 $cm^2/(V.s)$. This is a major improvement over MESFETs fabricated in the same material systems where the mobility is approximately half the above-mentioned values. The carrier density is typically specified in terms of a surface density; the values are between 10^{12}-10^{13} cm^{-2}. This allows HEMTs to satisfy the high current and the high frequency requirements for power devices.

GaN HEMTs promise high power, high frequency operation and are poised to replace vacuum tubes in the RF power device application area. Studies on GaN HEMTs suggest that the performance and reliability of these devices can be limited significantly by trapping effects [2]. Charged traps degrade the power performance by bending the bands and diminishing mobility in the 2DEG region in these devices [3]. They also degrade the power performance. Initial investigations on trapping effects in these devices suggest that failure mechanisms like current collapse are mainly due to the presence of surface traps. Current collapse is defined as a recoverable reduction in the drain current [4]. Current collapse is typically observed after a large drain bias is applied to the device. When the DC *I-V* characteristics are measured again (starting from a drain bias of 0 V), the drain current is seen to be much smaller than what is typically observed. There has also been other studies that suggest that the main mechanism responsible for current collapse in these devices is the presence of bulk traps in the buffer GaN layer where the 2DEG is formed [5]. This thesis assesses and quantifies the impact of bulk traps in these HEMTs. The impact of bulk traps on DC *I-V* characteristics is presented. This study also looks in detail at the relationship between deep traps in the bulk and gate-lag (described

in Chapter 7). Self-heating is another important phenomenon in these devices. This thesis discusses the physics of self-heating and how its effects can be separated from those due to traps (described in chapter 6).

1.2 Brief history of GaN HEMTs

GaN based HEMTs are relatively immature when compared to GaAs HEMTs and GaN optical technologies. Khan *et al.* [6] reported the first AlGaN/GaN hetero-junction with an areal carrier density of 10^{11} cm^{-2} and a mobility of 400-800 cm^2/Vs. They were also the first group to report the DC and RF behavior of GaN HEMTs in 1993 and 1994, respectively [7, 8]. The devices were 0.25 μm gate length devices with a saturation current of 40 mA/mm. In 1996 Wu *et al.* [9] reported a power density of 1.1 W/mm at 2 GHz. Over the past few years the performance of GaN HEMTs has been helped due to two major improvements. The first one was the SiN passivation layer, which has proven to be extremely effective in reducing DC to RF dispersion [10]. The second improvement is the large increase in breakdown voltage due to the inclusion of field plates [11, 12]. The field plate also helps in reducing DC to RF dispersion. Output power densities in excess of 12 W/mm are common nowadays. GaN devices have traditionally exhibited better linearity compared to other power devices. When compared to GaAs HEMTs, GaN HEMTs have demonstrated a power density of 2.4 W/mm with a PAE (power added efficiency) of 53%, which was much better than GaAs based HEMTs [13]. In summary, the last decade and a half has seen much work on GaN HEMTs and the performance has improved significantly.

1.3 Material parameters of GaN and other technologies

The last two decades have seen much interest in III-V power device technology. GaAs HEMTs are now ubiquitous and find applications in most mobile-phone technologies [1]. On the other hand, for use in high power applications, GaN HEMTs have shown a great deal of promise. In general, GaAs- and GaN-based devices are very attractive for many power electronic applications, ranging from power conditioning to RADAR to microwave transmitters. The mobile systems, RF and microwave amplifier application spaces are expanding quite rapidly; consequently power amplifiers are getting more and more attention. A variety of power amplifier technologies are vying for the RF application space. These include Si-LDMOS (Lateral-diffused MOS), Bipolar SiGe transistors and finally GaAs and GaN HEMTs. The material properties of GaN are compared with other materials in Table 1.

	Si	GaAs	4H-SiC	GaN	Diamond
E_g (eV)	1.1	1.42	3.26	3.39	5.45
n_i (cm^{-3})	1.5×10^{10}	1.5×10^{6}	8.2×10^{-9}	1.9×10^{-10}	1.6×10^{-27}
ε_r	11.8	13.1	10	9.0	5.5
μ_n	1350	8500	700	1500(2DEG)	1900
ν_{sat}(10^7cm/s)	1	2	2	2.5	7
E_{br} (MV/cm)	0.3	0.4	3.0	3.3	5.6
Θ (W/cm)	1.5	0.43	4.9	1.3	20
JM	1	2.7	20	27.5	50

Table 1. Material properties related to power and frequency parameters of 5 different materials.

Johnson's figure of merit (JM) is defined as [14]:

$$JM = \frac{E_{br}\nu_{sat}}{2\pi} \tag{1}$$

Johnson's figure of merit gives the power-frequency limits of the material. The quantity is solely based on material parameters. A JM of 3 and below implies a material that is suitable for low power operation. Comparing Johnson's figures of merit from the table, it is evident that Si is able to satisfy the low power and low frequency applications. Also, of late the incorporation of SiGe into Si technology has vastly improved Si technology [15]. The low breakdown voltage and the low saturation velocity limit the high power and high frequency application of silicon. GaAs has a large saturation velocity and high mobility, but does not have a large breakdown field (0.4 MV/cm). This limits its use in high power applications, and is due to the small band gap as compared to GaN and SiC. The power densities are limited to 1-2 MW/mm. The power density is expressed as a linear density to allow easy comparison of device performance across different designs. High power and high frequency applications need both high breakdown voltages and high saturation velocity.

From a high frequency, high power application perspective, materials with higher JM are preferable. The wide band gap results in a higher breakdown voltage. HEMTs have better electron mobility than GaN MESFETs mainly due to the isolation of dopant atoms from the 2DEG, attributed to the reduction in impurity scattering [16]. High carrier concentration and high mobility implies a low on-resistance (R_{ON}). This is extremely useful when it comes to power switching applications. The major use of HEMTs is in power amplifiers, and from that perspective GaN has many advantages over GaAs. However, GaAs has proved to be the material of choice for the low power application space. GaN-based HEMTs provide higher output power densities; this allows the device sizes to be much smaller than GaAs for the same output power requirement. Impedance

matching is much easier due to the smaller size of GaN HEMTs. The wide band gap ensures operation at high voltages, and this is a major step forward in improving amplifier efficiency. The high carrier concentration, high mobility, and large breakdown voltage make GaN HEMTs a very promising technology for power amplifier design.

1.4 Summary of key results

Previous studies have studied the degradation of HEMT DC characteristics with bulk traps [17-20]. These studies use analytical models to model the interplay between bulk traps and HEMT characteristics. Analytical models make many approximations and lump several device parameters together [21, 22]. This dissertation studies the relationships between bulk traps, surface traps and DC and RF HEMT characteristics using TCAD (Technology computer aided design) simulations. TCAD simulations model semiconductor devices using basic equations like the Poisson and continuity equations. TCAD simulations allow analysis of parameters like the band structure and mobility. This is not easily done using analytical models. This section summarizes in brief some of the key results from the dissertation. The characteristics studied are band bending and DC to RF dispersion. The effects of self-heating are separated from those due to traps.

1.4.1 Band bending

Experimental data and simulations on GaN HEMTs are used to demonstrate the electrostatic effects of deep acceptor-like defects. Charged defects in the GaN HEMT degrade the *I-V* characteristics by bending the bands and degrading mobility. Irradiating the devices with protons creates these charged defects. Protons cause displacement

damage, which causes the formation of the charged defects. TCAD simulations allow us to understand the interplay between charged defects, band bending and mobility degradation in the device. Figure 2 compares experiment and simulation results. These results suggest that band bending and mobility degradation both play important roles in degrading the *I-V* characteristics when traps are introduced via a proton exposure. The Pre-irradiation experiment and simulation curves do not match at higher drain voltages. This is because self-heating is not modeled in these simulations.

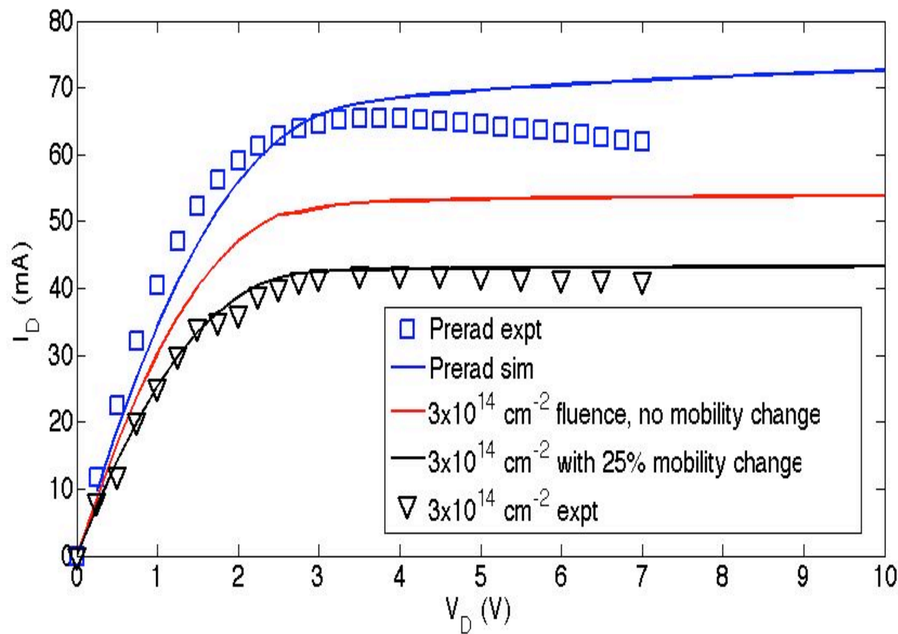


Fig. 2. I_D-V_D comparison between experiment and simulation.

1.4.2 Self-heating

Self-heating effects are a serious concern in GaN HEMTs because of their large power densities. Self-heating can be summarized as follows. The application of high voltage and high current results in greater heat generation in the channel of the device, which in turn results in a rise of lattice temperature, and thus a degradation of device

performance. The power densities in GaN HEMTs are 10 times higher than those that can be obtained in silicon and GaAs devices. This is a result of the large current densities possible in GaN HEMTs [23]. The elevated temperatures near the 2DEG reduce the drain current in the device compared to what can be obtained if the lattice temperature is maintained at room temperature. The reduction in drain current is due to degradation in mobility [23]. Figure 3 is a comparison between experiments and simulations. In this dissertation we quantify this interplay between bulk defects, self-heating and mobility degradation in AlGaN/AlN/GaN HEMTs using experiments and simulations. This work also quantifies the interplay between mobility degradation, self-heating and the degradation in the *I-V* characteristics. This will allow us to better distinguish between trap induced and self-heating induced degradation in the *I-V* characteristics.

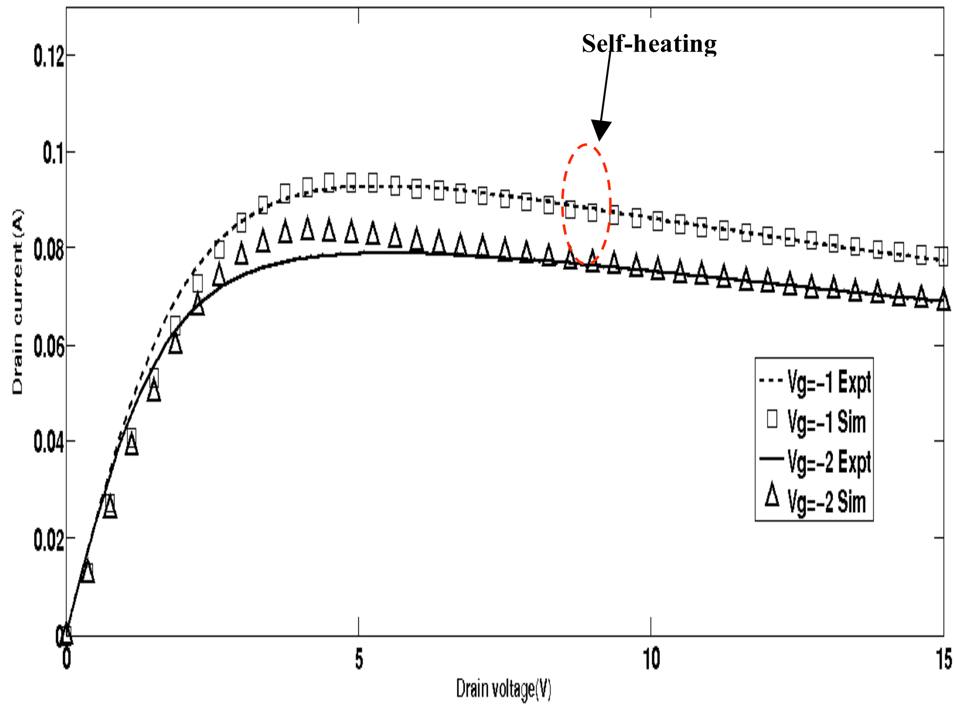


Fig. 3. I_D-V_D characteristics at two different gate voltages

1.4.3 DC to RF dispersion

The power performance of GaN HEMTs has always been one of the most attractive features. The first demonstration of microwave operation was in 1996 by Wu *et al.* [9]. The use of SiN passivation has further helped this cause by improving performance. This has helped to improve output power densities to values closer to 10-12 W/mm. However, theory predicts limits that are much larger, and at present there is a large gap between the theoretical and actual device characteristics. According to the well known linear and saturated output power equations [24],

$$P_{\max,lin} = \frac{1}{8} I_{\max} \bullet (V_{BD} - V_{Knee}) \quad (2)$$

$$P_{sat} = \frac{16}{\pi^2} P_{\max,lin}, \quad (3)$$

A typical AlGaN/GaN HEMT with maximum current I_{max} of 1.2 A/mm, knee voltage V_{Knee} of 5V and breakdown voltage V_{BD} of 100 V should produce maximum linear power of 14 W/mm, while the saturation power should reach 22 W/mm.

The difference between the DC and RF measured output power is known as DC to RF dispersion. Figure 4 demonstrates a typical dispersion characteristic. Both DC and pulsed *I-V* characteristics are displayed. When a pulsed measurement is made, the current observed is much lower than the DC characteristic. Research suggests that dispersion is related to traps. Although traps can be located in the buffer layer [24, 25], the barrier layer [26] or at the surface [27], SiN passivation has been shown to improve power performance, which suggests that surface traps cause much of the dispersion. A virtual gate model explains the effect of dispersion due to traps at the surface [28].

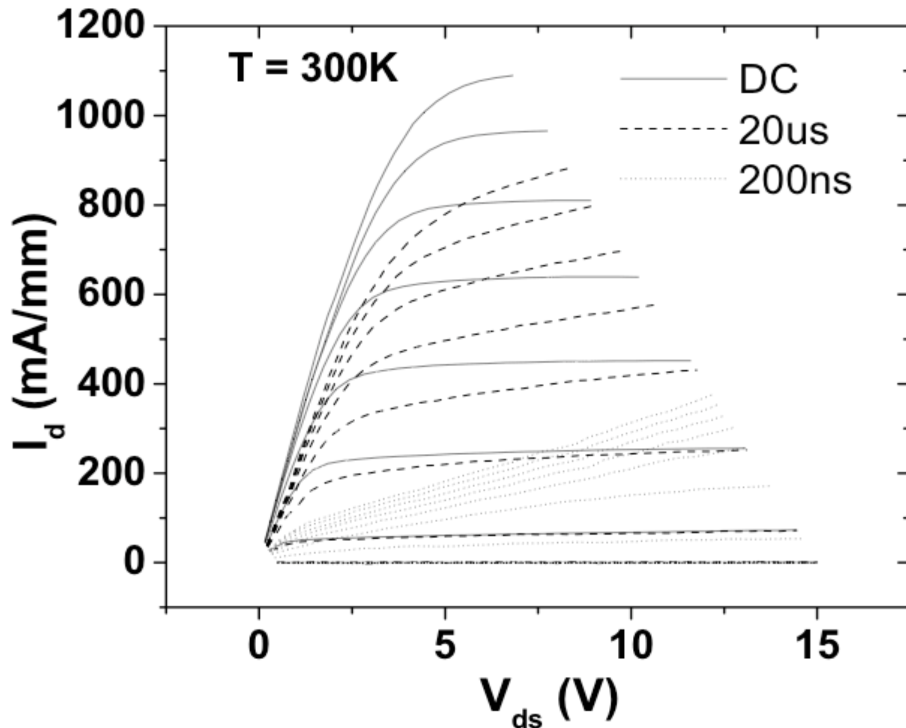


Fig. 4. Typical DC to RF dispersion characteristics [65].

Figure 5 illustrates how surface states cause dispersion. In region 1, a negative voltage below pinch off is applied to the gate. The channel under the gate is depleted and the device is off. Due to the high electric field at the drain edge of the gate, there is a small amount of gate leakage between the gate and drain. This current charges up the surface states, forcing the surface potential to become negative. As a result, the channel under the part of the drain access region next to the gate is depleted too. In region 2, the gate bias is positive. The channel under the gate is able to respond quickly. The region under the access region is slow to react. The deep level traps and the low mobility of the electrons under this region are responsible for the slow turn-on of the region. Thus, after the bias changes the access region is still depleted and has a very low carrier concentration. This produces a highly resistive region and most of the drain bias drops across that region. This drop causes the drain current to remain low after changing the

bias. The electrons are eventually released from the traps and move back to contribute to the current. The current increases correspondingly. If the pulse is long enough the drain current reaches a steady state.

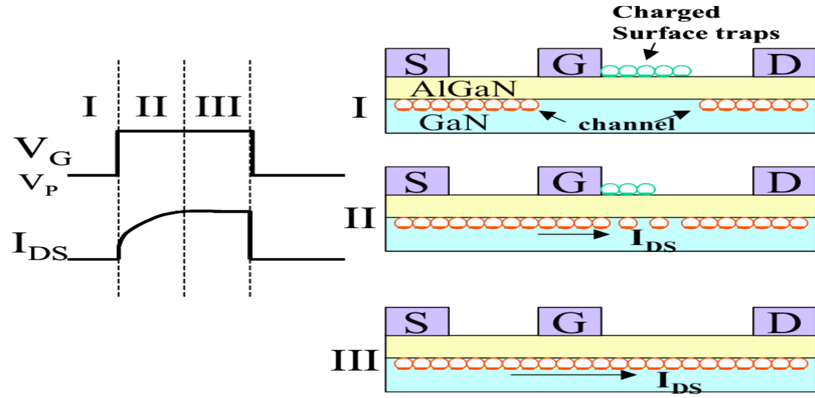


Fig. 5. Mechanism behind surface states causing dispersion in a GaN HEMT.

Buffer-layer traps also may cause DC to RF dispersion [5]. This results from the capture of hot electrons from the channel in the buffer traps. This depletes the 2DEG and causes a reduction in the drain current. Figure 6 illustrates the time evolution of the hot electrons being captured by buffer traps. The magnitude of the collapse depends on a variety of conditions like trap density and trap distribution, trap energy, and the presence or absence of a passivation layer on the surface.

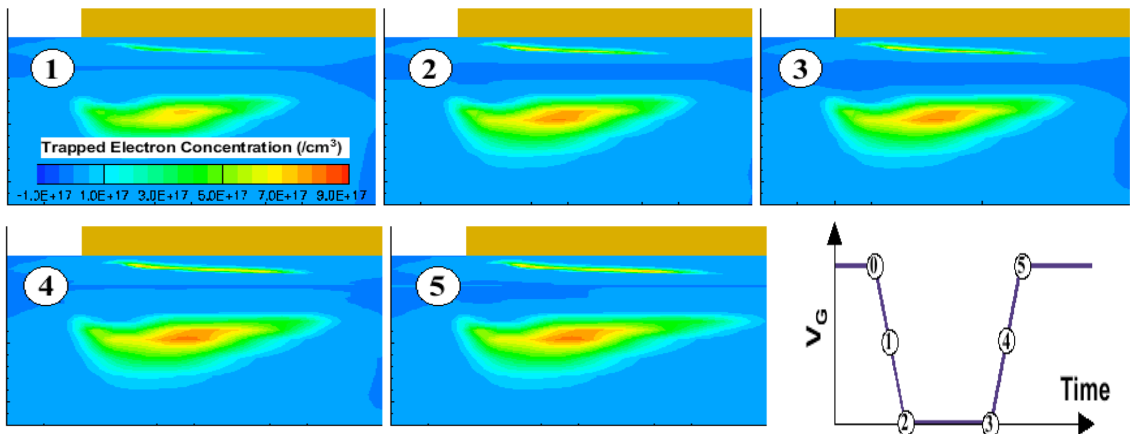


Fig. 6. Mechanism behind bulk states causing dispersion in a GaN HEMT.

This work discusses the relationship between surface traps, bulk traps and gate-lag in these devices. The devices were irradiated with protons and simulations and experiments were used to quantify the impact of bulk traps on gate-lag.

1.5 Approach

The approach used in the dissertation is summarized in this section. The pre-irradiation devices were characterized and TCAD models were calibrated with respect to these data. Devices were irradiated with 1.8 MeV protons and the post-irradiation characteristics were measured. The 1.8 MeV protons allow us to introduce defects in a controlled manner. These post-irradiation experimental results are interpreted using simulations. Calibrated TCAD simulations are used to understand the effects of bulk defects and surface defects on HEMT characteristics.

CHAPTER 2

BASIC GAN HEMT DEVICE PHYSICS

2.1 Introduction

This chapter summarizes the device details and the physics needed to understand the results in this dissertation. The device structure, basic *I-V* characteristics and analytical models are discussed. Also discussed are sources of traps and the impact that these traps have on GaN HEMT operation.

2.2 Device structure

The structure of the HEMTs examined in this work is shown schematically in Fig. 7 (not to scale). The AlGaN/AlN/GaN heterostructures were fabricated by metallorganic chemical vapor deposition (MOCVD) on a sapphire substrate. The sapphire substrate is not shown in the figure. The gate length is 0.7 μm, and the gate width is 150 μm. A semi-insulating GaN layer was grown over the sapphire substrate and a 1 nm interfacial AlN layer was grown over the semi-insulating GaN buffer layer. On top of the AlN layer, there is a 27.5 nm layer of n-type $Al_{0.22}Ga_{0.78}N$. Over this layer is a 0.25 nm unintentionally doped (UID) layer of $Al_{0.22}Ga_{0.78}N$. The n-type $Al_{0.22}Ga_{0.78}N$ layer is doped with silicon at 7×10^{18} cm^{-3}. These devices were fabricated at UCSB and were packaged in 40 pin DIP packages. The dimensions of the structure are provided in the figure. The devices used in this study had a passivation silicon-nitride layer over the gate-drain and gate-source access regions. There was no field-plate in these devices. The field

plate is a contact that extends over the gate-drain or gate-source access regions. The purpose of the field plate is to mitigate the large fields at the gate-drain and gate-source edges.

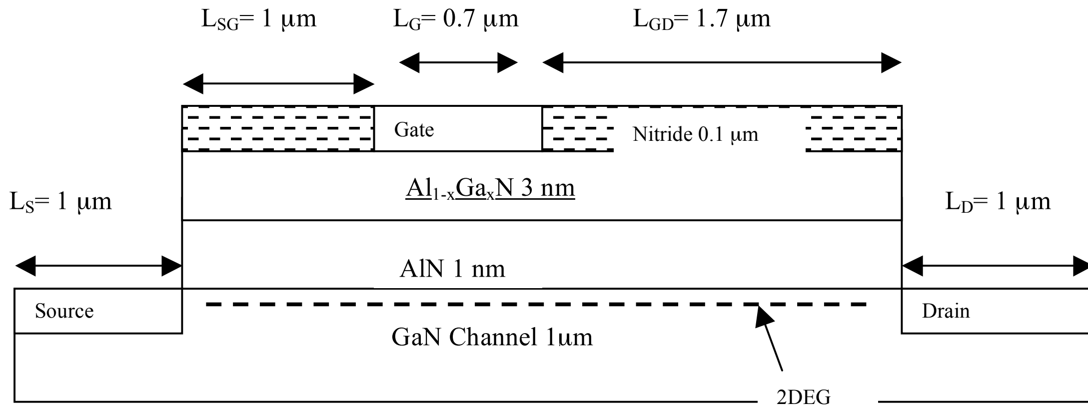


Fig. 7. Schematic diagram of the AlGaN/AlN/GaN HEMT structure used in the study

2.3 Band structure, IV characteristics, analytical model and polarization charge

2.3.1 Band structure

First we look at the representative band diagram for the GaN HEMT being studied. Figure 8 is a vertical cross section plot of the conduction band in the device.

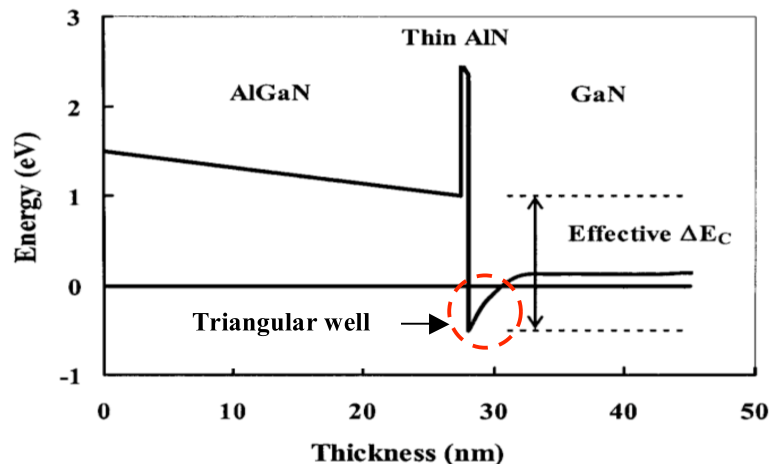


Fig. 8. Conduction band diagram of the devices used in the study.

The line at zero energy is the position of the Fermi level. Since the Fermi level is above the conduction band edge in the triangular well region, there are many electrons localized in that area. Since the electrons are confined in the triangular well in two dimensions, the layer of electrons in the well is called a 2DEG (two dimensional electron gas). The addition of the AlN layer in the thin film structure improves the mobility in the 2DEG [29]. Applying a gate voltage controls the 2DEG electron concentration; applying a voltage at the drain electrode controls the electron conduction. Changing the thin film structure of the device can change the 2DEG properties.

Figure 9 is a schematic diagram that explains the gate-control mechanism in this device. By controlling the Fermi-level position, the 2DEG density can be changed. These are depletion mode devices, and a gate voltage of 0 V corresponds to very large 2DEG densities.

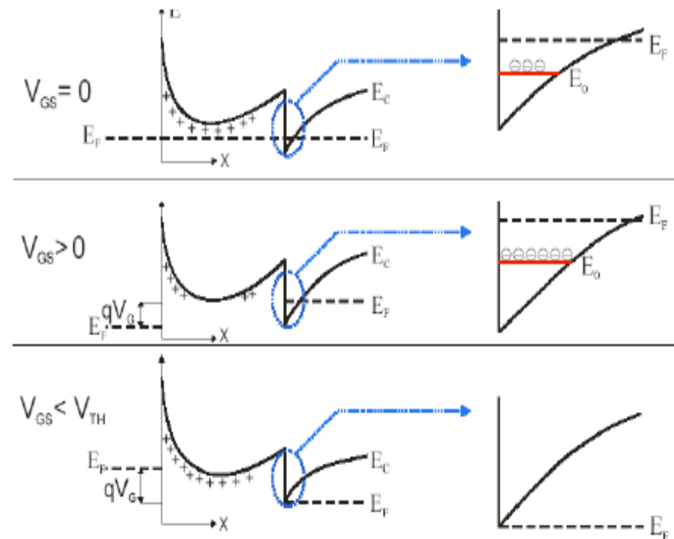


Fig. 9. Gate-control in a typical GaN HEMT device.

Here V_{TH} is the threshold gate voltage at which the 2DEG is completely pinched off. The devices used in this study have a V_{TH} of -7 V. V_{GS} is the gate-voltage, the source in these devices is always biased at 0 V. This makes the V_{GS} in figure 9 the same as V_G.

2.3.2 *I-V* characteristics

Applying a drain voltage leads to electron conduction in the device. Figure 10 is a plot of the typical I_D-V_D characteristics. For the larger gate-voltages and at large drain voltages we can see that the drain current decreases as the drain voltage increases due to self-heating. This phenomenon will be discussed in greater detail in Chapter 6.

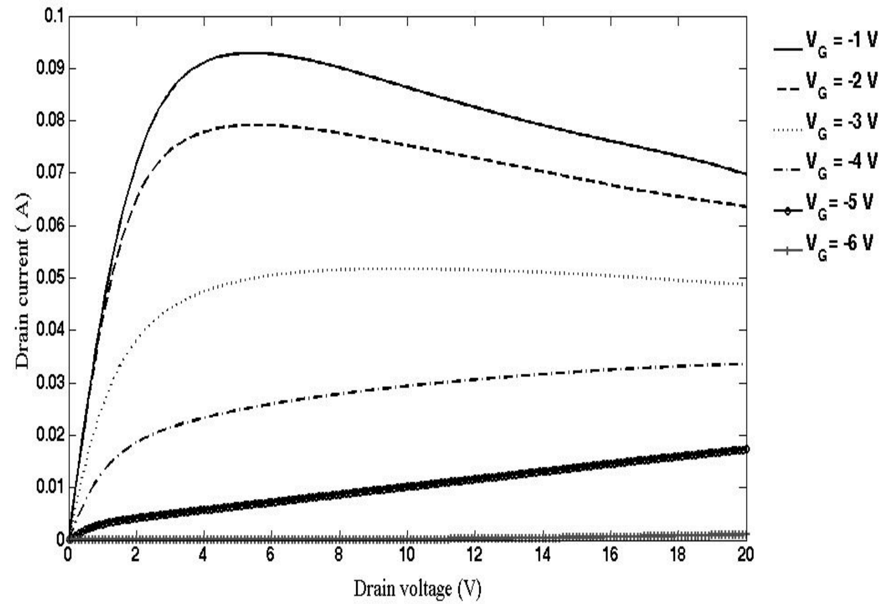


Fig. 10.Typical $I_D V_D$ characteristics of a GaN HEMT.

2.3.3 Analytical model for an AlGaN/GaN HEMT

This section summarizes the analytical models used to describe the behavior of HEMTs [21, 22]. These analytical models describe an approximation of the behavior of these devices. Studying the analytical models allows better understanding of the TCAD models. One of the key drawbacks in the analytical models is the inability to include effects of polarization charge and increased defect density on the characteristics of the device. The TCAD simulations described later in this dissertation do not have the above limitations. These TCAD simulations are self-consistent and model the HEMT in greater

detail by modeling the polarization charge in the device.

The analytical model discusses an AlGaN/GaN HEMT without the effect of the polarization charge. This makes the model inaccurate for AlGaN/AlN/GaN HEMTs where the polarization charge dominates. The conduction band discontinuity at the AlGaN/GaN interface creates a potential well; this well confines the 2DEG. The potential well is assumed to have only two quantum levels, E_0 and E_1, which are relevant for the operation of the device (other levels are always above the Fermi level). A self-consistent solution to the Poisson and Schrödinger equation gives us the 2DEG density. The 2DEG density (cm^{-2}) in terms of energy levels is as follows:

$$n_s = DkT\left\{\left[1+\exp\left(\frac{E_F - E_0}{kT}\right)\right]\times\left[1+\exp\left(\frac{E_F - E_1}{kT}\right)\right]\right\} \quad (2)$$

D is the density of states in the 2D potential well and the 2DEG density is given as:

$$n_s = \frac{\varepsilon}{qd}\left(V_{GS} - V_{TH} - \frac{E_F}{q}\right) \quad (3)$$

Here V_{GS} is the gate voltage, V_{TH} is the threshold voltage, E_F is the Fermi level and d is the thickness of the AlGaN between the Schottky gate and the 2DEG. The complete expression for the threshold voltage may be written as:

$$V_{TH} = \Phi_b - \Delta E_C - \frac{qN_D d_d^2}{2\varepsilon} - \frac{\sigma d}{\varepsilon} \quad (4)$$

Here Φ_b is the barrier height at the Schottky/AlGaN junction, and ΔE_C is the conduction band discontinuity at the AlGaN/GaN interface. Finally, in many devices an important factor is the polarization charge density σ. The charge is formed at the AlGaN/GaN or the AlN/GaN interface due to the highly polar nature of the GaN material system. Polarization charge is explained in greater detail in the next section. For the weak

inversion case (close to pinch off), the Fermi level is below most of the allowed energy states. The carrier density is small in the 2DEG. In this case the Fermi energy and the 2DEG density are expressed as:

$$E_F = kT \ln\left(\frac{n_s}{2DkT}\right) \tag{5}$$

$$n_s = 2DkT \exp\left(\frac{q(V_{GS} - V_{TH})}{kT}\right) \tag{6}$$

Beyond the weak inversion region (close to pinch off), the device operates in the strong inversion region. In this mode the sheet carrier density is much higher and the Fermi level is much higher in the potential well. The threshold voltage is conventionally defined as the beginning of the strong inversion region. The sheet carrier density and the Fermi level are given by the following expressions:

$$E_F = \frac{n_s}{2D} \tag{7}$$

$$n_s = \frac{2\varepsilon qD}{\varepsilon + 2q^2 Dd}\left(V_{GS} - V_{TH}\right) \tag{8}$$

The HEMT is a field effect transistor, and once the 2DEG is formed the current is controlled by the channel potential $V_C(x)$. The channel current is given by:

$$I = qn_s(x)Zv(x) \tag{9}$$

Here Z is the gate width and $v(x)$ is the electron velocity. As in a MOSFET, depending on the electric field, the velocity changes in the channel. At very high fields the velocity reaches its saturation level v_s, but below this limit the velocity is limited by

mobility. Thus, for the different electric field regimes we can write the expressions for electron velocities as follows:

$$v = \mu E, \text{ for } E < E_C \tag{10}$$

$$v = v_s, \text{ for } E \geq E_C \tag{11}$$

E_C is the critical field at which the velocity saturates; at electric fields less than the critical field, the current can be written as:

$$I = \mu Z \frac{\varepsilon}{d}\left(V_{GS} - V_C(x) - V_{TH}\right)\frac{dV_C}{dx}. \tag{12}$$

In the linear region of the device, we can approximate the last term in the above expression as follows:

$$I = \mu Z \frac{\varepsilon}{d}\left(V_{GS} - V_{TH}\right)\frac{V_C(L) - V_C(0)}{L}. \tag{13}$$

Here L is the gate length. The above expression can be modified to include the effects of the drain and source resistances R_D and R_S. Using the expressions $V_C(0) = R_S I$ and $V_C(L) = V_D - R_D I$ in (13) we get:

$$\frac{V_{DS}}{I_{DS}} = R_S + R_D + \frac{Ld}{\mu Z \varepsilon (V_{GS} - V_{TH})} \tag{14}$$

The above expression can be used to extract a number of useful physical parameters from the device-like 2DEG density and mobility using experimental I-V characteristics but there are some major drawbacks. The major drawbacks in this model are the absence of polarization charge and the inability to include the effect of defects and self-heating in the device. Since all of these parameters are necessary to model GaN HEMTs accurately, self-consistent TCAD models are employed.

The TCAD simulations in this study use a self-consistent solution of the Poisson and Schrödinger equations to describe the device characteristics correctly. The characteristics studied in this dissertation, namely band bending, mobility degradation due to self-heating, and DC to RF dispersion need the use a self-consistent simulation. Band bending needs the modeling of defects in the device. The time evolution of the filling and emptying of traps is necessary to study dispersion. Finally, to study self-heating in GaN HEMTs in detail, we need to couple the heat equation with the Poisson and Schrödinger equations. The details of these self-consistent simulations are provided in Chapter 4. In summary, to gain an accurate understanding of the impact of bulk traps in GaN HEMTs, we need the use of self-consistent TCAD simulations. The next section discusses the impact of the polarization charge on the 2DEG in detail.

2.3.4 Polarization charge

One of the key properties of GaN HEMTs is the presence of polarization charge at the interfaces. The presence of the polarization charge affects 2DEG density and is essential for the operation of AlGaN/AlN/GaN HEMTs. GaN and AlN are highly polar in nature. In proximity, these layers naturally will exhibit polarization-induced fields [30-32]. These fields are classified into spontaneous polarization and piezoelectric polarization. Spontaneous polarization refers to the built in polarization field present in an unstrained crystal. This field exists because the crystal lacks inversion symmetry and the bond between the two atoms is not purely covalent. This results in a displacement of the electron cloud towards one of the atoms in the bond. Thus, along the direction in

which the crystal lacks inversion symmetry, the asymmetric electron cloud leads to a net positive charge on one face of the crystal and a net negative charge on the other.

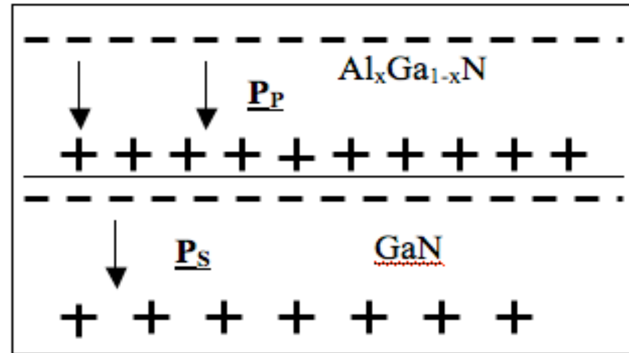


Fig. 11. Combined piezoelectric and spontaneous fields for AlGaN grown on GaN.

Piezoelectric polarization is the polarization field that results from the distortion of the crystal lattice. Due to the differences in lattice constants of AlN, GaN, and AlGaN, growing AlGaN on GaN leads to compressive strain in AlGaN [30-32]. This strain results in a charge sheet at the two faces of the crystal. As an example, figure 11 shows the combined piezoelectric (P_P) and spontaneous (P_S) electric fields in a structure with an $Al_xGa_{1-x}N$ layer grown on GaN. The polarization field increases with the Al content in the AlGaN. Thus, HEMT structures with AlN on GaN have very large polarization fields [29]. The impact of the polarization field on the 2DEG has been discussed in previous studies [30]. First, a 2DEG is formed in the GaN buffer layer even if there is no intentional doping in the AlGaN layer. Second, when the AlGaN layer is doped, it has very little effect on the 2DEG density. Experiments suggest that the 2DEG density increases only by 15% due to the doping in AlGaN. This 15% increase takes place when the AlGaN is doped beyond 10^{19} cm^{-3} [33]. The analytical relation between 2DEG density and the barrier potential (at the AlN/GaN interface) and other parameters in the HEMT is summarized by the following equations [34].

$$\phi_B = \frac{-qn_s t_1}{\varepsilon\varepsilon_0} + \frac{q(\sigma_{AlGaN} - n_s)t_2}{\varepsilon\varepsilon_0} - \frac{qn_s d_0}{\varepsilon\varepsilon_0} \quad (15)$$

$$n_s = \frac{\sigma_{AlGaN} t_2 + \sigma_{AlN} t_3 - \frac{\varepsilon\varepsilon_0 \phi_B}{q}}{t_1 + t_2 + t_3 + d_0} \quad (16)$$

Here n_s is the 2DEG density in the channel, σ_{AlGaN} is the net polarization charge density of the AlGaN, σ_{AlN} is the net polarization charge density of the AlN, t_1 is the thickness of the AlGaN cap layer, t_2 is the thickness of the AlGaN layer, t_3 is the thickness of the AlN layer, d_0 is the distance between the centroid of the 2DEG and the top UID-AlGaN/AlGaN interface, and ϕ_B is the surface potential. The lack of any doping term in (15) and (16) indicates that the 2DEG density in AlGaN/AlN/GaN HEMTs is mainly due to the polarization charge.

2.4 Traps in GaN HEMTs

Many studies have shown that trapping effects are the primary cause for degradation in the power densities in GaN HEMTs. These traps are either surface traps or bulk traps. These traps cause effects like DC to RF dispersion and gate-leakage [2, 6-8, 28]. This section discusses some of the key characteristics of surface and bulk traps found in these devices. The next section summarizes the impact that these traps have on GaN HEMT characteristics, in particular gate-lag (the recoverable reduction in the drain current transient response). It is clear from a survey of existing literature that the traps causing a departure from the ideal HEMT behavior can be present in the AlGaN, AlN as well as the GaN bulk material. Traps can also be present at the free AlGaN surface on top

of the device. We first consider the bulk traps and then discuss surface traps.

2.4.1 Bulk traps in GaN, AlGaN and AlN

The first question that needs to be answered is why there are traps in the GaN region. Current flow between the source and drain contacts in these devices can happen through the 2DEG and through leakage paths in the GaN bulk. The presence of electrons in the bulk degrades pinch-off characteristics. This can be avoided by making the GaN buffer layer semi-insulating and minimizing the leakage current [35]. To obtain minimal leakage through the buffer layer the electron density in the buffer must be minimized, or the Fermi level must be close to the intrinsic level or midgap. The Fermi level is close to midgap in materials of very high purity. Obtaining materials that have carrier concentrations at intrinsic levels is not possible from a fabrication standpoint. It is easier to pin the Fermi level at midgap by adding deep impurities. This method of obtaining insulating material has been used in GaN, GaAs and InP material systems and is known as compensation [35]. This eliminates buffer leakage but introduces many deep traps into the GaN. The method involves doping the material with impurities.

Typically GaN buffer layers have a background electron concentration due to the presence of oxygen and nitrogen vacancies [35]. Recent studies have shown that oxygen is the main impurity responsible for the background electron concentration [35]. The source of oxygen is impurities present in the NH_3 and metal-organic precursors used in MOCVD growth, and the residual water vapor in MBE or MOCVD chambers. Carbon impurities can act as compensating acceptors. Threading dislocations may also act as acceptors. This explains why some growth conditions lead to better semi-insulating GaN

layers as opposed to others. To get a good semi-insulating buffer layer, the densities of the carbon and oxygen impurities need to be well controlled. This is typically done by minimizing the concentration of unintentional donors (optimizing growth process) and by adjusting the incorporation of the compensating acceptors. The process of manufacturing a semi-insulating buffer introduces traps in the GaN buffer layer. The exact trap energy and densities of these traps are not known, but photoionization studies in GaN buffer layers grown for GaN MESFETs and HEMTs have reported deep traps 1.8 and 2.8 eV below the conduction band as the two main trap centers [25, 36-39]. These traps are believed to be acceptor-like. In summary, trapping centers in GaN buffer layers are due to the presence of impurities. These impurities are found in the material due to the processing techniques being employed. Therefore, the only way to estimate the exact number of trapping centers in the GaN buffer layer is by looking at the impurity concentrations in the GaN buffer layer. Some studies have estimated an upper bound of 10^{18} cm^{-3} as the impurity density in these layers [35]. Next we look at traps in the AlGaN layers.

Deep traps in AlGaN adversely affect device characteristics. These deep traps are attributed to carbon and oxygen. Studies of growth conditions of AlGaN have shown that both carbon and oxygen content increase with the increase in Al content. The concentrations of carbon and oxygen are both higher in AlGaN than in GaN. These are of the order of 10^{17} cm^{-3}. The strategy used to decrease these impurities in AlGaN is by minimizing cracking in the material and by ensuring that carbon and oxygen incorporation in the material is minimized. The energy of these traps is not very well known. Studies have suggested that these are deep acceptor-like traps [2].

2.4.2 Surface traps

Despite improvements in bulk GaN and AlGaN materials, issues like gate-lag and DC to RF dispersion did not improve by a large amount. This prompted many studies of the effects of gate-lag on surface states. Measurements of surface potential using floating gates in GaN HEMTs indicate that the surface in GaN HEMTs can become negatively charged. This indicates that surface states exist in these devices. The presence of very large polarization fields in the GaN system is a fundamental difference between conventional III-V semiconductors and GaN. Studies have also shown that large polarization fields in the GaN material system make it necessary for surface states to exist [28, 40]. These floating gate experiments provided the first direct evidence that the surface potential between the gate and drain becomes negative when the gate-drain diode is strongly reverse biased, which confirms the presence of surface states.

Surface states are of two kinds: intrinsic states and defect related states. The term “intrinsic” means that these states would exist on an ideally perfect surface. They correspond to solutions of Schrödinger’s equations with energy levels within the forbidden gap and to imaginary values of the wave vector ***k***: the wave functions are evanescent waves that decay exponentially with distance and exist only at the surface. “Extrinsic” surface states are caused by surface point defects or impurities at the surface, formed during crystal growth or in subsequent device fabrication processes such as metal evaporation. Together, these states are believed to be responsible for phenomena like gate-lag. Although the exact energies or the densities of these traps are not very well known, several studies have suggested that these traps are of the order of 10^{13} cm^{-2} and are donor type [25, 28]. The next section looks at the impact of traps on GaN HEMT

gate-lag characteristics and current collapse.

2.5 Impact of bulk and surface traps on HEMT characteristics

Several studies on GaN HEMTS suggest that traps affect the performance of GaN HEMTs adversely. Traps influence power performance through the formation of quasi-static charge distributions. These charge distributions are formed either on the wafer surface or in the layer under the 2DEG. This distribution reduces the drain current. Surface defects reduce the 2DEG density. Large defect densities in the AlGaN and GaN layers also degrade the 2DEG density and subsequently degrade the drain current [41]. Traps in the device also affect pinch off characteristics and gate-leakage currents adversely. In this section we will focus on the impact of bulk and surface defects on current collapse and gate-lag.

2.5.1 Current collapse

Current collapse in a nitride-based FET was first reported in an AlGaN/GaN HEMT by Khan *et al.* [7]. Figure 12 plots the *I-V* characteristics taken before and after the application of a large drain-source bias. The device was kept at a drain voltage of 20 V and a gate voltage of 0 V for many minutes. The DC *I-V* characteristics were measured again. The drain current could be recovered by illumination with light either corresponding to the GaN band gap or near 600 nm. Following earlier work done in the AlGaAs/GaAs system, the collapse was assigned to hot carrier trapping in the AlGaN. Binari *et al.* reported current collapse in GaN MESFETs [2]. Their results indicated that the drain current improved with illumination. The devices were illuminated with a broad

beam light source and with sources at different wavelengths. The drain current showed recovery with illumination.

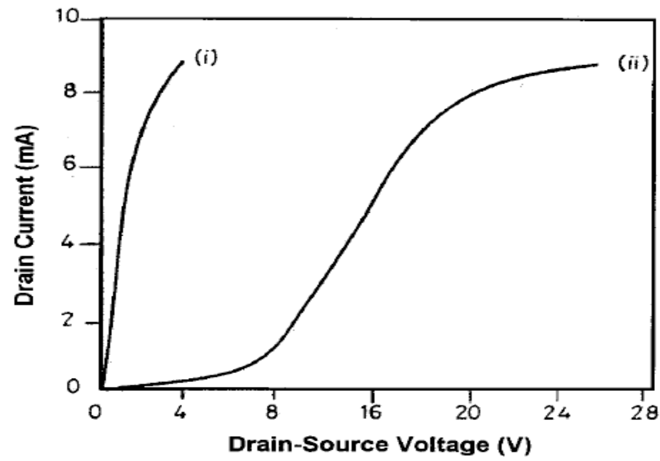


Fig. 12. Current collapse in GaN HEMTs. Drain current vs. drain voltage is plotted before (i) and after (ii) a drain bias of 20 V is applied (After [26]).

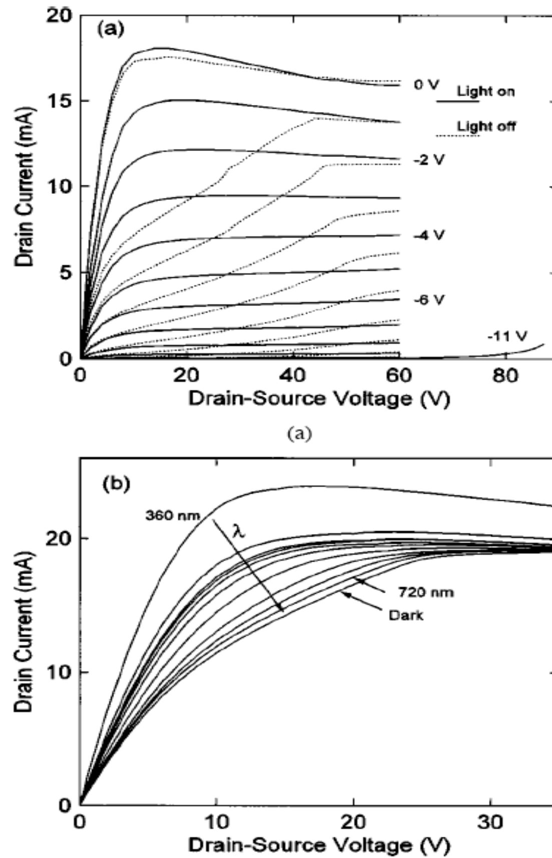


Fig. 13. (a) Current collapse in a GaN MESFET with (solid) and without (dotted) light illumination. (b) Drain current dependence on wavelength of light source (After [25]).

The different wavelengths penetrate deeply into the buffer layer of the device,

suggesting that the majority of the contribution is from the buffer layer [2]. Figure 13 is a plot reproduced from the MESFET study showing the recovery in the drain current with illumination. These results suggest that deep traps in the highly resistive buffer layer below the channel caused the collapse. As discussed in the previous section, these layers have a lot of traps to compensate for the shallow donors present due to oxygen and nitrogen impurities. Other studies were also able to confirm the location of these traps [35]. These results on MESFETs suggest that similar traps might be responsible for current collapse in GaN HEMTS. Studies on GaN HEMTs have also indicated that deep traps in the buffer GaN region dominate current collapse. In summary, bulk traps in the buffer GaN region have been suggested to be the main cause for current collapse.

2.5.2 Gate-lag

Gate-lag is defined as the reduction in the drain current observed in the pulsed *I-V* characteristics relative to DC measurements made at the same bias point. Pulsed-gate *I-V* measurements are made by keeping the drain voltage constant and pulsing the gate from the "off" to "on" state. Figure 14 is a plot of the pulsed *I-V* characteristics for an unpassivated GaN HEMT. The pulsed drain currents are much smaller than the DC currents.

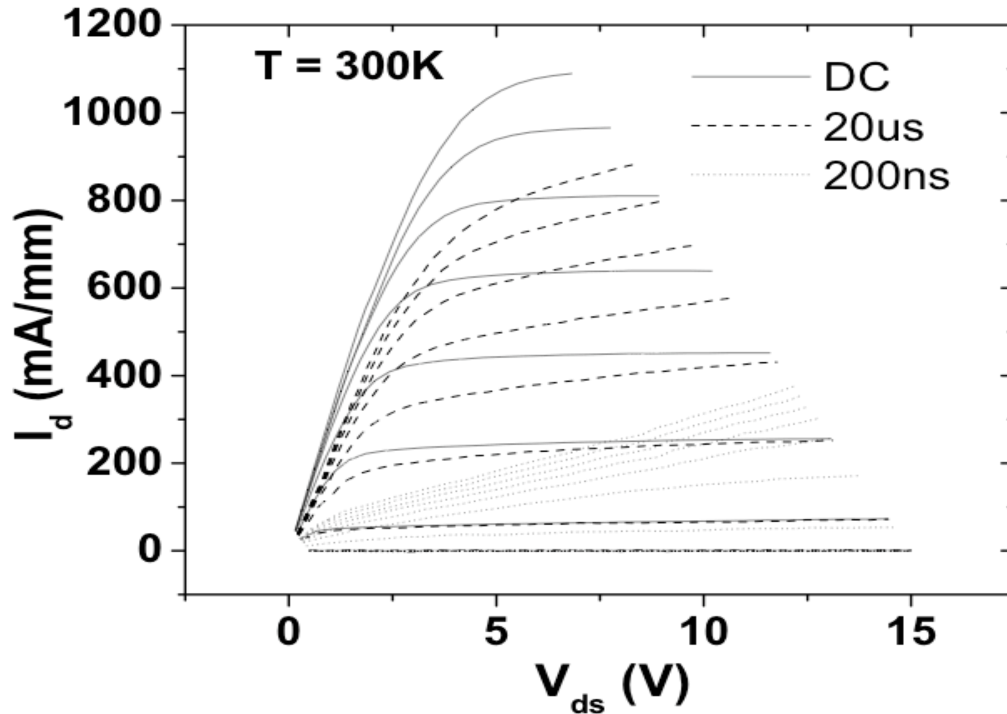


Fig. 14. Pulsed and DC *I-V* characteristics for an unpassivated GaN HEMT [65].

Most studies suggest that gate-lag is directly related to the defects present on the surface [28]. This is suggested to be caused by the formation of virtual gate in the drain and gate access regions [28]. Studies also show a substantial reduction in the amount of gate-lag with annealing and the inclusion of a passivation layer [10]. These studies further suggest a close relationship between surface traps and gate-lag. Figure 1 indicates the nitride passivation layer in the HEMT structure. Figure 15 is a plot of the pulsed *I-V* characteristics after the addition of a silicon nitride passivation layer on top of the device. There are other studies that suggest that bulk defects in the GaN buffer may also cause gate-lag [5], as a result of the capture of hot electrons in bulk traps in the GaN buffer [5, 42]. Thus, while the majority of studies suggest that the surface trap mechanism is the primary mechanism responsible for gate-lag, bulk effects must also be considered. The

detailed mechanism behind the gate-lag and the relationship with bulk and surface defects is explained in greater detail in Chapter 7.

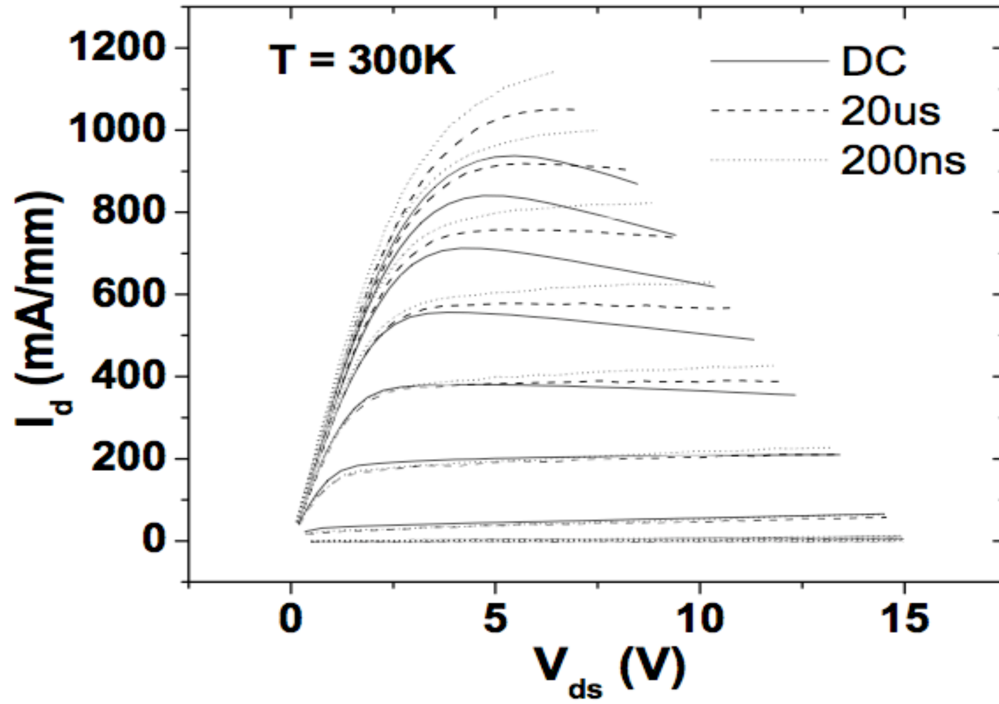


Fig. 15. Pulsed *I-V* characteristics of a passivated GaN HEMT [65].

CHAPTER 3

EXPERIMENTS

This chapter describes the details of the devices used in this study and the experiments that were conducted. The experiments are divided into DC, gate-lag, and irradiation experiments. All the devices used in this study were packaged in 40 pin DIP packages. A cross-sectional view of the device structure is shown in figure 16. In addition to the thin film structure, the sapphire substrate layer is also shown.

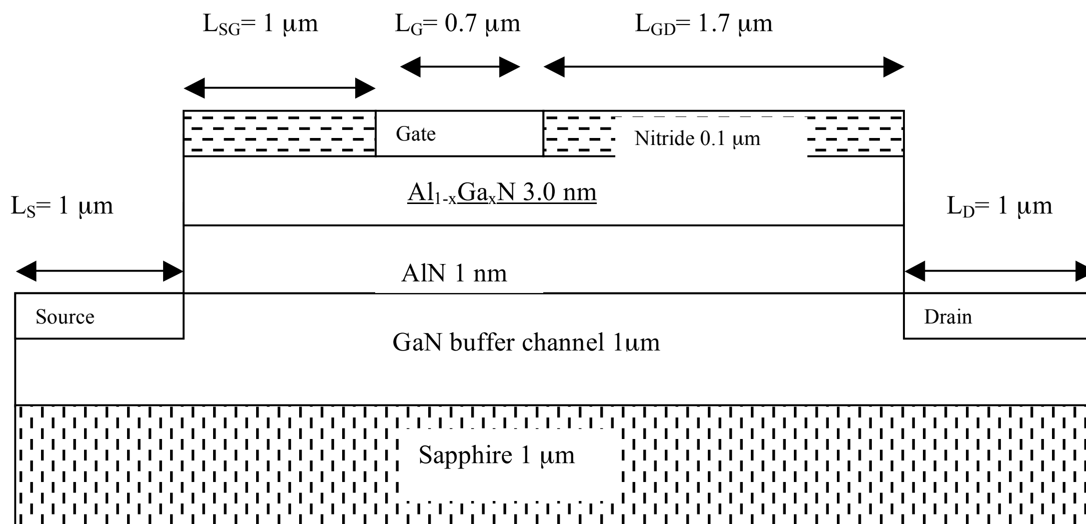


Fig. 16. Schematic diagram of the AlGaN/AlN/GaN HEMT structure used in the self-heating simulations.

3.1 Radiation experiments

The purpose of the irradiation experiments was to study the impact of bulk defects on device properties in a controlled manner. The AlGaN/AlN/GaN HEMTs were irradiated at the Vanderbilt University Van De Graaff proton accelerator facility with 1.8 MeV protons. The ion currents ranged from 6 nA to 40 nA. The fluences ranged from 3 ×

10^{12} to 5×10^{14} protons/cm^2. All radiation exposures were performed at room temperature. All the pins of the devices were grounded during the irradiations.

3.2 Characterization Experiments

The characterization experiments are divided into two distinct categories: DC characterization and gate-lag measurements. DC characterization acquires *I-V* characteristics, whereas the gate-lag transients are measured using an RF characterization system. This section presents the results obtained from the above-mentioned experiments.

3.2.1 **DC characterization**

The DC characterization was done using an HP 4156B parameter analyzer. The gate voltage was varied between -8 V (pinch off) and -1 V. The drain voltage was varied from 0 V to 15 V. Figure 17 is a plot of the pre-irradiation DC *I-V* characteristics. Self-heating induced reduction in the drain current is evident at the higher drain voltages. Figure 18 is a plot of the *I-V* characteristics at 4 different fluences. The drain current decreases with increasing fluence. The mechanisms that cause the reduction in drain current will be discussed in Chapter 5.

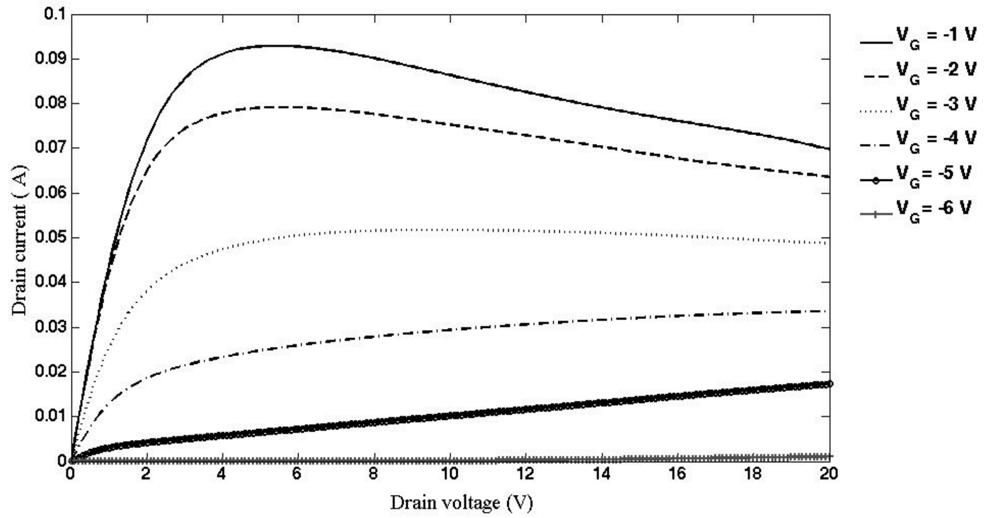


Fig. 17. Pre-irradiation experimental IV characteristics.

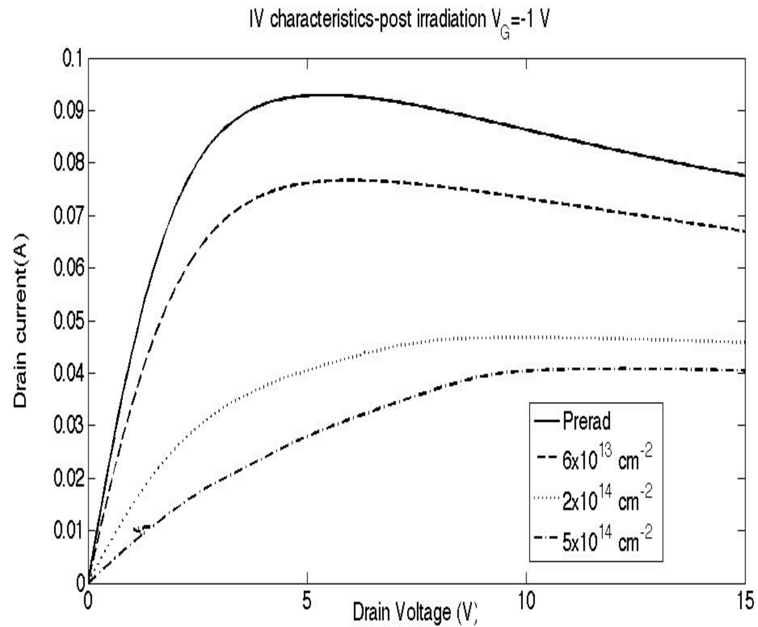


Fig. 18. Post-irradiation *I-V* characteristics.

3.2.2 Gate-lag characterization

The gate-lag transients in the devices were measured for various bias conditions. Gate-lag is defined as a recoverable collapse in the drain current. The experiment was performed using the setup shown in figure 19. A pulsed gate bias from V_G = -8 V to V_G = -1 V was applied to the gate. The drain voltage was 5 V.

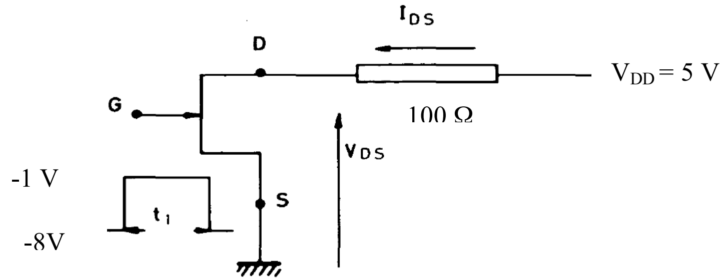


Fig. 19. Setup to measure gate-lag characteristics.

The transients for the drain current were measured across the 100 Ω load using a digitizing oscilloscope. The pulse width and period of the gate pulse were 20 ms and 100 ms, respectively. The rise time of the pulse was 22 ns. This provides a duty cycle of 20%. Figure 20 is a plot of gate-lag transients for 2 different drain biases for the pre-irradiation case. The amount of collapse is also indicated in the plot. There is approximately a 70% collapse in both cases.

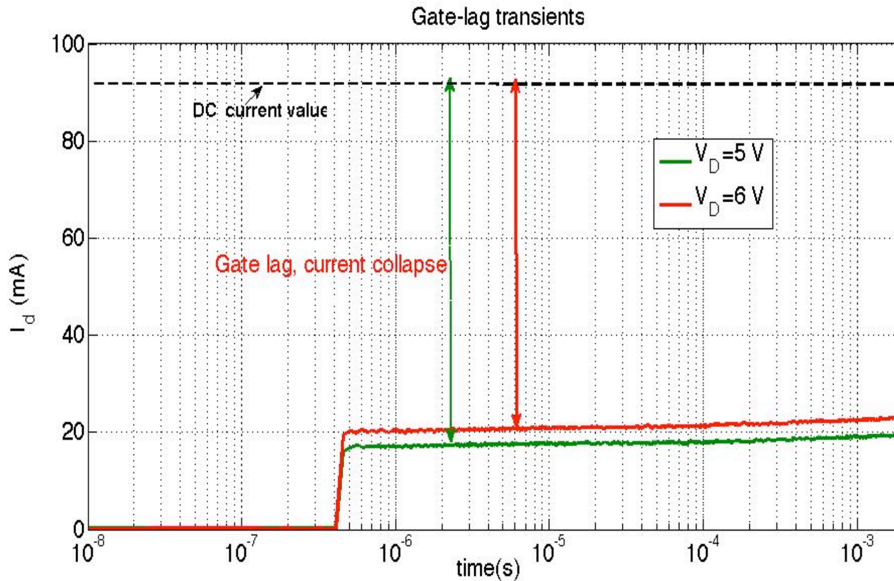


Fig. 20.Gate-lag transients measured at two different drain voltages.

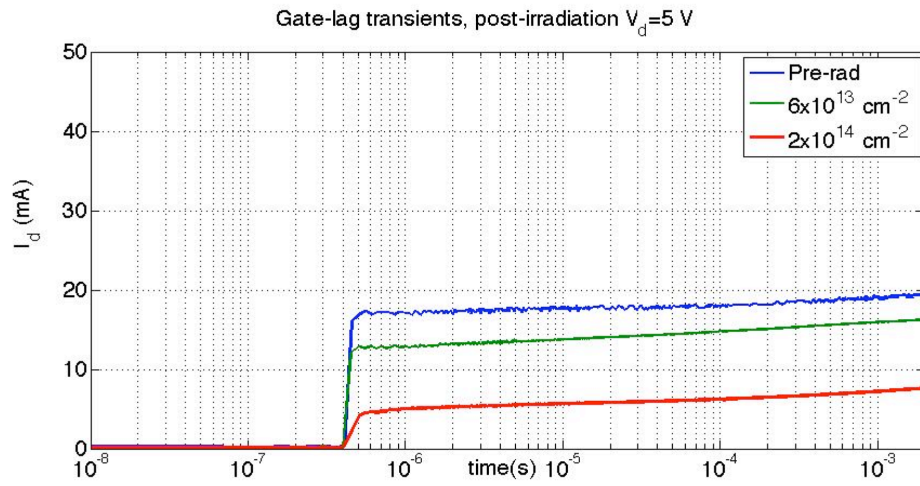


Fig. 21.Gate-lag transients measured at different fluences.

Figure 21 is a plot of the post irradiation gate-lag transients at 3 different fluences. There is degradation in the maximum drain current with increasing fluence.

CHAPTER 4

SIMULATIONS

TCAD simulations were used to analyze the device operation. SRIM (stopping range of ions in matter) simulations were used to estimate the defect density in the various layers of the device [43]. The models used with the TCAD simulations help to understand the *I-V* characteristics, including phenomena such as gate-lag, as well as the impact of defects on these characteristics. This chapter describes the various simulations used in this thesis. The basic structure used in these simulations is depicted in figure 22.

The band bending simulations described in Chapter 5 do not incorporate the sapphire substrate. The gate-biases described in Chapter 5 are low enough (V_G = -3 V and -4 V) that self-heating effects are not a big issue and the sapphire substrate need not be modeled. The self-heating simulations discussed in Chapter 6 do incorporate the sapphire substrate. The sapphire substrate does not affect the simulation results described in Chapter 5, but they do affect the self-heating simulations discussed in Chapter 6.

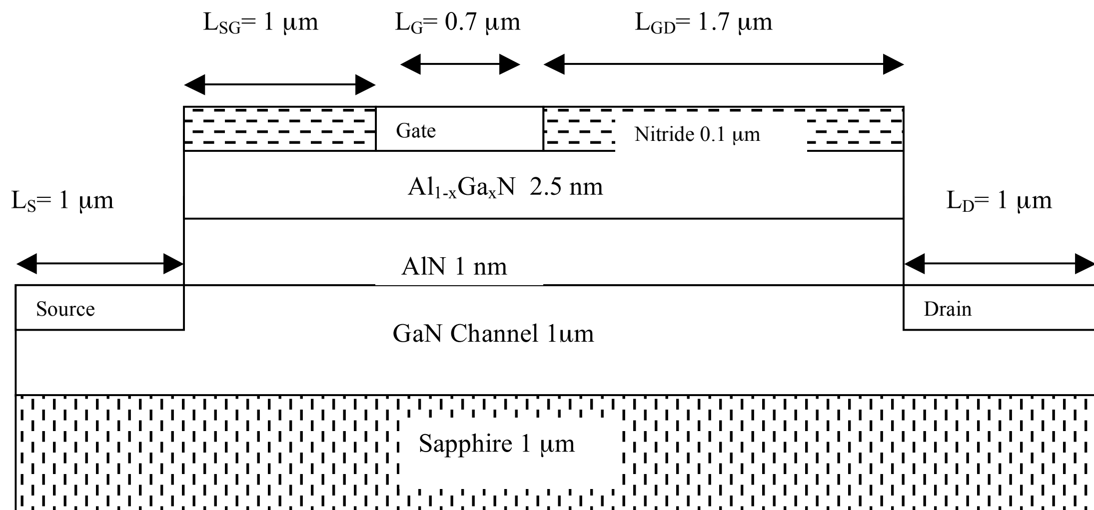


Fig. 22. Schematic diagram of the AlGaN/AlN/GaN HEMT device used in the self-heating simulations.

The thermal conductivity of the sapphire substrate needs to be modeled to accurately capture the diffusion of heat generated in the device. Finally, the gate-lag simulations do not incorporate the AlN layer in the thin film structure. This was done to improve convergence in the simulations.

4.1 SRIM simulations

SRIM is a group of programs that calculate the stopping and range of ions (up to 2 GeV/u) in matter using a model of ion-atom collisions. This calculation is made very efficient by the use of statistical algorithms that allow the ion to make jumps between calculated collisions and then average the collision results over the intervening gap [43]. During the collisions, the ion and atom have a screened Coulomb collision, including exchange and correlation interactions between the overlapping electron shells. The ion is allowed long-range interactions that can create electron excitations and plasmons within the target. These are calculated from a description of the target's collective electronic and inter-atomic bond structure that is included in the setup of the simulation (tables of nominal values are supplied). The charge state of the ion within the target is described using the concept of effective charge, which includes a velocity-dependent charge state and long range screening due to the collective electron sea of the target. SRIM provides the number of defects in the various regions of the structure but does not provide any information about the electrical characteristics of these defects. The defect density is calculated by calculating the non-ionizing energy loss (NIEL) in the device. This is then used to calculate the number of defect centers [43].

The number of defects corresponding to a given proton fluence was estimated using SRIM; these results are consistent with previously published results [44]. The thin film structure described in figure 1 was simulated in SRIM for irradiation with 1.8 MeV protons. Figures 23 and 24 are plots of the defect densities in the AlGaN and GaN layers obtained from SRIM. The energies of these traps are obtained from previously published literature on proton implantation. These trap energies are discussed in detail in Chapter 5. The defect densities in the AlGaN and GaN layers calculated by the SRIM simulations are used in the TCAD simulations.

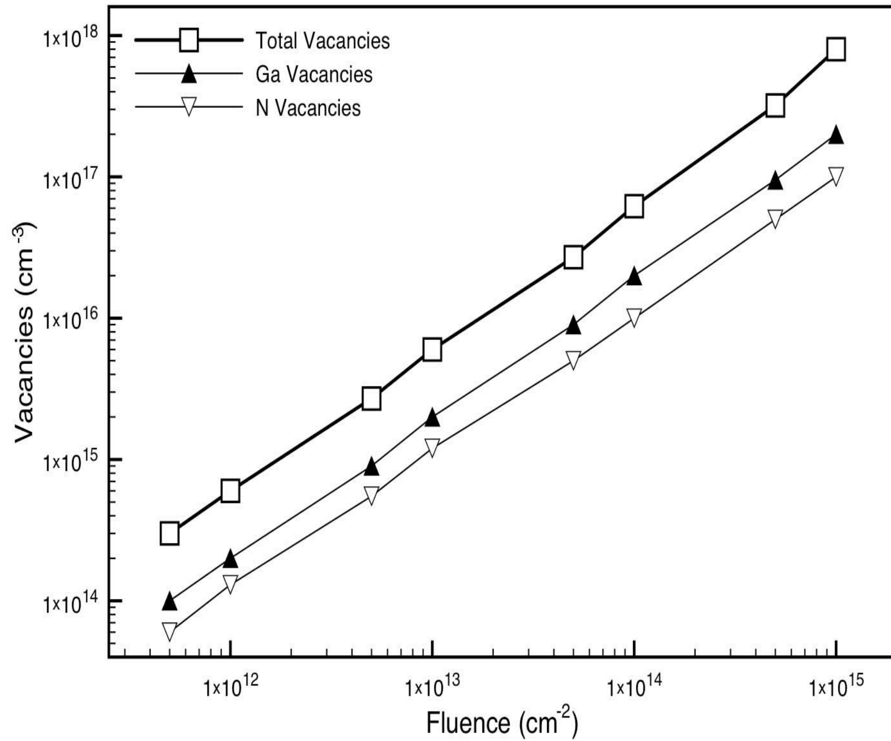


Fig. 23. Vacancies in GaN obtained from SRIM.

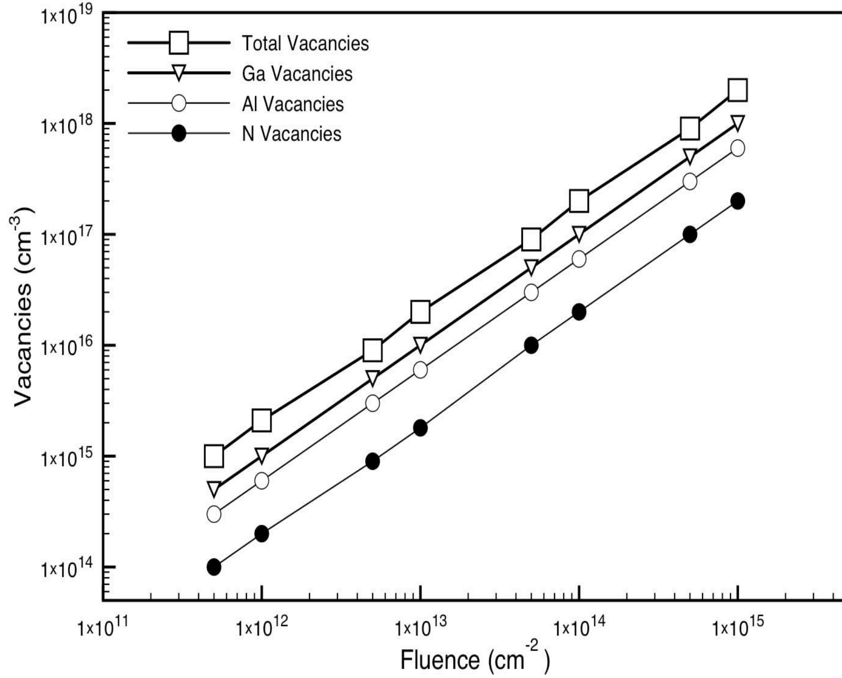


Fig. 24. Vacancies in AlGaN obtained from SRIM.

4.2 TCAD simulations

TCAD simulations are used to investigate the sensitivity of the GaN HEMT structure to bulk defects. This section describes the models used to simulate the GaN HEMTs used in this study.

4.2.1 DC *I-V* characteristics

The structure simulated is shown in figure 1, corresponding to the devices that were fabricated at UCSB and tested in this work. The model parameters required for simulating GaN, AlN, and AlGaN were obtained from material tables present in Synopsys Sdevice simulator [45]. These parameters are summarized in table 2. HEMT devices are difficult to simulate because they involve self-consistent solutions to the Poisson, current-continuity, and Schrödinger equations. There is coupling between the

Poisson equation and the Schrödinger equation, which allows one to calculate the potential in the device. This is then used in conjunction with the current-continuity equation to generate the *I-V* characteristics of the device.

Property	GaN	AlN	$Al_{0.22}Ga_{0.78}N$
Dielectric constant	9.5	8.5	8.8
Energy gap (eV)	3.47	6.2	4.28
Electron affinity (eV)	3.4	1.9	2.9
Electron mobility (cm^2/V.s)	1100	300	600
Saturation velocity (cm/s)	2.1×10^7	1.5×10^7	1.8×10^7
Cond band density of states (cm^{-3})	2.65×10^{18}	1.3×10^{18}	1.9×10^{18}
Energy relaxation time (ps)	0.1	0.1	0.1

Table. 2. Properties used in TCAD simulations.

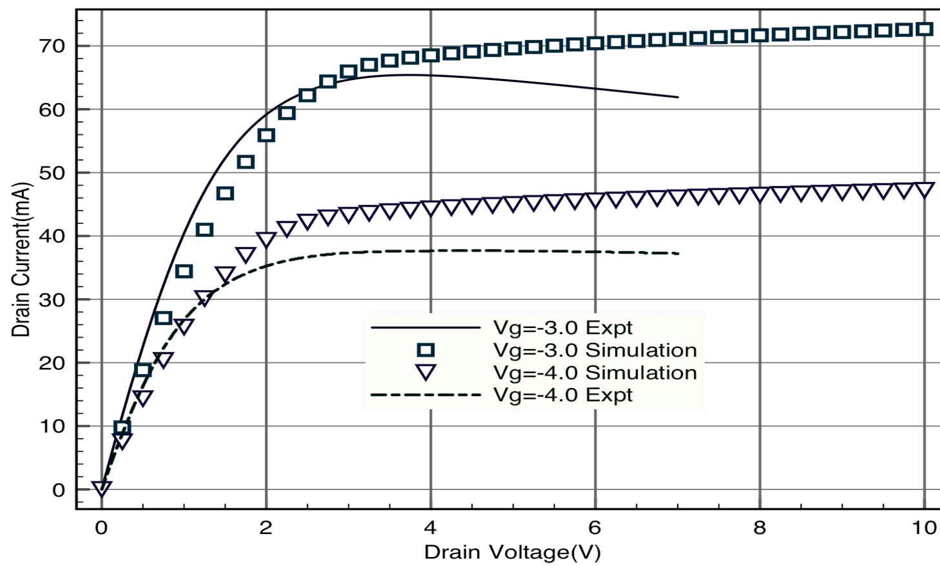


Fig. 25. I_D-V_D characteristics at two different gate voltages.

The net polarization charge density at the AlN/GaN interface was assumed to be 1.2×10^{13} cm^{-2}, as determined from previous studies quantifying polarization charge at different interfaces in HEMTs [31, 32]. Without the polarization charge, there is no

2DEG at the AlN/GaN interface. Figure 25 shows the results comparing simulations and actual device data. These simulations do not include self-heating.

The 2DEG density is closely related to the polarization charge at the AlN/GaN interface. This is modeled as a positive fixed charge density at the AlN/GaN interface. These simulations without self-heating are used to study the effects of defects on *I-V* characteristics at lower gate-biases (from -8 V up to -3 V). At these voltages self-heating effects are not as dominant as at higher gate-voltages. This allows the study of effects such as band bending and mobility degradation due to charged defects in these devices. Chapter 5 discusses these effects in greater detail.

The modeling of charge transport in semiconductors involves a self-consistent solution to Poisson's equation, as well as the hole and electron continuity equations. First we look at an isothermal case and then we describe the non-isothermal case that describes self-heating. The Poisson equation is:

$$\nabla \cdot \varepsilon \nabla \phi = -q(p - n + N_D - N_A) - \rho_{trap} \quad , \tag{17}$$

where ε is the electrical permittivity, q is the elementary electronic charge, and n and p are the electron and hole densities, N_D is the concentration of ionized donors, N_A is the concentration of ionized acceptors, and ρ is the charge density contributed by traps and fixed charges. The current continuity equations for electrons and holes are:

$$\nabla \cdot \vec{J}_n = qR_{net} + q\frac{\partial n}{\partial t} \qquad -\nabla \cdot \vec{J}_p = qR_{net} + q\frac{\partial p}{\partial t} \tag{18}$$

Here R_{net} is the net electron hole recombination rate and J_n and J_p are the electron and hole current densities. The drift-diffusion model is used to capture the electron and hole

current densities. They are summarized as follows:

$$\vec{J}_n = -nq\mu_n \nabla\Phi_n$$

$$\vec{J}_p = -pq\mu_p \nabla\Phi_p \tag{19}$$

where μ_n and μ_p are electron and hole mobilities, and ϕ_n and ϕ_p are electron and hole quasi-Fermi potentials.

4.2.2 Self heating simulations

This section describes the models used to simulate self-heating effects in TCAD. These models are described in further detail in ISE-TCAD [45]. The non-isothermal model modifies the drift-diffusion equations to account for the effects of self-heating. The assumption here is that the lattice is in thermal equilibrium with the charge carriers. This implies that the carrier and lattice temperatures are described by a single quantity *T*. *T* is calculated by coupling the lattice heat equation and the modified drift-diffusion equation. The modified drift-diffusion equation includes the generalized heating term as follows.

$$\vec{J}_n = -nq\mu_n(\nabla\Phi_n + P_n\nabla T)$$

$$\vec{J}_p = -pq\mu_p(\nabla\Phi_p + P_p\nabla T) \tag{20}$$

P_n and P_p are the electron and hole thermoelectric powers for non degenerate

semiconductors [45]. The lattice heat equation is:

$$c_L\frac{\partial T}{\partial t} - \nabla \cdot \kappa \nabla T = -\nabla \cdot [(P_n T + \Phi_n)\vec{J}_n + (P_p T + \Phi_p)\vec{J}_p] - \left(E_C + \frac{3}{2}kT\right)\nabla \cdot \vec{J}_n - \left(E_V - \frac{3}{2}kT\right)\nabla \cdot \vec{J}_p + qR_{net}(E_C - E_V + 3kT) \quad (21)$$

Here κ is the lattice thermal conductivity of the semiconductor material, c_L is the lattice heat capacity and E_C and E_V are the conduction and valence band energies. Our simulations use the physics described above and generate a self-consistent solution of equations 1-5. The thermal conductivities of the GaN, AlGaN AlN, and sapphire layers in the simulations are 2.075, 1.5, 1.3 and 0.35 (W/K-cm), respectively. The lattice heat capacity for the materials is 3.275, 3.125, 3.0 and 2.89 (J/K-cm^3), respectively. The polarization charge density at the AlN/GaN interface in the simulations was 1.2×10^{13} cm^{-2}, as discussed previously.

Figure 26 shows the simulation results compared with actual device data. The self-heating is included in the simulation results. The 2DEG room temperature Hall mobility measured by our collaborators at UCSB was 1100 cm^2/(V-s); this value was used in the simulations as the room temperature mobility. The v_{sat} value in the 2DEG region at room temperature was fixed at 1.1×10^7 cm/s, which is consistent with previous studies [46]. In addition to the equations described above, mobility and saturation velocity are temperature-dependent. The coupling relation between room temperature mobility and lattice temperature used in the simulations is

$$\mu(T) = \mu_0\left(\frac{T}{T_0}\right)^{-3} \quad (22)$$

where μ_0 is the room temperature mobility and T_0 is 298 K. The coupling relation

between v_{sat} and the lattice temperature is

$$v_{sat}\left(T\right) = A_{vsat} - B_{vsat}\left(\frac{T}{T_0}\right) \tag{23}$$

where A_{vsat} is 1.7×10^7 cm/s and B_{vsat} is 0.5×10^7 cm/s. Figure 26 is a plot of the *I-V* characteristics with the self-heating model described in this section.

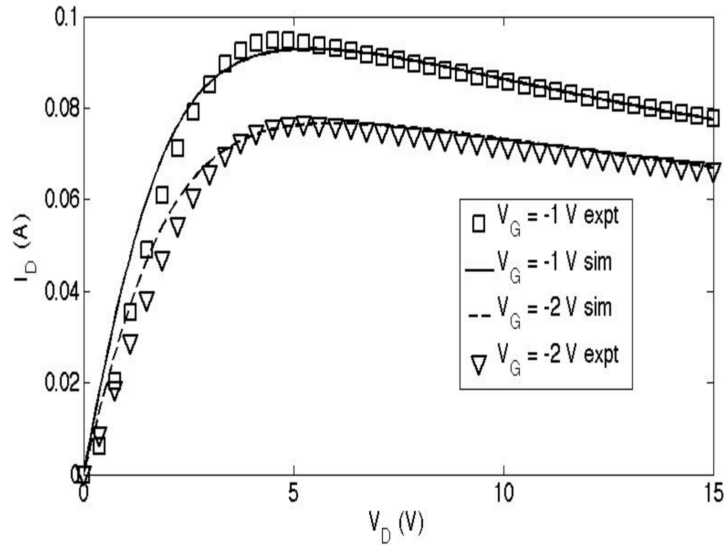


Fig. 26. I_D-V_D characteristics at two different gate voltages including self-heating.

Chapter 6 discusses these simulations in greater detail, including the impact of self-heating on mobility and saturation velocity. The chapter also discusses the interplay between self-heating, mobility, and bulk defects in the structure.

4.2.3 Dispersion simulations

As noted above, gate-lag has been attributed to two main mechanisms. The first mechanism involves surface traps [28]. The second mechanism involves the trapping of hot electrons in bulk traps at the gate edges [5]. The AlN layer in the HEMT was not

simulated. Increasing the mobility values to 1100 cm^2/V-s captured the effect of the AlN layer. In the device the very thin (1 nm) AlN layer improves the mobility by reducing dopant scattering [29]. Since this layer is very thin, inclusion of the layer in the TCAD deck can cause convergence issues. Increasing the mobility in the 2DEG and removing this layer from the TCAD deck allows us to bypass this problem while retaining the improvement in mobility due to the AlN layer. This section summarizes the models used to describe these two dispersion mechanisms in the simulations.

4.2.3.1 Surface trap mechanism

The surface trap mechanism involves a change in the net charge density at the AlGaN/passivation interface. The mechanism is better described using a chart of the various space-charge components in the device. Figure 6 is a schematic plot of the relevant space charge components at the surface and in the device.

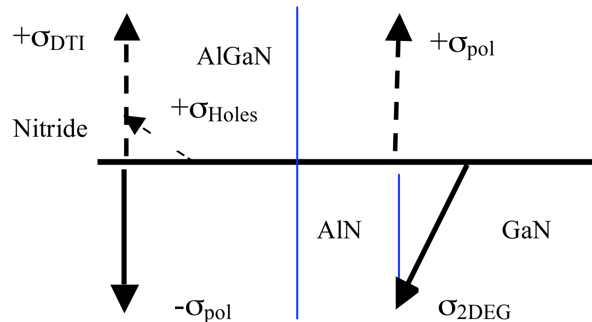


Fig. 27. Space charge components in the GaN HEMT device studied.

In Figure 27, $\pm\sigma_{pol}$ is the fixed polarization charge density at the interfaces. σ_{2DEG} is the 2D electron gas density, σ_{Holes} is the free hole accumulation charge density at the surface, and σ_{DTI} is the ionized donor trap density at the surface. The positive components are indicated with dashed arrows pointing upwards; the solid arrows pointing downwards indicate the negative components. The angled arrows are the very thin hole and electron

bulk densities at the surface and the AlN/GaN interface, respectively. The blue lines indicate the AlGaN/AlN and AlN/GaN interfaces. The relationship between the surface components is given by

$$\sigma_{net} = -\sigma_{pol} + \sigma_{Holes} + \sigma_{DTI} \tag{24}$$

The mechanism can be explained by looking at the change in the above-mentioned space charge components at the surface. A net change in the space charge at the surface will affect the 2DEG density in the channel.

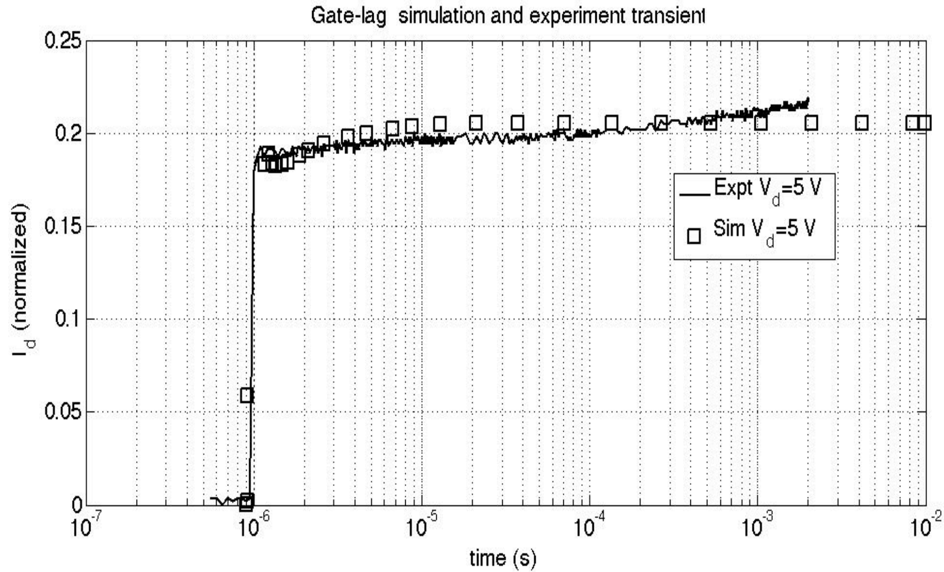


Fig. 28. Gate-lag transient simulated using the surface trap mechanism.

Figure 28 is a plot comparing the experiment and the simulated gate-lag transient. The current has been normalized to the drain current measured in the DC characterization. There is good agreement between experiment and simulation. We assumed a surface fixed charge density of -1.2×10^{13} cm^{-2}. These donor-like traps were assumed to be 0.35 eV and 0.5 eV from the valence band. The amount of gate-lag is

sensitive to the trap parameters used. The mechanism and the trap parameters are analyzed in greater detail in Chapter 7.

4.2.3.2 Hot electron capture mechanism

Previous studies on HFETs, MOSFETs and MESFETs suggest that enhanced trapping of hot electrons in bulk traps near gate edges contributes to current collapse. These studies also suggest that current collapse is related to hot electrons spreading deeply into the bulk GaN region of the device [42, 47].

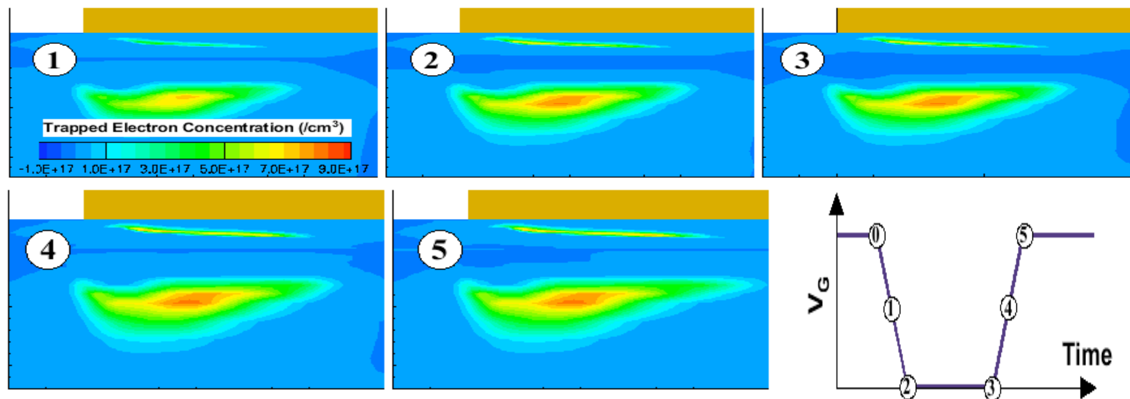


Fig. 29. Mechanism behind bulk states causing dispersion in a GaN HEMT.

This mechanism can be explained as the capture of hot electrons from the channel in the buffer traps. This depletes the 2DEG and causes a reduction in the drain current. Figure 29 illustrates the time evolution of the hot electrons being captured by buffer traps. The magnitude of the collapse depends on a variety of conditions like trap density and trap distribution, trap energy, and the presence or absence of a passivation layer on the surface. This phenomenon is described using the hydrodynamic charge transport model in the simulator [45]. Drift-diffusion transport equations are not adequate to model effects like velocity overshoot in GaN HEMTs [45]. These effects are critical for accurate

modeling of electron penetration deep into the bulk. Monte Carlo methods involving the solution of the Boltzmann kinetic equation are the most general approach. The drawback of these methods is the very high computational time required [45]. The hydrodynamic model, also called the energy balance model, provides a very good approximation to these Monte Carlo methods [48]. The hydrodynamic model used in Sdevice solves six PDEs. In general the hydrodynamic model includes the Poisson, continuity and energy conservation equations for holes and electrons [45]. The simulator manual discusses the model in much greater detail [45].

Previous simulations in the literature suggest that the amount of collapse observed depends on the specific spatial and energetic distribution of the traps used [11]. As an example, a uniform trap distribution of traps in the various layers of the GaN HEMT does not produce as much collapse when compared to enhanced trap distribution under the gate edge. This suggests that traps near the gate-edge are more effective than elsewhere in the device. Figure 30 shows results from a simulation of the enhanced trapping case. The distribution is assumed to be Gaussian with a width of 0.1 μm.

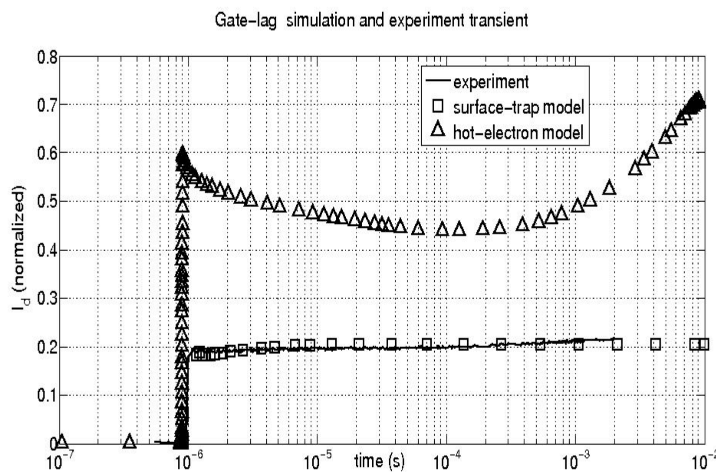


Fig. 30. Gate-lag transient simulated using the hot-electron and the surface trap mechanisms.

The peak trap density used to get these results shown in Fig. 30 is 3.5×10^{18} cm^{-3}. These simulations assume that there is a passivation layer, but no field plate. This Gaussian distribution is superimposed over a uniform trap distribution of 6.5×10^{18} cm^{-3}. The amount of collapse also depends on trap energy, trap density, and the presence or absence of a passivation layer. Chapter 7 discusses this parameter space in greater detail. Figure 30 also includes the experimentally observed collapse and the surface trap model curves.

CHAPTER 5

THE ELECTROSTATIC EFFECTS OF BULK TRAPS IN GAN HEMTS

5.1 **Introduction**

In this chapter we look at the electrostatic impact of charged defects on the performance of AlGaN/AlN/GaN HEMTs. Bulk defects of the order of 10^{16} cm^{-3} are common in GaN HEMTs [37, 49]. Since the defect densities in these devices will degrade device characteristics, there is a need to understand the relationship between bulk traps in these devices and DC characteristics. This chapter quantifies the relationships between charged traps and quantities like band bending and mobility in the 2DEG of the device using calibrated TCAD models. A change in these quantities directly affects the DC *I-V* characteristics of the device. Experimentally, bulk traps are added in the device in a controlled manner using a low energy proton beam. Low energy protons cause displacement damage in the structure. The displacement damage directly leads to bulk traps in different regions of the device. This chapter looks at the electrostatic impact of bulk traps.

Many studies in the literature have described the measured proton irradiation-induced change in the DC *I-V* characteristics using quantities that were extracted from existing quantitative models, namely the 2DEG density, the threshold voltage, or the mobility [50,44]. These studies do not directly address the mechanisms behind the change in the 2DEG density. Also, in these studies the proton irradiation-induced degradation in DC *I-V* characteristics was not related directly to the density of radiation-induced traps

using self-consistent simulations. The advantage of the self-consistent model is that it predicts the 2DEG density more accurately by including the effect of polarization charge. Also, the self-consistent model is necessary to understand the interplay between charged defects, polarization charge, and the 2DEG density. This effect is not very well described by the analytical models used previously [21,22]. A previous self-consistent model of radiation damage in GaAs HEMTs was based on the dependence of the 2DEG density on the doping in the doped AlGaAs layer [51]. However, for the devices used in this study, the 2DEG density is very strongly related to the polarization charge [52,34,33].

In this work, we show how the 2DEG density decreases due to the electrostatic effects of charged deep-level defects (band bending). The different layers in these devices are meant to be undoped but the presence of defects causes the layers to be unintentionally doped. The roles of defect location and energy level are quantified. In the next section we discuss the defects and vacancies created in GaN, AlGaN and AlN by low energy proton irradiation. This information is used with SRIM data to estimate the trap parameters for use in the TCAD models.

5.2 Vacancies and defects in GaN and AlGaN

The number of defects corresponding to a given proton fluence estimated using SRIM is consistent with previously published results [44]. These results were summarized in the previous chapter. For this study, the energy levels of defects in GaN and AlGaN were estimated from proton implantation studies performed at 1 MeV [11], [12]. These studies were performed on bulk GaN and AlGaN samples. The experiments described in this dissertation were performed on HEMT structures that have both GaN and AlGaN layers. The proton energy used was 1.8 MeV. While the exact number of

defects created by the 1MeV protons will slightly be more than the 1.8 MeV protons, the difference is very small. So, we assume that the amount of displacement damage and defect density using 1 MeV and 1.8 MeV protons is comparable for equal fluences.

Proton implantation at low energies causes a reduction in the majority carrier density in GaN and AlGaN [53,54], via the formation of shallow and deep level traps. The introduction of these traps in the material causes a corresponding reduction in the conductivity, mobility and minority carrier lifetime. The phenomenon of compensating majority carriers by shallow or deep level traps is also known as carrier removal [55]. In p-type GaN, the defects are formed at 0.9 eV and 0.3 eV from the valence band edge. These defects are donor-like and make the material less p-type. On the other hand, defects in the n-type AlGaN layer are predominantly formed at 3.7 eV and 2.3 eV from the conduction band edge [54]. These defects are acceptor-like and thus make the material less n-type as the number of defects increases [54].

The position of the Fermi level with respect to these trap levels decides their charged state. The 2DEG in AlGaN/GaN heterostructures is charge sensitive and the placement of defects affects the charge balance in the structure and thus the operation of the HEMT itself. Studies with low energy electron nanoscale (LEEN) spectroscopy have shown that the presence of deep level defects in the AlGaN layer can reduce the 2DEG confinement through a reduction in band gap [56]. The next section of this paper will discuss the effect of defects at various energies and spatial locations within the different regions of the device. This will allow us to identify the mechanisms responsible for displacement damage-induced change in DC *I-V* characteristics in these devices.

5.3 2DEG density and defect location and energy

The 2DEG density in AlGaN/AlN/GaN HEMT devices is a strong function of the polarization charge at the AlN/AlGaN and the AlGaN/AlN interface. In this section we look at the effects of defects at various locations and energies within the structure. We have assumed that the polarization charge at the interfaces in the device does not change due to radiation damage. This is a valid assumption because at the fluences reported in this study the composition of the materials does not change substantially [57].

In the simulations, defects were introduced into all three layers of the GaN HEMT structure. For the purpose of illustration, the defect density in these simulations corresponds to a fluence of 10^{14} protons/cm^2. The energy levels for the defects are the same as in the proton implantation studies mentioned in the previous section [53, 54]. A total defect density of 1×10^{17} cm^{-3} was introduced into the AlGaN; the energy of the traps was 2.3 eV from the conduction band minimum [7]. The defect density in the GaN estimated from SRIM simulations was 5×10^{16} cm^{-3}; these defects were assumed to be donor-like at 0.9 eV from the valence band maximum. There are not many studies looking at proton-induced defect energy levels in AlN. For the purposes of this study we assumed defects at midgap (3.1 eV). The density of AlN is the similar to AlGaN; this makes it likely that the defects due to protons are also deep.

The defect density estimated by SRIM in the AlN layer at different fluences is the same as that in the AlGaN layer. The defect density at a proton fluence of 10^{14} cm^{-2} in the AlN layer is 2×10^{17} cm^{-3}. Our simulations show that only the acceptor-like defects in the AlGaN layer have an effect on the 2DEG density. The donor-like defects introduced in

the GaN layer do not have any impact on the 2DEG density. This is consistent with previous LEEN studies looking at the impact of deep level traps in AlGaN [56].

Figure 31 is a plot of the simulated 2DEG density in the HEMT at a gate voltage *(V_G)* of -3 V, $V_D = 0$ V, $V_S = 0$ V. The 2DEG density is plotted as a function of the defect type and energy; the energies are defined with respect to the conduction band minimum. The plot corresponds to a defect density of 1×10^{18} cm^{-3} in the AlGaN and a defect density of 5×10^{17} cm^{-3} in the GaN. As the acceptor-like defects get farther away from the conduction band, the change in 2DEG density is more pronounced. The donor-like defects in the AlGaN have no substantial effect on the 2DEG because the bias point at $V_G = -3$ V ensures that the Fermi level is above the defect energy level in the AlGaN. This leaves the acceptor-like defects negatively charged, which causes the formation of net negative space charge in the bulk AlGaN region of the HEMT. This negative space charge causes band bending in the device and thus reduces the 2DEG density. This effect will be discussed in detail below. Figure 32 is a plot of the 2DEG density at different gate voltages extracted from the simulations. The 2DEG pinches off at -6 V. Figures 31 and 32 allow a comparison between changing the gate voltage in the device with that of charged defects.

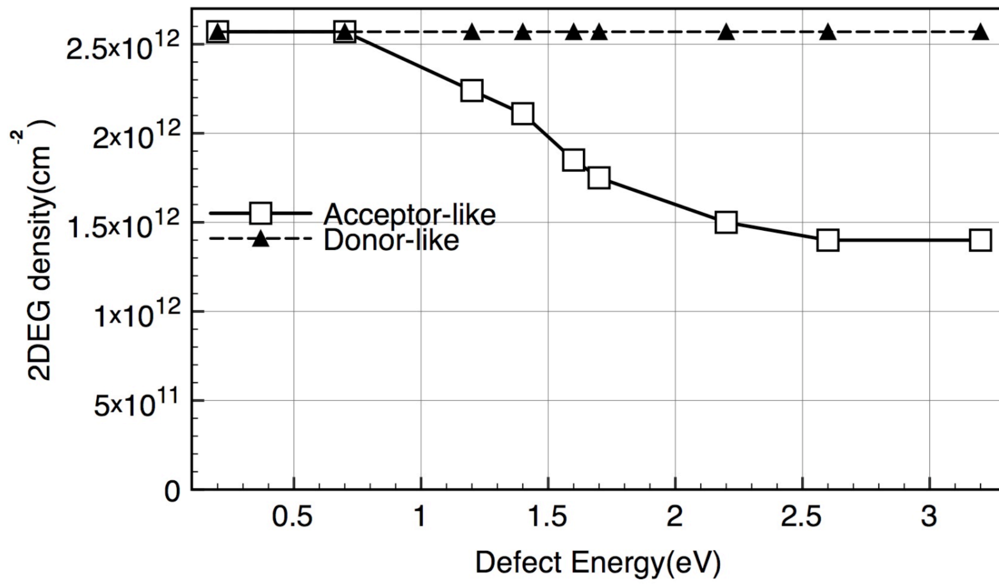


Fig. 31.2DEG density as a function of defect energy and defect type in AlGaN at V_G = -3 V.

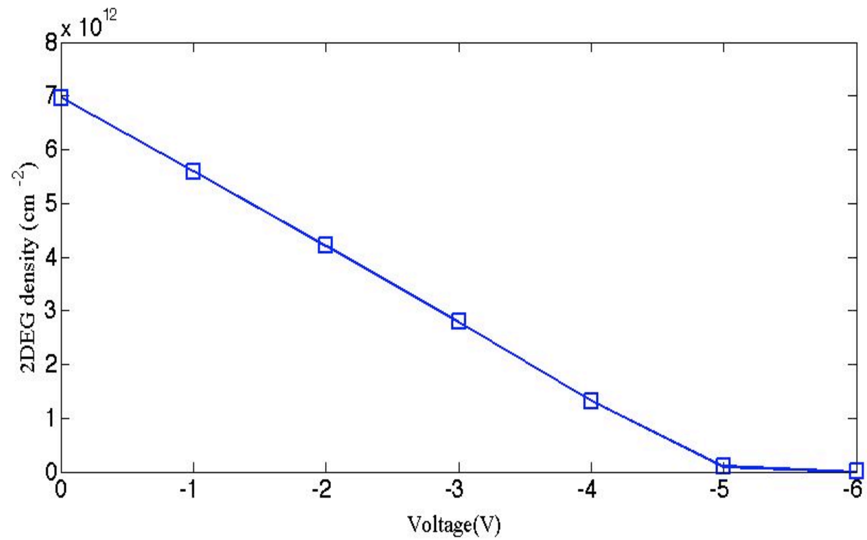


Fig. 32. 2DEG density as a function of gate voltage.

5.4 HEMT performance and 2DEG density

The drain current in HEMTs is very closely related to the 2DEG density. Figure 33 plots the 2DEG density and I_{Dsat} obtained from simulation vs. fluence, illustrating the close correspondence between the 2DEG density and I_{Dsat}. A reduction in 2DEG density

corresponds to a direct reduction in I_{Dsat}. To obtain the data in figure 33, defects were placed in the various layers of the HEMT device. The defect type, densities, and energies used at various fluences were the same as described in the previous sections of this chapter. The I_{Dsat} values were extracted from the *I-V* characteristics.

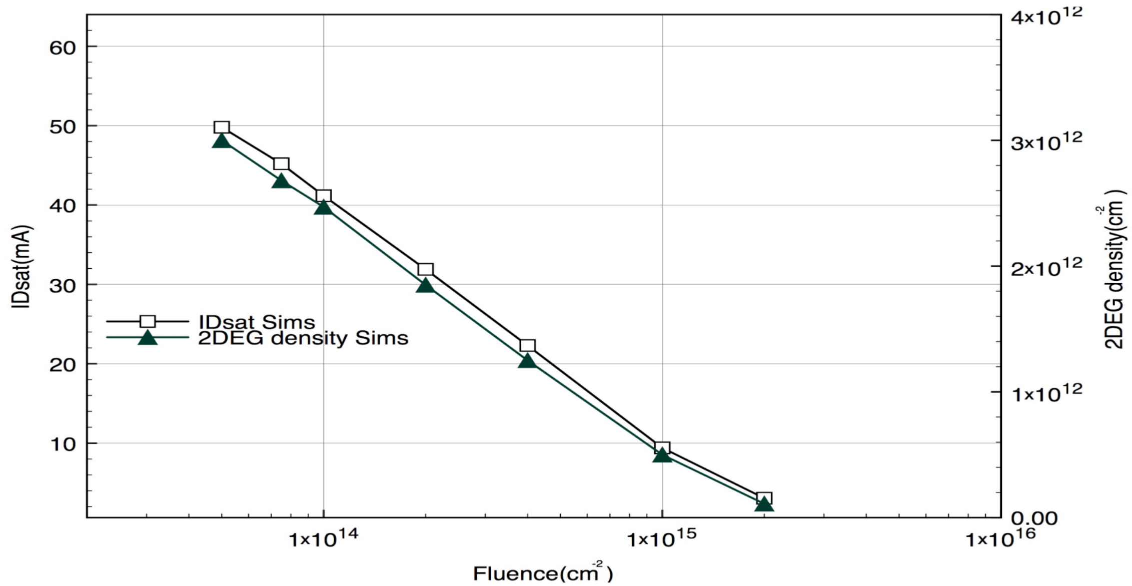


Fig. 33. I_{Dsat} and 2DEG density at V_G = -3 V as a function of fluence.

5.5 Discussion

5.5.1 Band bending due to charged defects

Previous studies of radiation damage in GaN HEMTs have attributed the reduction in 2DEG density to carrier removal in the AlGaN and GaN [50,44]. Although the analytical models used in these studies include the effect of carrier removal on the 2DEG density, they do so by combining all the effects of radiation damage in device-level parameters like threshold voltage. The analytical model used in these studies is given by

$$n_s = \frac{\varepsilon}{qd}\left(V_{GS} - \left(\phi_b - \frac{qN_D d_d^{\ 2}}{\varepsilon} - \Delta E_C\right)\right) \tag{25}$$

$$V_{TH} = \phi_b - \frac{qN_D d_d^{\ 2}}{\varepsilon} - \Delta E_C \tag{26}$$

where n_s is the 2DEG density in the channel, ϕ_b is the Schottky barrier, ΔE_C is the difference in the conduction band between the AlN layer and the GaN buffer layer, N_D is the doping in the AlGaN layer, and d_d is the thickness of the AlGaN layer. The change in n_s is determined from the change in V_{TH}. V_{TH} is obtained directly from the experimentally measured I_D-V_G characteristics of the device. This model underestimates the 2DEG density by approximately 33% as compared with experimental Hall measurement 2DEG density [50]. Plugging in the quantities described in equations 25 and 26, the model estimates the 2DEG density as 10^{13} cm^{-2}, whereas the Hall measurement gives a 2DEG density of 1.5×10^{13} cm^{-2}. Using these models one cannot directly relate defect density to the change in 2DEG density. Moreover, the impact of polarization charge on the 2DEG density in these models is not very clear.

The self-consistent model discussed in Chapter 2 allows us to estimate the 2DEG density in AlGaN/AlN/GaN devices much more accurately by modeling polarization charge. The error between the model and the measured experimental 2DEG density values is less than 0.5%. The 2DEG density and other quantities from the model were extracted by getting qualitative agreement between simulation and experimentally measured I_D-V_D data. Previous studies on the same devices have shown the 2DEG density with 10 Å AlN layers to be ~ 10^{13} cm^{-2} [29]; the self-consistent model on that structure gives us a 2DEG density of ~ 1.4×10^{13} cm^{-2}. Also, the self-consistent model that we have used allows us to relate defect density directly to the 2DEG density.

The mechanism behind the proton irradiation-induced change in DC *I-V* characteristics of the 2DEG may be summarized as follows. Adding acceptor-like charged defects in the AlGaN layer changes the space charge in the device. Since these defects are deep, they are below the Fermi level and thus negatively charged. This causes band bending in the HEMT structure and the bands move up with respect to the Fermi level, thus reducing the 2DEG density.

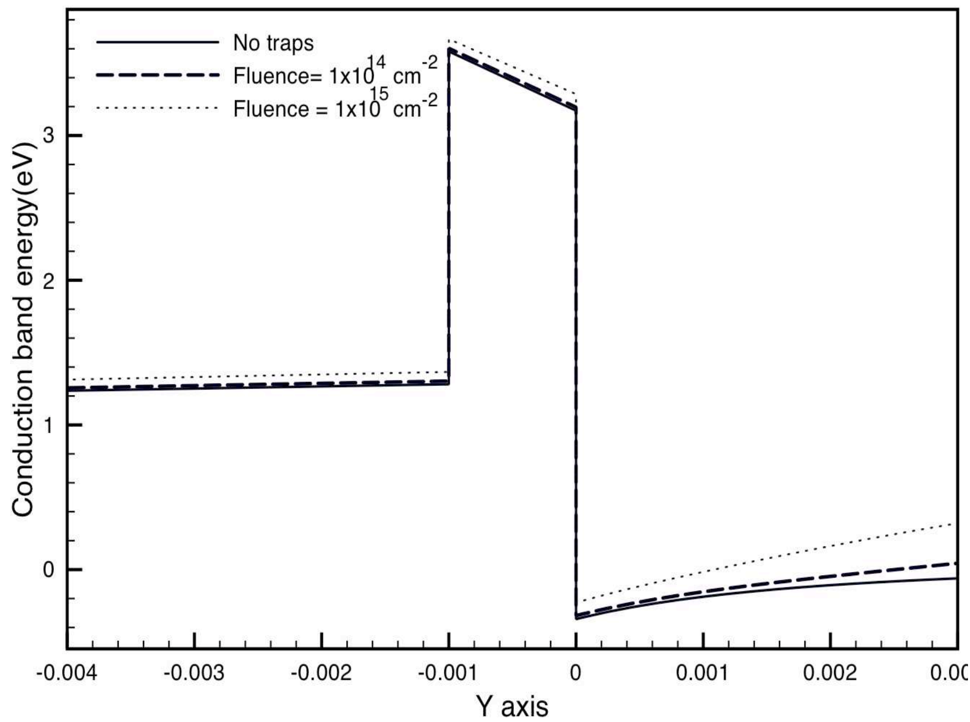


Fig. 34. Band bending in the HEMT structure due to defects in the HEMT structure layer.

This change in 2DEG density reduces the amount of drain current in the device. Figure 34 shows the effect of acceptor-like deep defects in the HEMT heterostructure on the band structure for fluences of 1×10^{14} and 1×10^{15} cm^{-2}, corresponding to defect densities of 2×10^{17} cm^{-3} and 2×10^{18} cm^{-3} in the AlGaN and AlN layers. The defects were assumed to be acceptor-like and the energy levels of the defects were the same as

listed in the previous section on defect energy and location. The defects in the p-type GaN channel were donor-like and the defect densities were 5×10^{16} cm^{-3} and 1×10^{17} cm^{-3} at the two fluences considered here. With increasing acceptor-like defect density in the AlGaN, the energy bands move up with respect to the Fermi level (the Fermi level corresponds to 0 eV on the *y*-axis). This band bending in turn decreases the 2DEG density.

5.5.2 Band bending vs. mobility degradation induced changes in DC I-V characteristics

Previous studies have examined the combined effects of carrier removal and mobility degradation due to proton irradiation in GaAs devices. This is because the device degradation is mainly due to displacement damage in the doped layers in these devices [51]. The majority of free carriers in these devices come from the doped layers [51]. In the devices considered here, the majority of carriers in the 2DEG are due to polarization charge, and the proton irradiation-induced changes in DC *I-V* characteristics are due to band bending as a result of charged acceptor-like defects in the AlGaN layer. By including the polarization charge in the self-consistent model, we can understand the impact of radiation-induced defects on the space charge and ultimately on the 2DEG. The effect described here is different from carrier removal. Carrier removal directly changes the doping of a material and removes free carriers. The phenomenon described here changes the 2DEG density indirectly by bending the bands. Also, the inclusion of polarization charge is necessary to accurately model the 2DEG density in AlGaN/AlN/GaN devices.

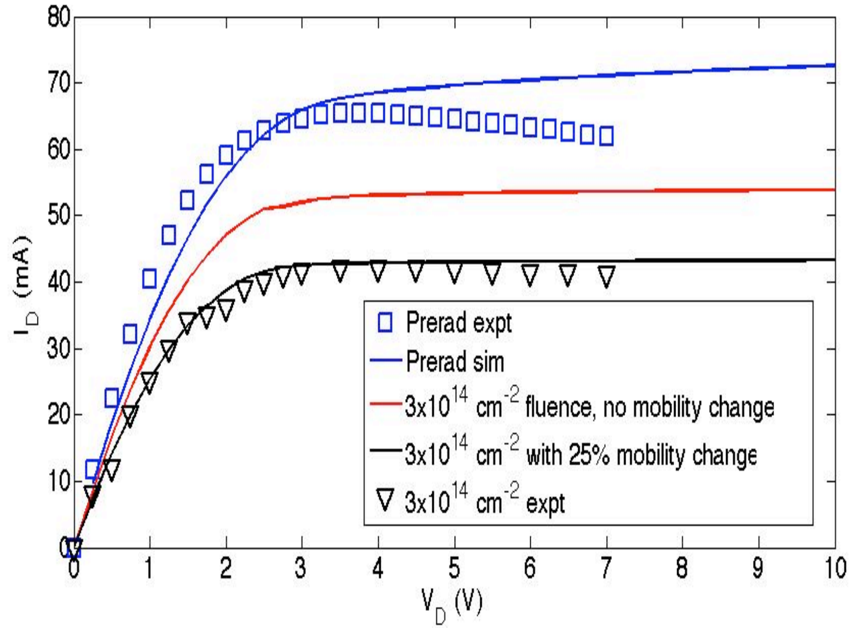


Fig. 35. I_D-V_D comparison between experiment and simulation.

Figure 35 compares the I_D-V_D characteristics obtained from TCAD and the experimental data for a fluence of 3 × 10^{14} protons/cm^2. The different curves were obtained by simulating only the electrostatic effect of defects, keeping the mobility the same as the pre-irradiation case. The mobility change was subsequently added to the simulations to match the experimental results after an exposure of 3 × 10^{14} protons/cm^2. This figure shows that band bending alone cannot account for the proton irradiation-induced degradation in the I_D-V_D curves. There is a component of mobility degradation that one has to add in the simulations to explain the degradation in the I_D-V_D characteristics.

At 1 × 10^{14} cm^{-2} the amount of mobility degradation is ~20%, and at 3 × 10^{14} cm^{-2} it is ~25%. These values are consistent with those reported in previous studies [19]. The

2DEG region is very thin, so there are not many defects in the 2DEG region itself. These results suggest that Coulomb-scattering from defects outside the 2DEG region causes mobility degradation [19]. Coulomb scattering and defect scattering have been shown to reduce mobility in these devices. Previous work using Hall effect measurements on similar devices indicated the mobility degradation at a fluence of 3×10^{14} cm^{-2} is approximately 25% [50], which translates directly into a reduction in the output current.

CHAPTER 6

QUANTIFYING THE RELATIONSHIP BETWEEN TRAP AND SELF-HEATING INDUCED MOBILITY DEGRADATION

This chapter discusses and quantifies the relationship between trap and self-heating induced degradation in mobility. This chapter quantifies this interplay between bulk defects, self-heating and mobility degradation in AlGaN/AlN/GaN HEMTs. It shows that at more negative gate biases, corresponding to lower lattice temperatures, mobility degradation due to bulk defects in the device dominates. At less negative gate biases, self-heating induced mobility degradation dominates.

6.1 Introduction

Self-heating effects are a serious concern in GaN HEMTs because of their large power densities [9, 58-60]. The maximum power densities in GaN HEMTs are ten times those that can be obtained in silicon and GaAs devices; this is attributed to a larger current density for the same device area and higher breakdown voltage [59]. The elevated temperatures near the 2DEG degrade the drain current in the device. The reduction in drain current at higher drain biases has been attributed to degradation in mobility due to Joule heating [23] .

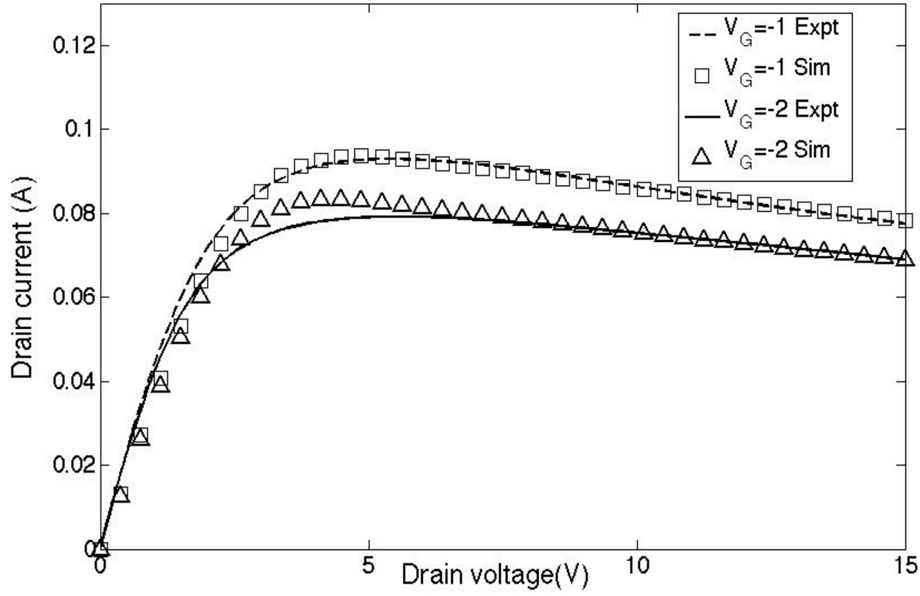


Fig. 36. I_D-V_D characteristics at two different gate voltages.

Figure 36 shows results comparing simulations and experimental data for a typical HEMT structure; self-heating is included in the simulation results. The 2DEG Hall mobility at room temperature was 1300 cm^2/(V-s); this value was used in the simulations as the room temperature mobility. The v_{sat} value in the 2DEG region at room temperature was fixed at 1.1 × 10^7 cm/s, consistent with previous studies [46]. The coupling between room temperature mobility and lattice temperature used in the simulations is described below. Equations 1 and 2 for mobility and saturation velocity, respectively, are the models used in the Sdevice simulator [45]. These models include the temperature dependences of the mobility and saturation velocity [61].

$$\mu(T) = \mu_0 \left(\frac{T}{T_0} \right)^{-3} \tag{27}$$

Here μ_0 is the room temperature mobility and T_0 is 298 K. The coupling relation between

v_{sat} and the lattice temperature is:.

$$v_{sat}(T) = A_{vsat} - B_{vsat}\left(\frac{T}{T_0}\right) \tag{28}$$

Here A_{vsat} is 1.2 × 10^7 cm/s and B_{vsat} is 0.5 × 10^7 cm/s. These values are obtained from previously reported studies on GaN [62]. Previous studies have also shown the dependence of saturation velocity on impurity scattering [62, 63]. These studies suggest that impurity scattering degradation can reduce the saturation velocity by as much as 50% at higher doping concentrations. This degradation in the saturation velocity is attributed to the increased polar and optical phonon scattering [62, 63]. Section 6.2 describes the model used to describe the effect of increased impurity scattering at higher fluences.

Figure 37 shows the experimentally observed impact of proton irradiation on the drain current (I_D) vs. drain voltage (V_D) characteristics. Results are shown at V_G = -1 and -2 V. These results are quite comparable to the damage reported in previous studies on AlGaN/AlN/GaN HEMTs [44, 50]. The smallest fluence at which significant changes in the I_D-V_D characteristics were observed was 3 × 10^{13} cm^{-2}. The figure shows the pre-irradiation *I-V* characteristics, as well as those at fluences of 6 × 10^{13}, 2 × 10^{14}, and 5 × 10^{14} cm^{-2}. As the particle fluence increases, the I_D-V_D characteristics degrade.

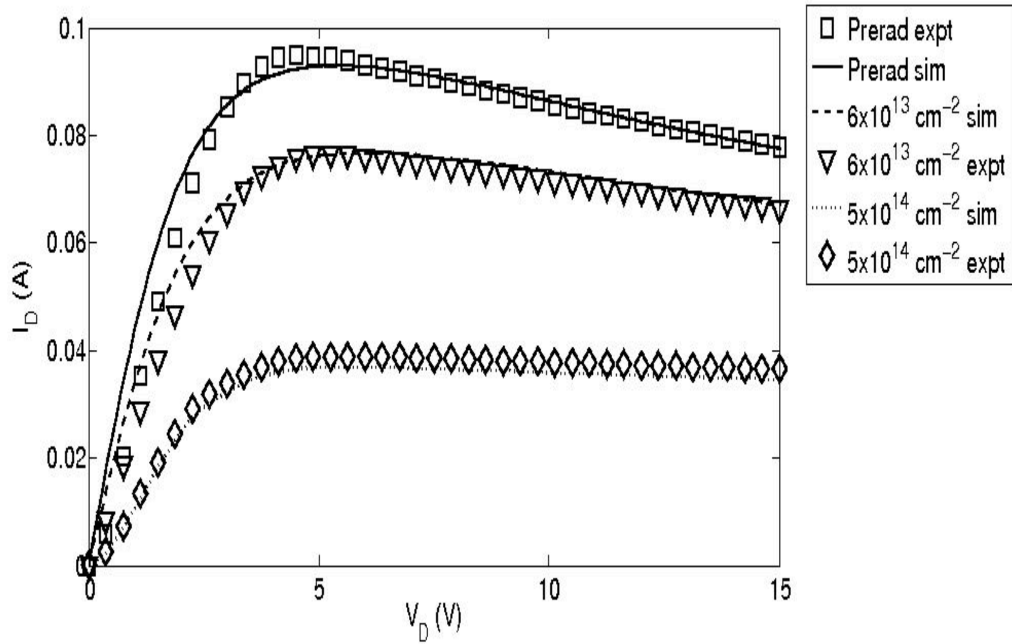


Fig. 37. Drain current vs. drain voltage data for irradiated AlGaN/AlN/GaN HEMT devices at different proton fluences.

Figure 37 also compares the measured I_D-V_D characteristics at different fluences with simulation data. The symbols represent simulation data and the solid lines represent experiment data. The I_D-V_D characteristics degrade with fluence due to band bending and mobility degradation [3]. The I_D-V_D characteristics also show degradation at higher drain biases due to self-heating. Model calibration was performed by including traps in the structure and by adjusting the mobility and saturation velocity. The saturation currents of the experiment and simulation curves were matched. Mobility and saturation velocity degrade with fluence and lattice temperature [23].

6.2 Degradation model & analysis

The self-heating model was presented in Section 4.2. This section applies this

model to analyze self-heating effects in GaN-based HEMTs.

6.2.1 Analysis

Figure 38 shows the simulated lattice temperature cross section of the HEMT at V_G = -1 V and V_D = 9 V at the drain side gate-edge. There is a hot spot near the drain-side gate edge. The red lines in figures 38 and 39 indicate the vertical cut-line used for figures 40 and 41. The "x" in figure 38 is a point near the hot spot that is used in the next section to discuss the mobility degradation near the hot spot. The temperature goes down by about 30 K in the GaN region. The experimentally measured 2DEG electron mobility at 298 K in these devices is 1200 cm^2/V-s and the mobility in the GaN layer is 1000 cm^2/V-s [64]. Figures 38-40 show the relationship between lattice temperature and mobility near the gate-drain access region. Each of these figures is discussed individually below.

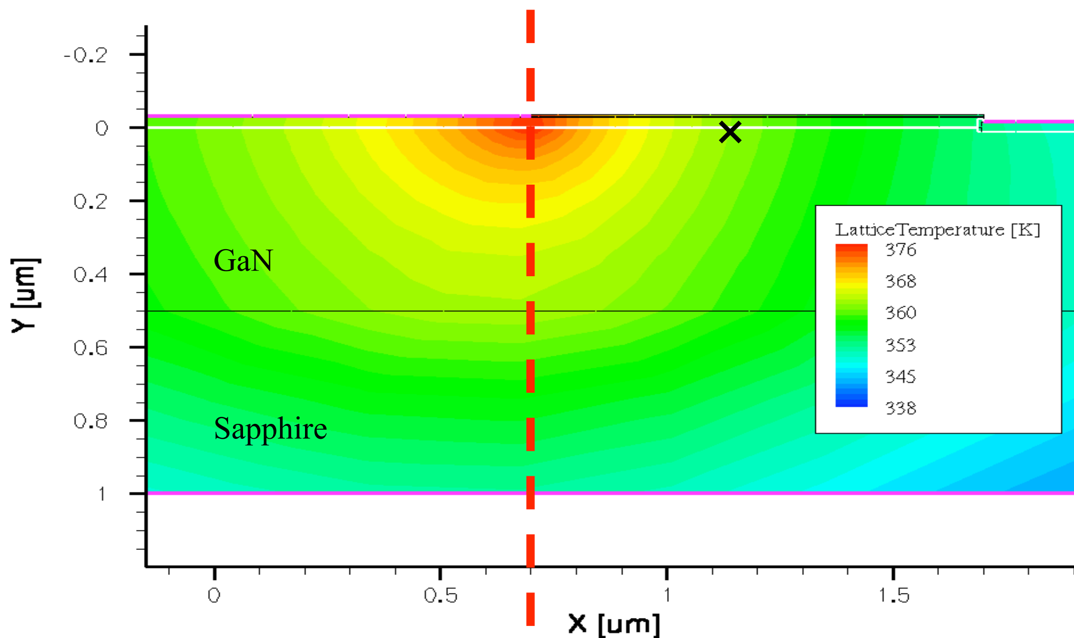


Fig. 38. Lattice temperature near the gate-drain access region V_G= -1 V, V_D= 9 V.

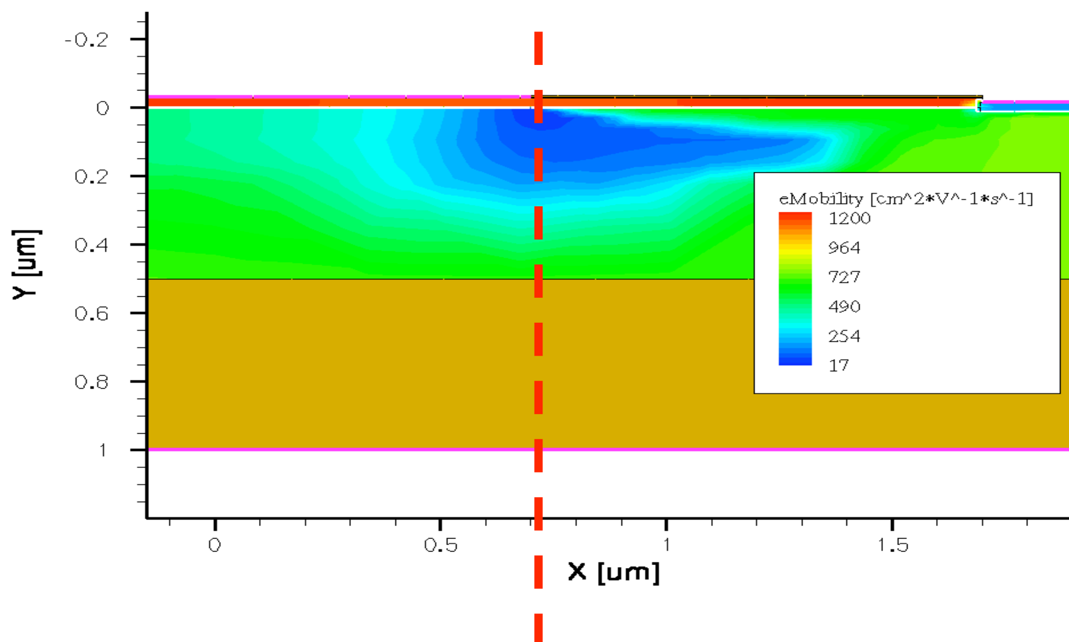


Fig. 39. Electron mobility near the gate-drain access region, V_G= -1 V, V_D= 9 V.

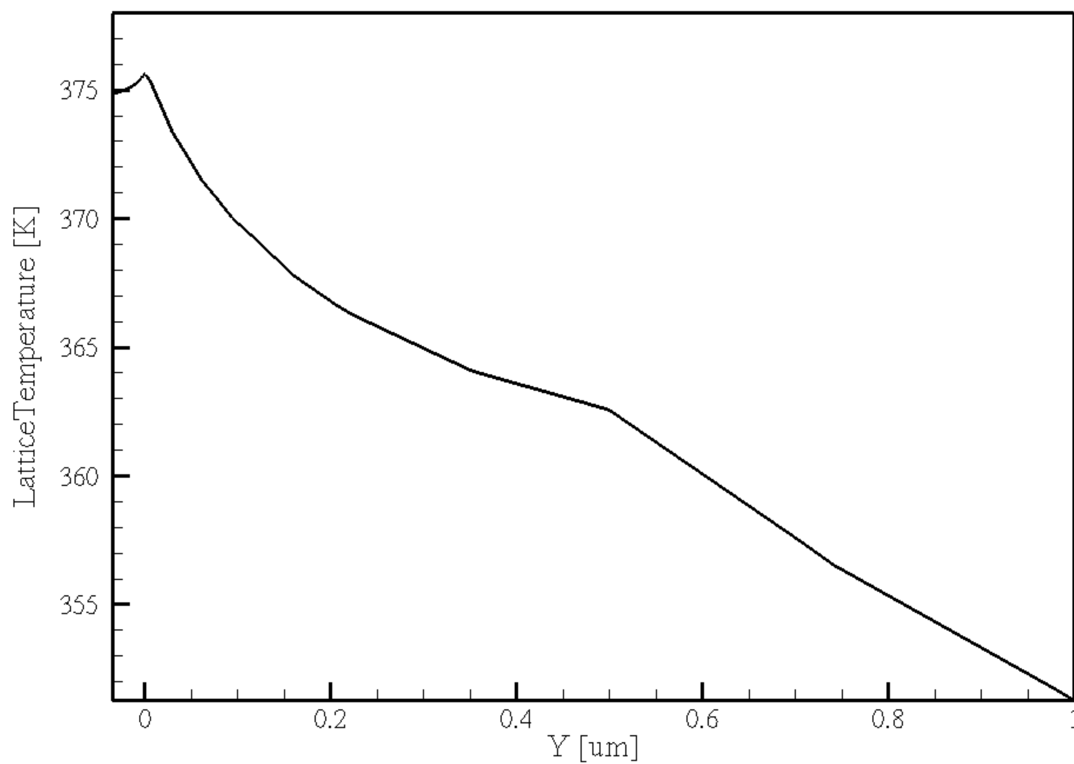


Fig .40. Plot of lattice temperature along a vertical cut line near the hot spot. The hot spot is near the gate-drain access region, V_G= -1 V, V_D= 9 V.

Figures 38-40 show that at large drain biases, self-heating causes degradation of the mobility. The mobility degrades rapidly around the hot spot. This degradation in the mobility causes a reduction in the drain current. Figure 41 is a plot along a vertical cut line through the hot spot. The temperature around the hot spot reaches a maximum of 375 K. In figure 38, we can see a reduction in the self-heating as we move away from the hot spot. Figure 41 is a plot comparing the mobility along the 2DEG at the bias described above and V_G = -1 V, V_D = 15 V and at zero bias. The plot illustrates the effect of self-heating on the mobility. This dramatic drop in mobility along the cut-line can be attributed to the high electric field near the hot spot in the devices studied [23].

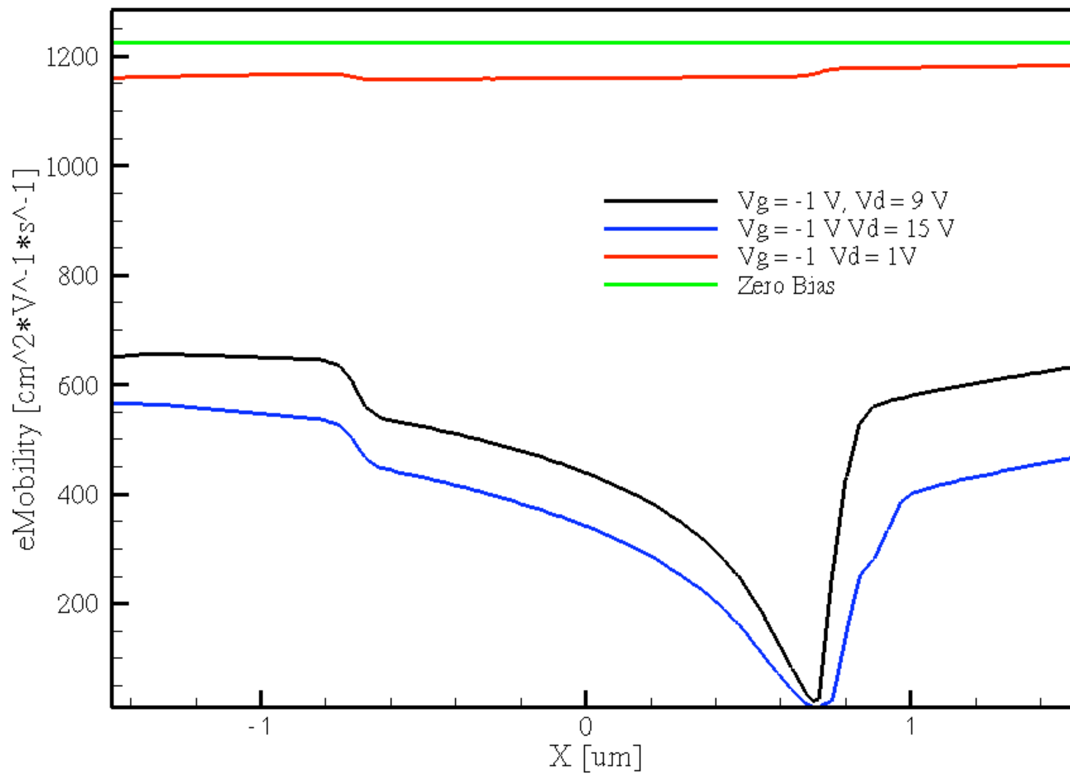


Fig .41. Electron mobility along the 2DEG at 4 different biases.

Mobility and saturation velocity also degrade due to the presence of bulk traps. The low energy proton irradiation experiment allows the creation of defects in the structure. Comparing the experimental data with our simulations suggests that the hot spot is created due to the high electric fields near the drain-gate access region at saturation. In summary, the high electric fields cause a rapid degradation in mobility [23]. This in turn increases the resistivity in the 2DEG. This increased resistivity causes increased self-heating. The mobility near the hot spot further degrades due to the increased self-heating. As an example, the mobility degrades to about 20 $cm^2/V.s$ near the hot spot.

6.3 Mobility and saturation velocity degradation

In Chapter 5 the effect of band bending due to charged defects in AlGaN/AlN/GaN devices was quantified [3]. In addition to the band bending due to the charged defects in the structure, we need to account for the mobility and v_{sat} degradation due to the defects introduced by the proton irradiation. Equations 29 and 30 give the relationship between fluence, mobility and v_{sat} degradation and temperature.

$$\mu_{\Phi}(T) = \mu_{\Phi 0}\left(\frac{T}{T_0}\right)^{-3} \tag{29}$$

$$v_{sat,\Phi}(T) = A_{vsat,\Phi} - B_{vsat}\left(\frac{T}{T_0}\right) \tag{30}$$

6.3.1 Saturation velocity degradation

This section uses the simulations and experiments to understand the degradation in saturation velocity due to temperature and defects. The model used for saturation

velocity above in equation 30 includes the degradation due to defects and temperature. Figure 42 compares the I_D-V_D characteristics obtained from TCAD and the experimental data for the pre-irradiation and the 5×10^{14} cm^{-2} fluence case. The pre-irradiation and the "5×10^{14} cm^{-2} without v_{sat} degradation" simulation curves were obtained by keeping v_{sat} the same for both cases. Band bending and mobility degradation models alone cannot account for the degradation of the I_D-V_D curves. There is a component of v_{sat} degradation with increasing defect density and temperature that one has to add as well. The v_{sat} change was subsequently added to the simulations to match the experimental 5×10^{14} cm^{-2} case.

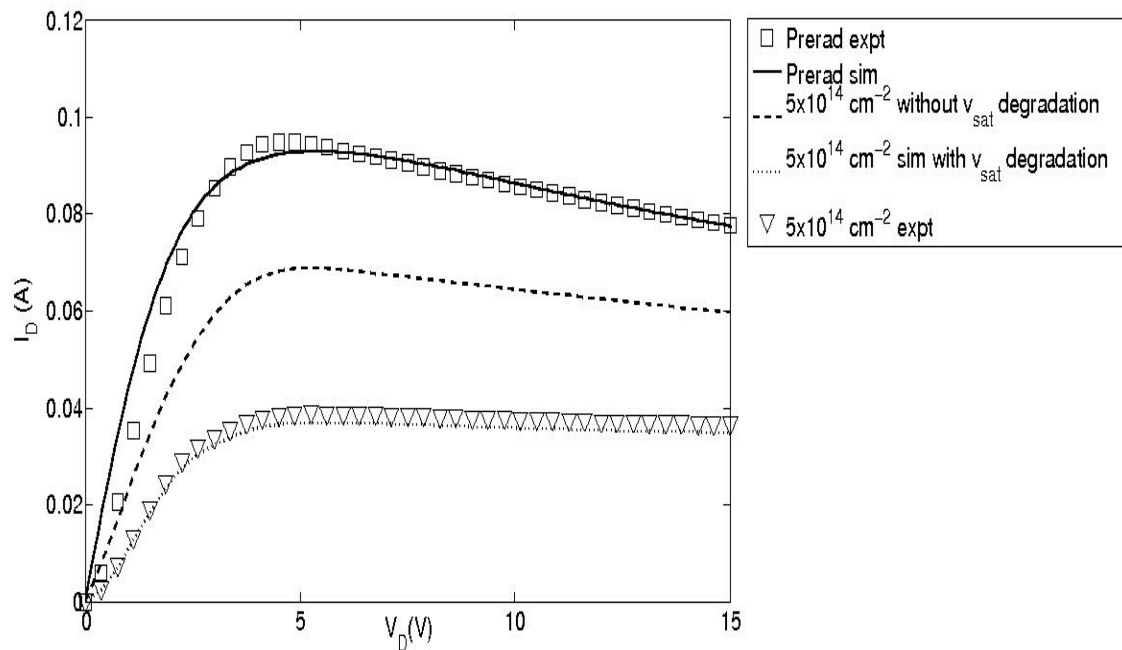


Fig. 42. I_D-V_D comparison between experiment and simulation, V_G = -1 V.

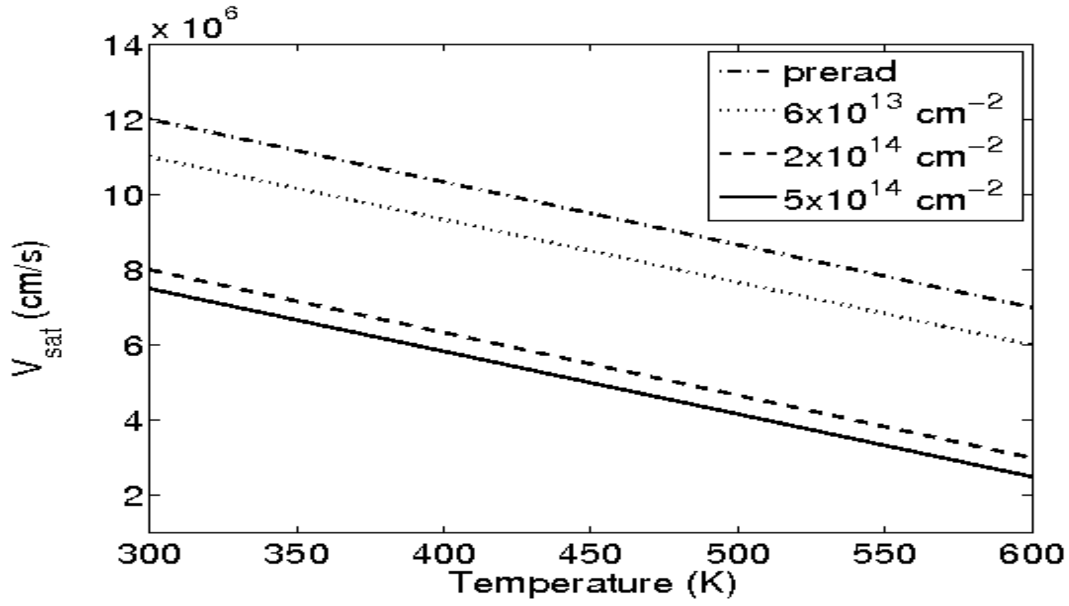


Fig. 43. Degradation of saturation velocity with temperature.

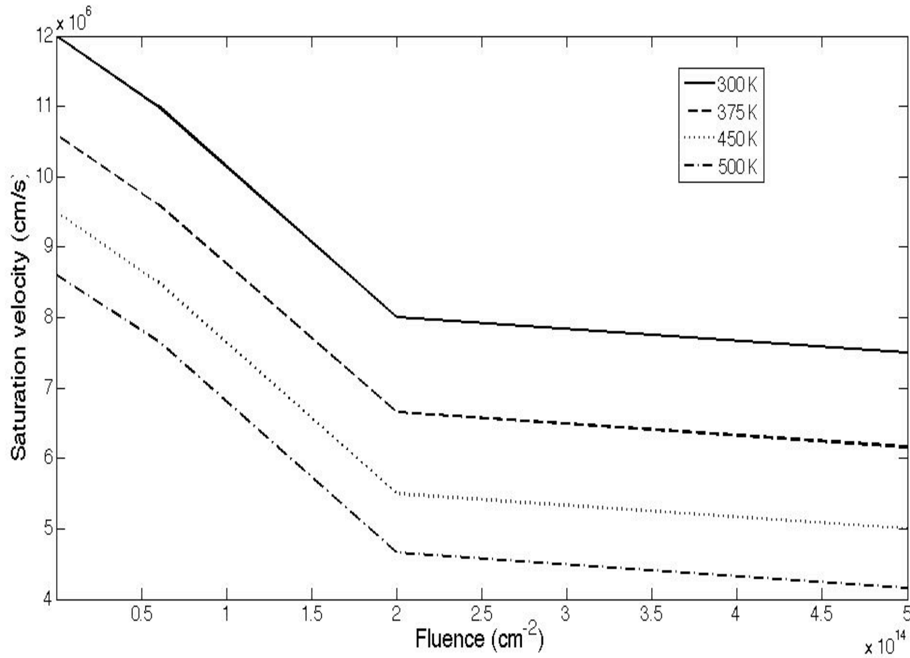


Fig. 44. Saturation velocity as a function of fluence.

Figure 43 is a plot of the saturation velocity as a function of temperature at different fluences. Figure 44 is a plot of the saturation velocity as a function of fluence at four different temperatures. Figures 43-44 were obtained from equation 30 by plotting $A_{sat,\phi}$ at different fluences. At a fluence of 2×10^{14} cm^{-2} there is 33% degradation in

saturation velocity. Beyond 2 × 10^{14} cm^{-2}, the saturation velocity does not degrade as dramatically with fluence, which suggests that increasing defect density beyond a fluence of 2 × 10^{14} cm^{-2} does not greatly affect impurity scattering in the 2DEG. The degradation of saturation velocity with fluence and temperature has been reported previously and is attributed to increased defect and phonon scattering [65].

6.3.2 Mobility degradation

Figure 45 is a plot of the mobility along the 2DEG near the hot spot at different fluences. The degradation in mobility near the hot spot is comparable at different defect densities. The slight difference in the mobility at different fluences may be attributed to the different amounts of band bending and slightly different temperature distributions in the device at different defect densities [3, 23]. This suggests that self-heating induced degradation is the main cause of degradation near the hot spot. As we go farther away from the hot spot, mobility degradation due to defect scattering dominates.

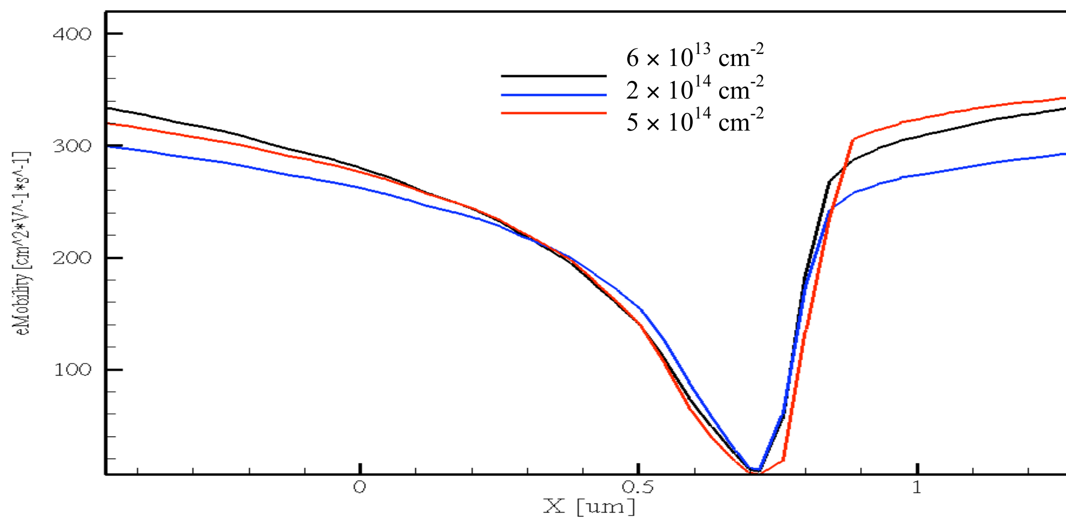


Fig. 45. Mobility along the 2DEG near the hot spot at the three different fluences, extracted from simulations.

Figure 46 is a plot of the temperature dependence of the mobility in the 2DEG, 0.5 μm from the middle of the hot spot, as a function of temperature. The exact location is pointed out by the symbol "×" in figure 38. The mobility at room temperature degrades by about 50% for the 5×10^{14} cm^{-2} fluence case, consistent with previous studies on GaN HEMTs [19, 51].

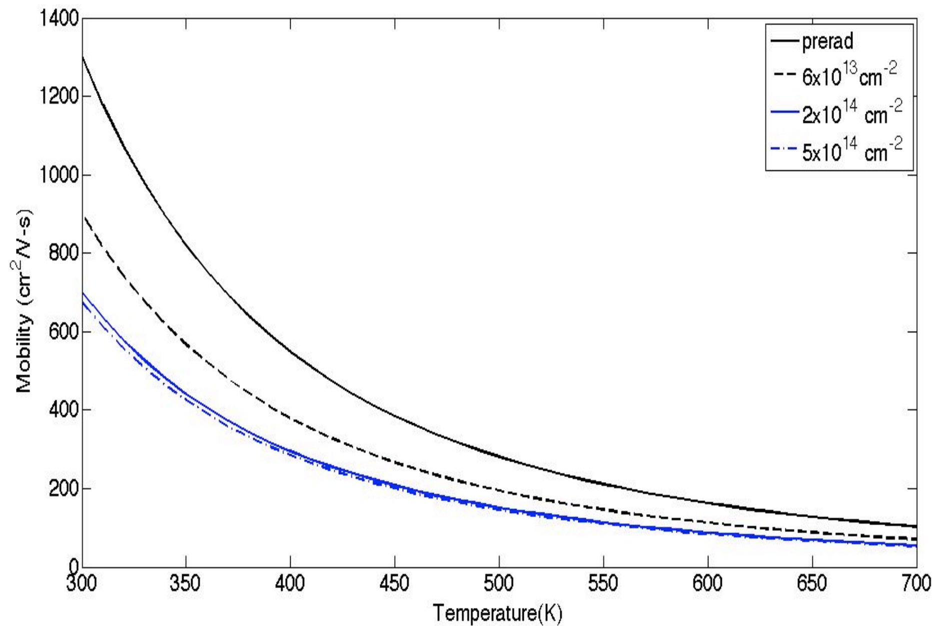


Fig. 46. Mobility vs. temperature at different fluences extracted from simulations.

The degradation in mobility with increasing fluence can be attributed to an increase in defect scattering in addition to the self-heating. Figure 47 compares the mobility at four different lattice temperatures. The difference in mobility is more pronounced at lower temperatures for the different fluences. Figures 46 and 47 compare the impact of bulk defects and self-heating induced mobility degradation. The 300 K case in figure 47 corresponds to a very small amount of self-heating in the device. This degradation in the mobility can be attributed to the impact of charged defects [3].

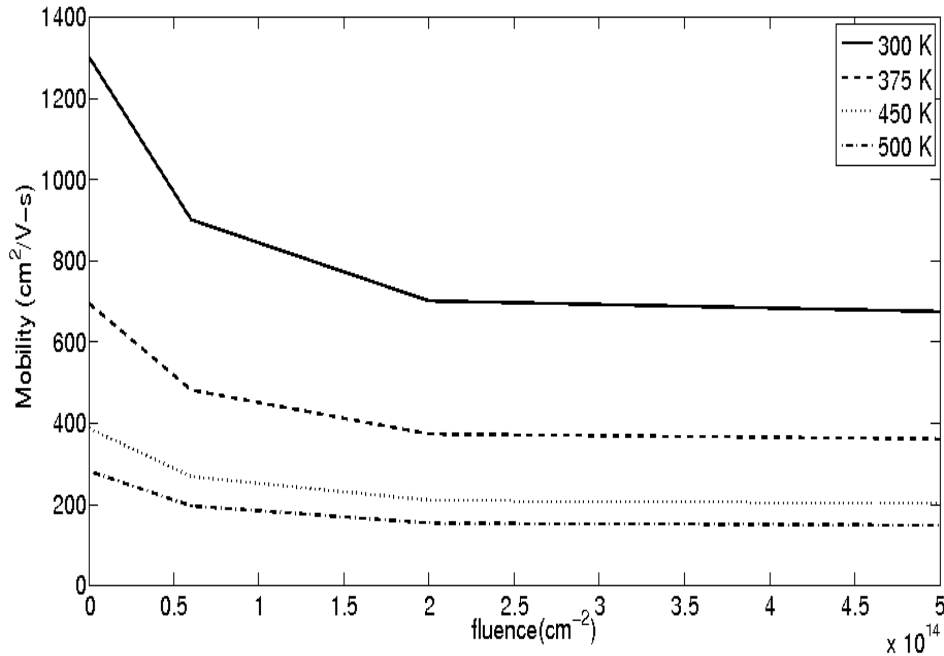


Fig. 47. Mobility vs. fluence at different lattice temperatures, extracted from simulations.

Higher temperatures correspond to higher current densities. At these higher temperatures, the mobility degrades due to self-heating in addition to the charged defect-induced degradation. As an example, by comparing the mobility at 450 K for the different fluences we can decouple the impact of self-heating on the mobility degradation. The no self-heating case corresponds to the 300 K curve in figure 46. The mobility at 5×10^{14} cm^{-2} is 675 cm^2/V-s. This is about 50% degradation in the experimentally measured mobility of the device. In the same figure the 450 K case corresponds to the self-heating case; at 5×10^{14} cm^{-2} fluence the mobility is 145 cm^2/V-s, corresponding to degradation of about 37% with respect to the original mobility in the device.

A different value of saturation velocity will change these results dramatically only if it is an order of magnitude different from the 1.2×10^7 cm/s pre-irradiation value used in this study [63]. This analysis can be extended to understand the interplay between

charged defect induced and self-heating induced mobility degradation in these devices at other lattice temperatures.

CHAPTER 7

THE IMPACT OF TRAPS ON GATE-LAG

7.1 Introduction

Gate-lag is defined as a recoverable reduction in the drain current transient response. Figure 48 is a schematic diagram that summarizes the phenomenon of gate-lag. The voltage pulse applied to the gate is sketched in the top part of the figure. The gate-lag response is sketched in the figure at the bottom. At 0 s the device is "on" and the drain current is at its maximum value I_{dmax}. The fall time of the voltage pulse is 50 ns and at 50 ns the device is off. The device remains off until 1.05 μs. The rise time of the pulse is 50 ns. At 1.1 μs the device is again switched back on. At 1.1 μs the drain current is not back to I_{dmax}; this phenomenon is termed as gate-lag. The simulations and experiments reported in this chapter use the voltage pulse described below.

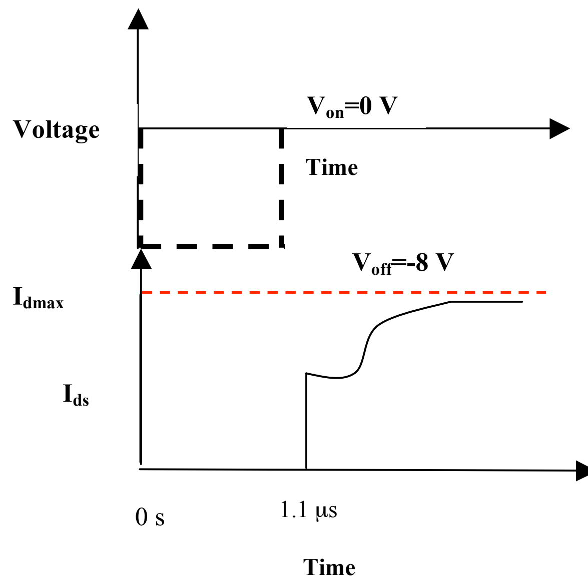


Fig.48. Schematic diagram of gate-lag in GaN HEMTs.

Gate-lag has been attributed to two different mechanisms: trapping in the bulk GaN region of the device and trapping on the AlGaN surface. Gate-lag due to surface traps originates from temporary variations in the concentration of donor traps ionized in the access regions next to the gate (source-gate, drain-gate) [66, 67]. Gate-lag due to bulk traps in the GaN buffer region occurs due to trapping of hot electrons generated in the 2DEG under the gate edges [5]. Figure 49 illustrates how surface states cause gate-lag. In region 1, a negative voltage below pinch off is applied to the gate. The green circles indicate the charged surface states and the red states indicate the 2DEG electrons. V_P indicates the voltage pulse. The channel under the gate is depleted and the device is off.

Due to the high electric field at the drain edge of the gate, there is a small amount of gate leakage between the gate and drain. This current charges up the surface states, forcing the surface potential to become negative. As a result, the channel under the part of the drain access region next to the gate is depleted too. In region 2, the gate bias is positive. The channel under the gate is able to respond quickly. The region under the access region is slow to react. The deep level traps and the low mobility of the electrons under this region are responsible for the slow turn on of the region. Thus, after the bias changes, the access region is still depleted and has a very low carrier concentration. This produces a highly resistive region and most of the drain bias drops across that region. This drop causes the drain current to remain low after changing the bias. The electrons are eventually released from the traps and the current increases correspondingly. If the pulse is long enough the drain current reaches a steady state.

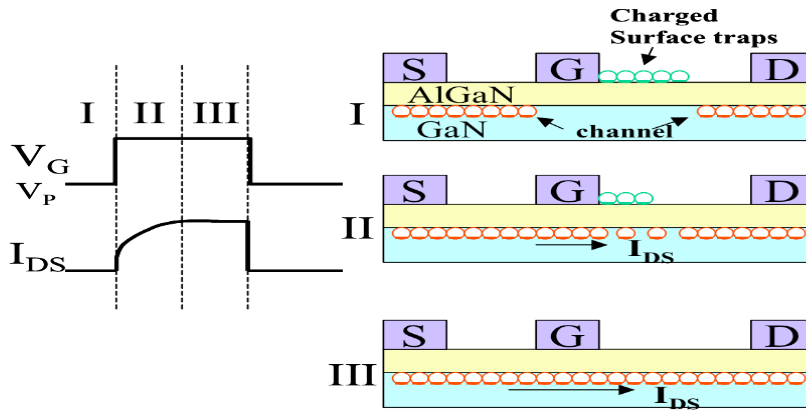


Fig. 49. Mechanism behind surface states causing dispersion in a GaN HEMT

Bulk traps may also cause gate-lag [5]. This is due to the capture of hot electrons from the channel in the buffer traps. This depletes the 2DEG and causes a reduction in the drain current. Figure 50 illustrates the time evolution of the hot electrons that are captured by bulk traps. The magnitude of the collapse depends on a variety of conditions like trap density and trap distribution, trap energy, and the presence or absence of a passivation layer on the surface.

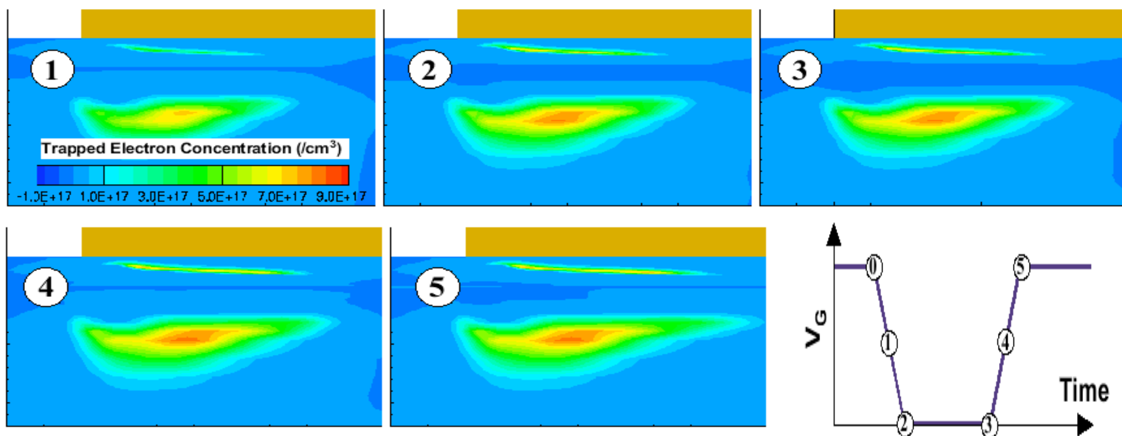


Fig. 50. Illustration of dispersion caused by bulk traps in a GaN HEMT.

In this thesis proton irradiation is used to induce bulk defects in the entire device in a controlled manner. Experimental data are then used with simulations to quantify and

analyze the relationship between proton irradiation induced bulk traps, surface traps, and gate-lag. The simulations are calibrated to the experiment results; the simulation results are used to understand the relationship between bulk traps and gate-lag. The sensitivity of gate-lag to parameters such as presence/absence of the passivation layer, energy of the surface traps, bulk trap density and bulk trap energy of bulk traps is analyzed in this study.

7.2 Sources of gate-lag in GaN HEMTs

The first part of this section discusses gate-lag due to bulk traps, the second part covers gate-lag due to surface traps. Finally, the measured and simulated gate-lag transients are compared. A comparison of simulation and experiment indicates that surface traps are the dominant cause of gate-lag in these devices.

7.2.1 Bulk trap mechanism

Previous studies on HFETs and MESFETs suggest that trapping of hot electrons in bulk traps near gate edges contributes to current collapse. These studies also suggest that current collapse is related to hot electrons spreading deeply into the bulk GaN region of the device [42, 47]. This has also been suggested to cause gate-lag [5].

GaN processing is not as sophisticated as silicon technology, and the bulk and surface trap densities are very large compared to silicon. Table 3 summarizes the possible impurity densities in the GaN material system. Different processing techniques lead to different impurity and defect densities. Photoionization spectra studies have suggested the presence of defects 1.8 and 2.85 eV below the conduction band in GaN [2]. The literature also suggests that the exact defect energies and densities of defects are still not

very well understood in the nitride material system. Most of the trap models are based on defects found in the GaAs system [2].

Nitride	Growth	H	C	O	Si
GaN	MOCVD	5×17	1×17	1×18	5×16
	(Source A)	4×18	7×16	2×18	2×17
		4×18	3×17	4×18	2×16
		2×19	2×17	5×18	1×16
		2×19	2×17	6×18	3×16
		7×19	2×19	5×19	···
		1.5×18	8×17	1×18	5×17
		1×18	7×17	1×18	7×17
		2×18	4×18	2.5×19	7×17
GaN	MOCVD	3×17	6×15	6×16	1.5×17
	(Source B)	5×17	3×16	2×17	1.5×17
		2×17	3×16	1×17	3×16
		3×18	2.5×17	9×17	5×17
		2×18	5×16	2×17	···
GaN	MOCVD	4×18	1.5×18	2×18	8×17
	(Source C)	2×19	3×17	5×18	2×17
GaN	MOCVD	<1×17	1×15	1×16	5×10^{15}
	(Source D)	2×19	3×17	5×16	···
GaN	MOCVD	1×17	3×15	2×16	2×10^{15}
	(Source E)				
GaN	MOCVD	2×17	3×16	1×17	3×16
	(Source F)	5×17	1×17	1×17	1×17
GaN	MBE	4×19	1.5×18	2×19	3×17
		9×18	1.2×18	2×18	5×17
GaN	LA	1×20	1×21	1×21	1×19
AlN	MOCVD	1–2×18	7×17	2×18	1.5×19
AlN	CVD	3×18	3×15	5×18	3×16
		4×20	1×18	5×19	1×19
AlN	CVD	1×19	5×18	8×18	···
AlN	CVD	4×18	1.5×18	8×18	8×17
AlGaN	MOCVD	2×19	2×18	5×18	3×18
AlGaN	MOCVD	7×18	8×18	2×19	7×17
AlInN	MOMBE	5×18	3×18	2×19	1×20
InN	MOMBE	8×20	7×19	1×21	2×19

Table 3. Impurity densities in III-Nitride system [35].

The defect density data in this section suggest that for MOCVD growth the maximum bulk impurity density in the device is on average around 10^{18} cm^{-3}. The defect density data in this section suggest that for MOCVD growth the maximum bulk impurity density in the device is on average around 10^{18} cm^{-3}. Simulations in this dissertation investigate the defect density and defect energy necessary to observe the experimentally measured gate-lag.

To simulate the spreading of electrons into the GaN region the hydrodynamic model in the simulator was used. The hydrodynamic models allow us to model the behavior of hot electrons in the device. Recent simulation studies have shown that different spatial distributions of traps have dramatically different effects on the amount of gate-lag in the device [5]. Gate-lag is also closely related to the trap energy and the presence or absence of the passivation layer. The first part of this section discusses the bulk trap mechanism in detail. The rest of the section discusses the sensitivity of the gate-lag to the various conditions described above.

7.2.1.1 Trap distribution and gate-lag

Previous studies suggest that the presence of a passivation layer causes large strain fields at the gate edges. This leads to much larger trap densities near the gate edges [68]. To understand the implication of trapping near the gate edges, a structure that incorporates larger trap densities near the gate edges was used in the simulation. For the purpose of illustration, the trap distribution was chosen to have a width of 0.1 μm, with a peak trap density of 3.5×10^{18} cm^{-3}. This was superimposed on a uniform trap density of 1.0×10^{18} cm^{-3}. The traps were acceptor-like with an energy 1 eV above midgap in each material (AlGaN and GaN), chosen to get qualitative agreement with experimental results and previous studies [5]. The choice of trap energy is discussed in greater detail in the next section.

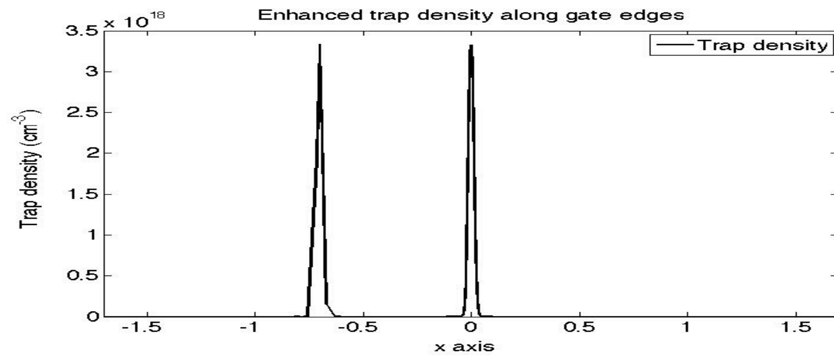


Fig. 51.Spatial trap distribution for the edge increased trapping case.

Figure 51 is a schematic diagram that shows the spatial trap distribution in the simulation structure. The first part of the figure shows an areal distribution of the traps in the device. The trap densities are highest at the gate-drain and gate-source edges. The second part of the figure is a cut line along the 2DEG. The gate-drain edge of the device has the maximum number of hot electrons generated. In this section all the figures describe the hot electron and trapped electron concentration near the gate-drain edge. Figure 52 indicates the device obtained from TCAD simulations and the electron temperatures. The gate-drain edge has the majority of the hot electrons in the structure.

Figure 53 compares the gate-lag for the uniform distribution case and the edge-increased trapping case. The edge increased trapping case is defined as an increased trap density near the drain and source edges next to the gate. The trap density in the uniform case was 1.1×10^{18} cm^{-3}; this density gives the same average trap density in the device as the edge-increased trapping case. The simulations were constructed to include the effects of a passivation nitride layer on the access regions by assuming that there were no surface traps on the access regions and by placing the high dielectric constant silicon nitride material over the access regions in the simulation deck. Figure 53 has been normalized to the maximum DC current expected from the DC I_D-V_D characteristics. The edge

increased trapping case corresponds to ~ 30% collapse, which is about three times the ~ 10% collapse for the uniform trap density case.

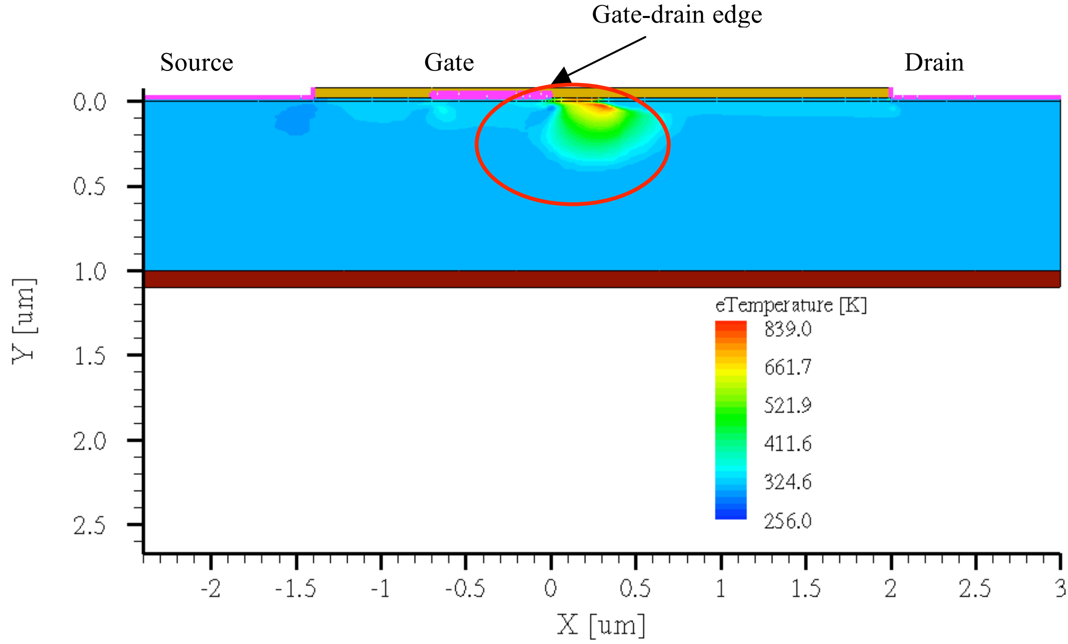


Fig. 52.Schematic diagram of the device from TCAD simulations; the gate-drain edge is indicated.

Figure 54 compares the hot electron spreading at 1.1 μs for the uniform and edge-increased trapping cases. 1.1 μs is the time at which the gate pulse is back at 0 V. This condition is indicated in figure 48. Figure 54 plots electron temperature as a function of position near the gate-drain edge. The gate-source edge is not shown in the figures because the number of hot electrons is very small when compared to the gate-drain edge. The 2DEG is in the horizontal direction along the 0 μm mark on the y-axis. The pink line in the figure indicates the gate-contact. The electron temperature is higher in the edge-increased trapping case.

Figure 55 compares the electron density at 1.1 μs for both cases. The edge-increased trapping case shows more electrons spilling out of the 2DEG region in the gate-

drain access region. As a consequence, the 2DEG density near the gate drain edge is depleted more in the edge-increased case. Figure 54 compares the hot electron spreading at 1.1 μs for the uniform and edge-increased trapping cases. 1.1 μs is the time at which the gate pulse is back at 0 V. This condition is indicated in figure 48. The figure plots electron temperature as a function of position near the gate-drain edge. The gate-source edge is not shown in the figures because the number of hot electrons is very small when compared to the gate-drain edge.

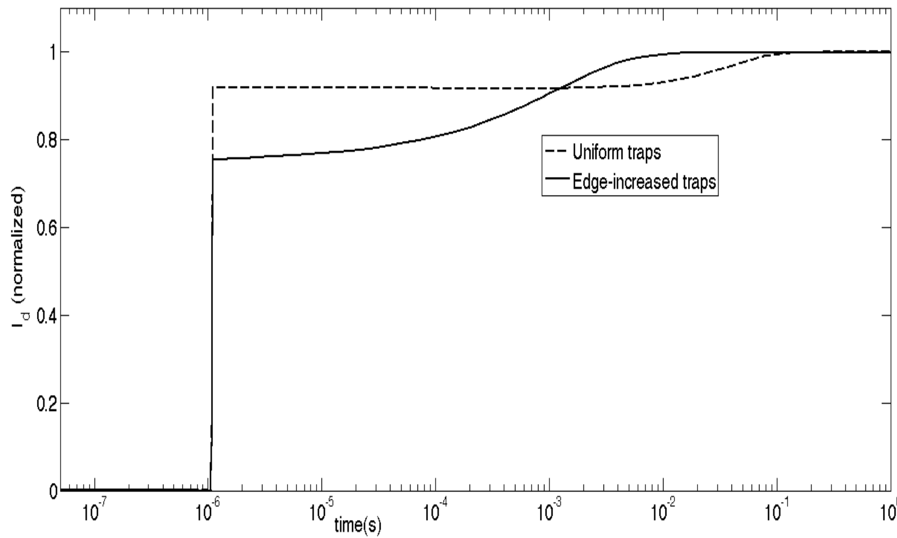


Fig. 53. Normalized drain current transients for edge-increased trap density and uniform trap density cases.

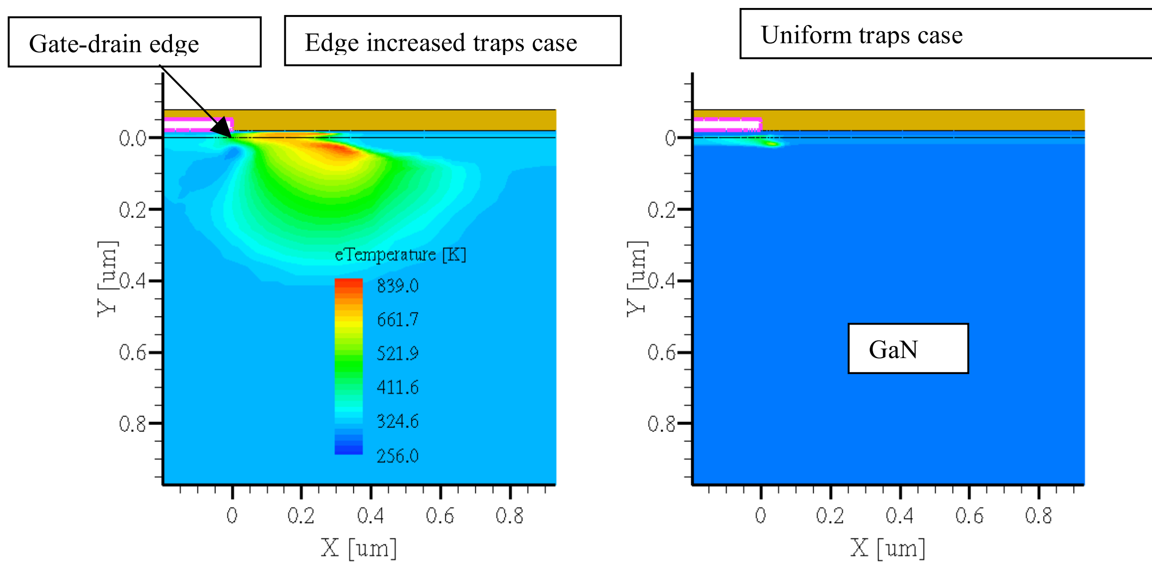


Fig. 54. Electron temperature under the gate-drain edge for the uniform and edge-increased trapping cases.

The 2DEG is in the horizontal direction along the 0 μm mark on the y-axis. The pink line in the figure indicates the gate-contact. The electron temperature is higher in the edge-increased trapping case. Figure 55 compares the electron density at 1.1 μs for both cases. The edge-increased trapping case shows more electrons spilling out of the 2DEG region in the gate-drain access region. As a consequence, the 2DEG density near the gate drain edge is depleted more in the edge-increased case.

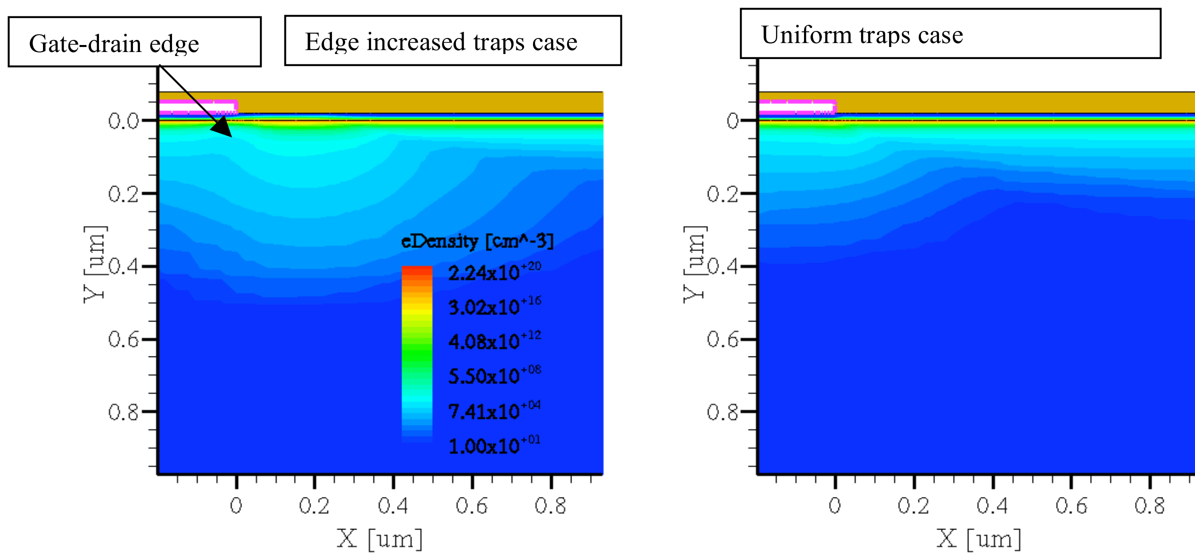


Fig. 55. Electron density as a function of position near the gate-drain edge for the uniform and edge-increased trapping cases.

We now consider the electron density close to the 2DEG. Acceptor traps capture hot electrons from the 2DEG, depleting the 2DEG. As these electrons are released from the traps, the 2DEG recovers and the current slowly returns to the original value. Figure 56 compares the trapped electron concentration in the device under the gate at 1.1 μs.

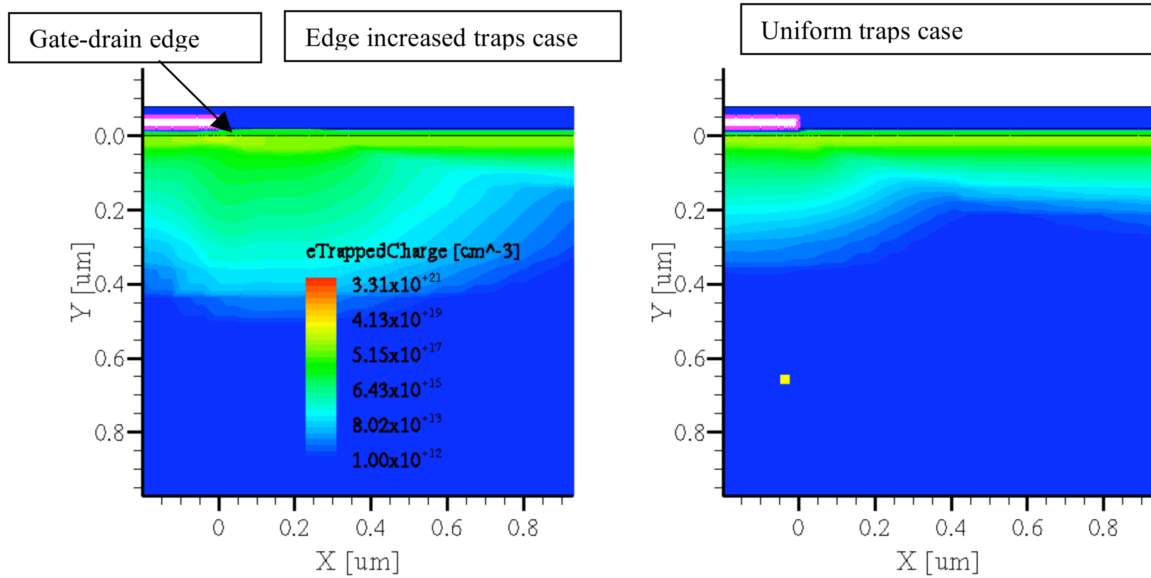


Fig. 56. Trapped electron concentration as a function of position near the gate-drain edge comparing the two cases.

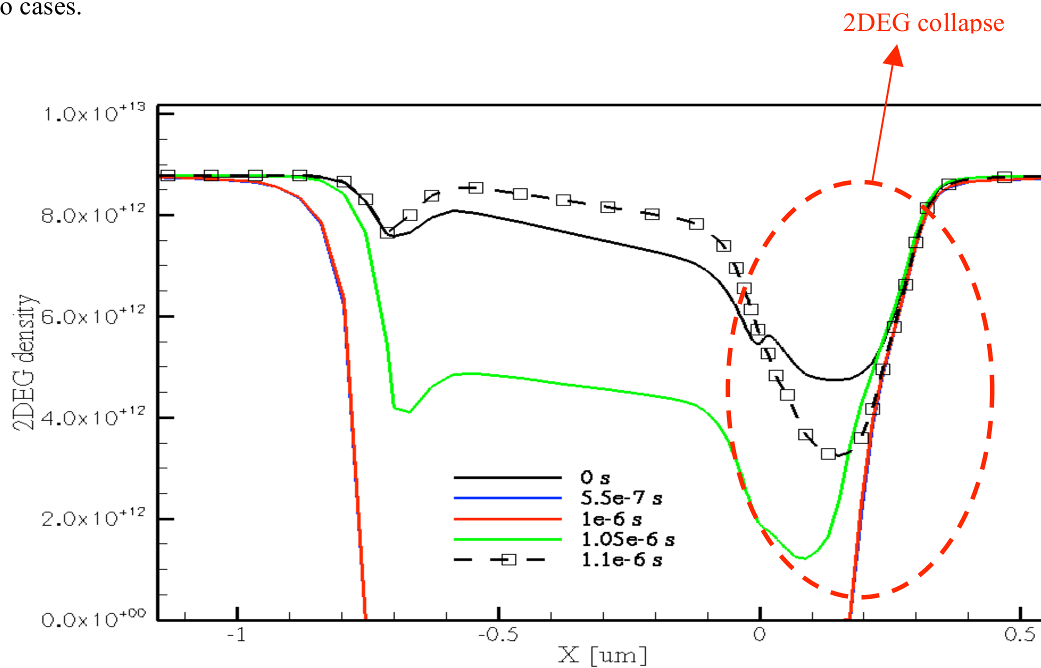


Fig. 57. 2DEG density (cm^{-2}) as a function of position in the device at different times.

Acceptor traps capture hot electrons from the 2DEG, depleting the 2DEG. As these electrons are released from the traps, the 2DEG recovers and the current slowly gets back to the original value. Figure 56 compares the trapped electron concentration in the device under the gate at 1.1 μs. Figure 57 is a horizontal cross section plot of the 2DEG in the device at various times during the voltage pulse. The device has a very low current density from 50 ns until 1.05 μs. The current slowly starts increasing at 1.05 μs. At 1.1 μs the 2DEG is not fully recovered when compared with the 0 s 2DEG density. This results in the observed gate-lag pulse.

If a uniform density corresponding to the peak value of the edge-increased distribution is used then it leads to a much larger amount of collapse. Figure 58 compares the normalized (I_D vs. time) gate-lag curves for the edge-increased and uniform trap density cases. The uniform trap density in the device is 4.4×10^{18} cm^{-3}. This is equal to the peak trap density near the gate-drain edge in the edge-increased case added to the background trap concentration of 1×10^{18} cm^{-3}. The edge-increased trap density is the same as discussed above. The collapse is about 50% for this larger uniform distribution case. Such large acceptor-like defect densities are not common in present day GaN HEMTs technology [35]. Uniform trap densities of the order of $\sim 10^{17}$ cm^{-3} are more common.

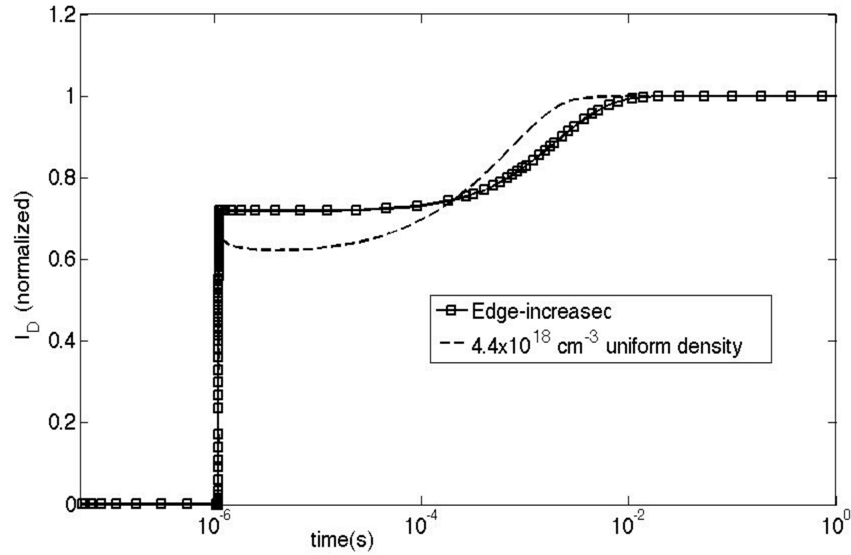


Fig. 58. Normalized drain current transients comparing edge-increased and a large uniform trap distribution.

7.2.1.2 Trap energy and gate-lag

This section discusses the impact of trap energy on the amount of gate-lag observed. Figure 59 is a plot comparing gate-lag at five different trap energies. For the purpose of comparison, the uniform trap density in the device was assumed to be 1×10^{18} cm^{-3} and the edge-increased trap density distribution near the drain and source access regions was assumed to have a peak of 3.5×10^{18} cm^{-3}. The traps were acceptor-like and their energy was specified with respect to midgap. Traps below midgap did not show any gate-lag. Also, donor-like traps did not yield gate-lag. The hot electrons generated near the 2DEG concentration and the trapped electron concentration near the gate-drain edge was negligible for both cases. Simulations indicate that the gate-lag is small but discernible for the 0.2 eV case; it is largest for the 1.0 eV case. The difference in the gate-lag between the 0.2 eV and the 1.0 eV cases can be explained by looking at the electron temperature and the trapped electron concentration as a function of position near the gate-drain edge of the device at different times. For the 0.2 eV case the spreading is not as

pronounced as the 1.0 eV case. Figure 60 is a plot of the electron temperature as a function of position at 0 s and 1.1 μs for traps at 0.2 eV and 1.0 eV.

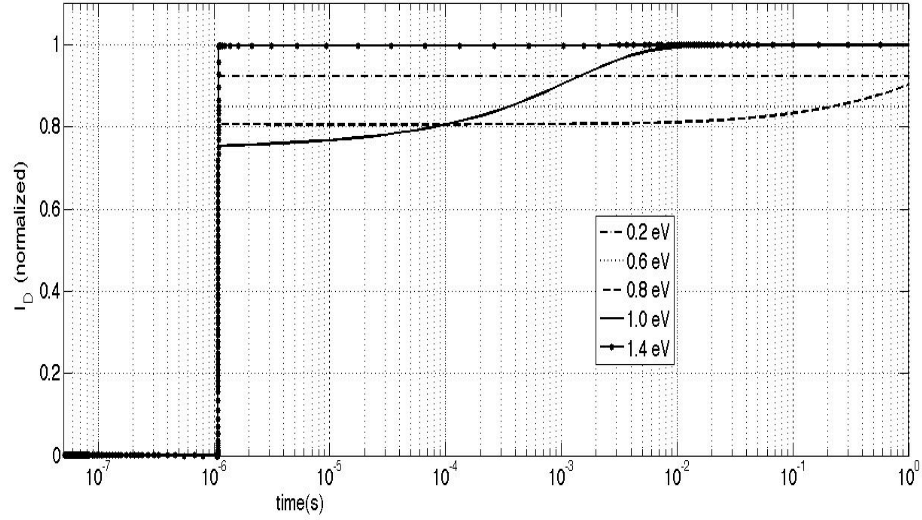
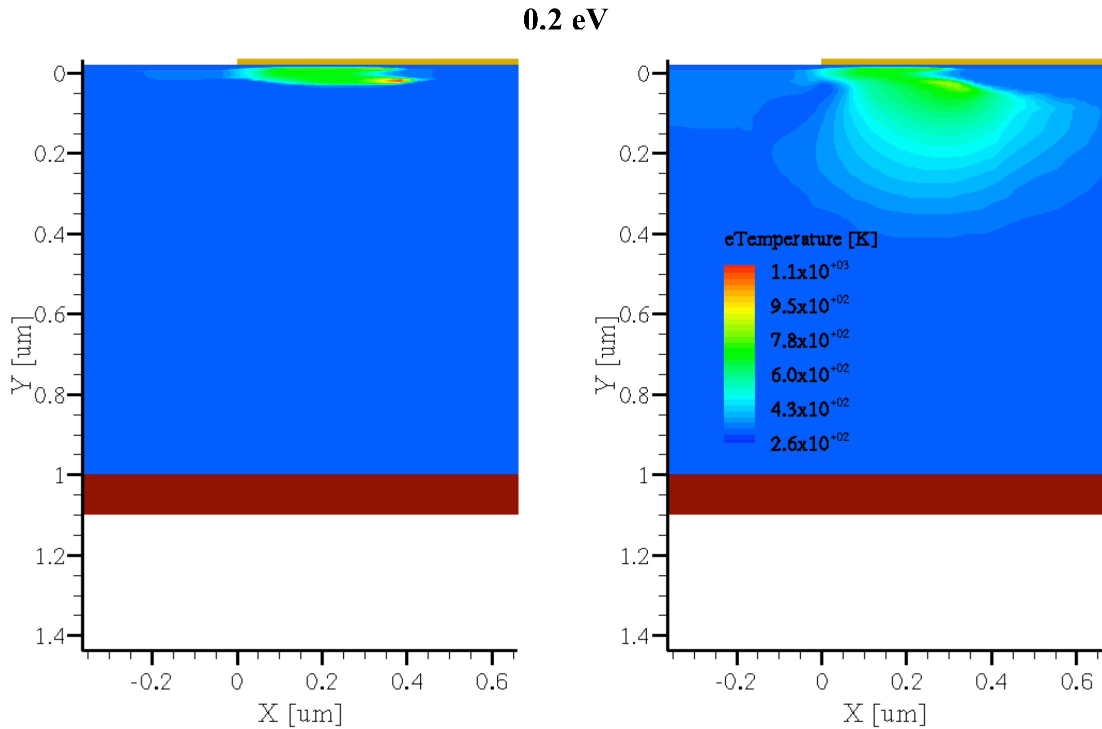


Fig. 59. Gate-lag using the edge-increased trap mechanism at 5 different trap energies; the trap distribution is the same for all the cases.



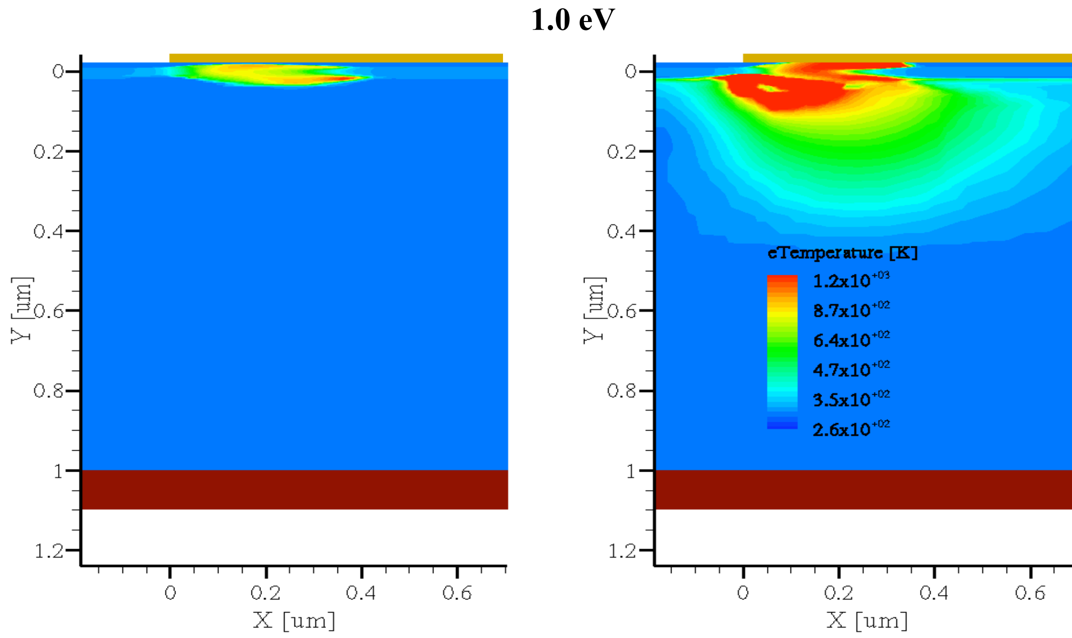


Fig. 60. Electron temperature as a function of position near the gate-drain edge comparing 0.2 eV and the 1.0 eV trap energies cases at 0 s and 1.1 μs, respectively.

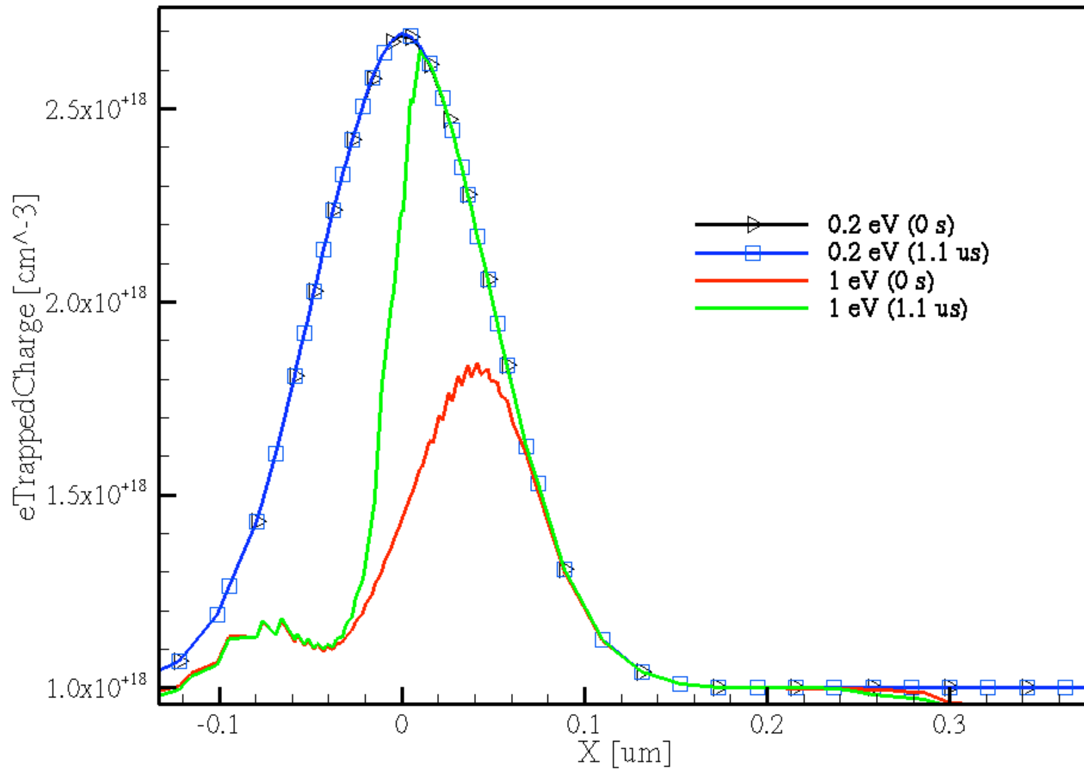


Fig. 61. Trapped electron concentration (cm^{-3}) comparing the 0.2 eV and 1.0 eV trap energies 0.02 μm below the 2DEG near the gate-drain edge at 0 s and 1.1 μs.

Figure 61 is a plot of the trapped electron concentration 0.02 μm below the 2DEG. The gate-drain edge is at 0 μm in the figure. These data show that the trapped electron concentration does not change between 0 and 1.1 μs for the 0.2 eV trap case. There is a much more dramatic change for the 1.0 eV case. This explains the larger amount of collapse observed here. Traps 1.4 eV above midgap do not cause any gate-lag. The electron temperature here is much smaller than the 0.2 eV and the 1.0 eV cases discussed above. The differences in electron temperatures between the different trap energy cases can be understood from the expression for electron current density used in the hydrodynamic model in TCAD [45].

$$J_n = \mu_n (n \nabla E_C + k_B T_n \nabla n + f_n^{td} k_B n \nabla T_n - 1.5 k_B T_n \nabla \ln m_e) \quad (31)$$

In equation 31 the gradient of the electron temperature is closely related to the gradient of the conduction band. Different trap energies correspond to different amounts of band bending in the device. This corresponds to different amounts of electric field near the gate-drain edge. The band bending in the 1.0 eV trap case is much more dramatic than for the 0.2 eV case. Figure 62 is a cross section of the conduction band along the gate-drain edge for the two trap cases at 1.1 μs. Figure 63 is a cross section of the electric field along the gate-drain edge. The electric field is comparable near the 2DEG, but as we go further down into the GaN region the field in the 1.0 eV case is much larger than the 0.2 eV case. This qualitatively explains the larger spread of hot electrons deeper into the GaN region for the 1.0 eV case.

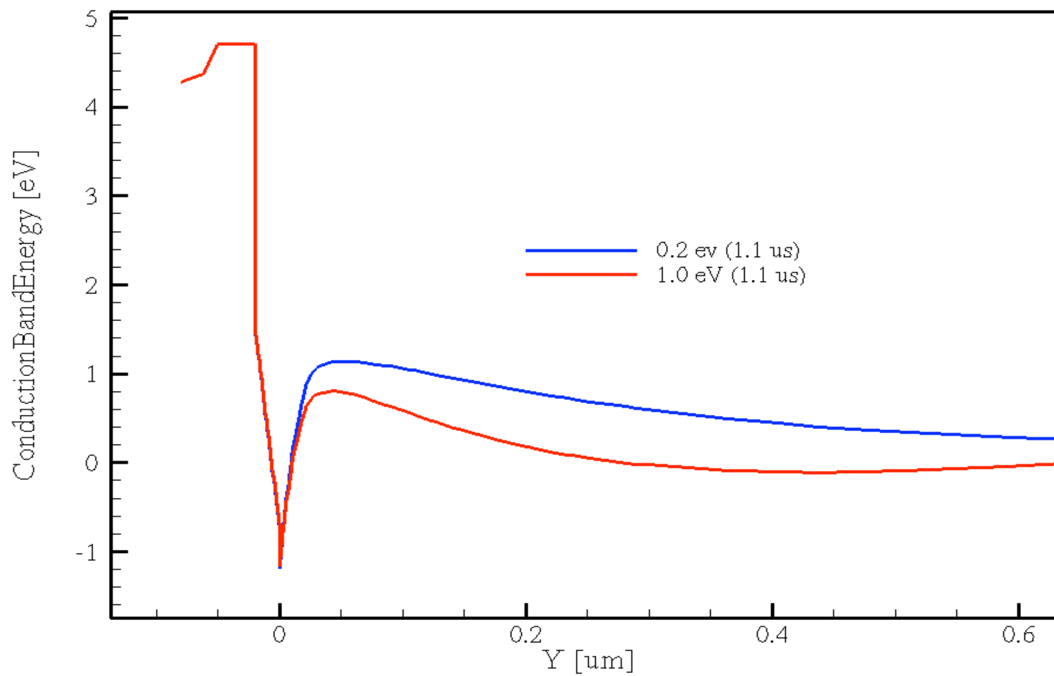


Fig. 62. Conduction band (vertical cross-section) as a function of position along the gate-drain edge.

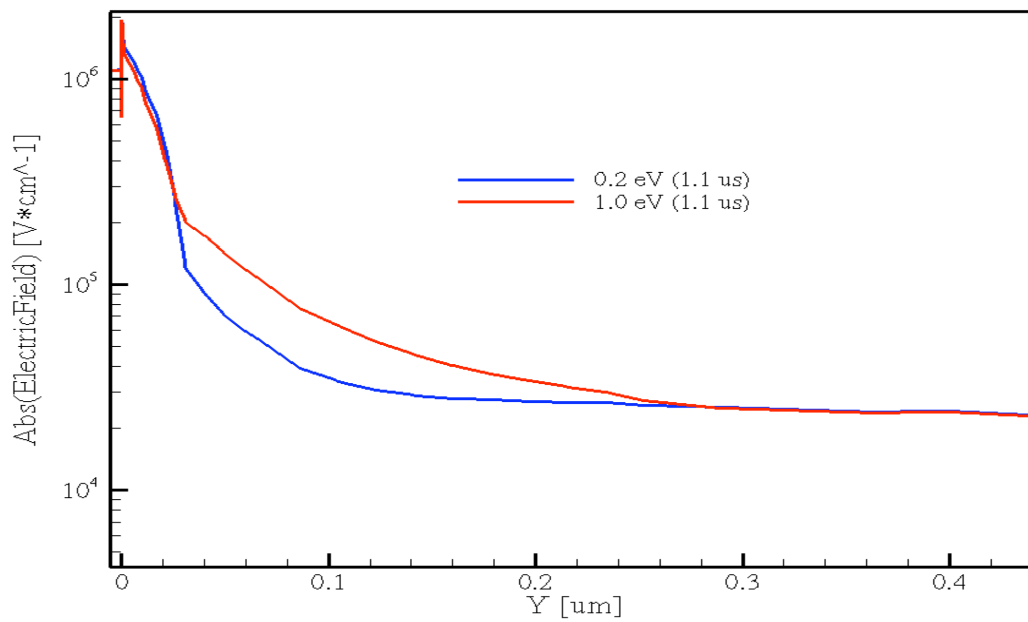


Fig. 63.Vertical cross-section of the electric field along the gate-drain edge.

7.2.1.3 Gate-lag and the Nitride passivation layer

In this section the impact of the passivation layer on the gate-lag in the device is examined. The uniform trap density in the device was 3×10^{18} cm^{-3}; the edge-increased trap distribution near the gate-drain and gate-source edges was assumed to have a peak density of 3.5×10^{18} cm^{-3}. This higher value of trap density makes the analysis much easier. The effect of the passivation layer on the electron temperature is easily seen in the simulation. The higher trap density leads to larger amounts of electron trapping in the GaN bulk. In the first case the passivation layer was chosen as silicon nitride; the second case assumed no passivation layer. Figure 64 is a plot comparing the gate-lag for the passivation and no-passivation case. Figure 65 compares the electron temperature for the two cases. Figure 66 compares the electric fields along the 2DEG for both cases at the bottom (-8 V) of the voltage pulse. Figure 67 is a plot of the electron density along the 2DEG.

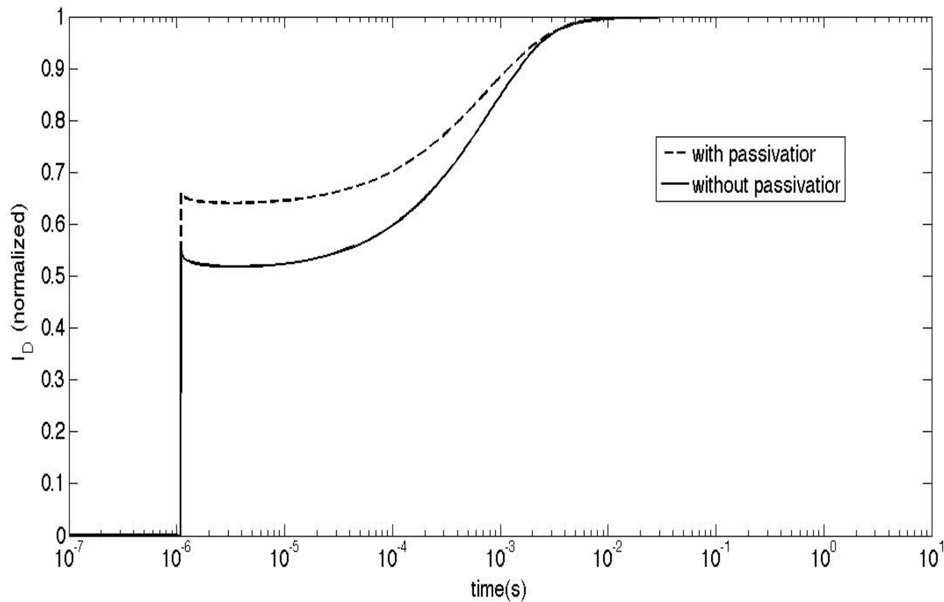


Fig. 64. Gate-lag (I_D vs. time) comparing the presence and absence of the passivation layer on the access regions.

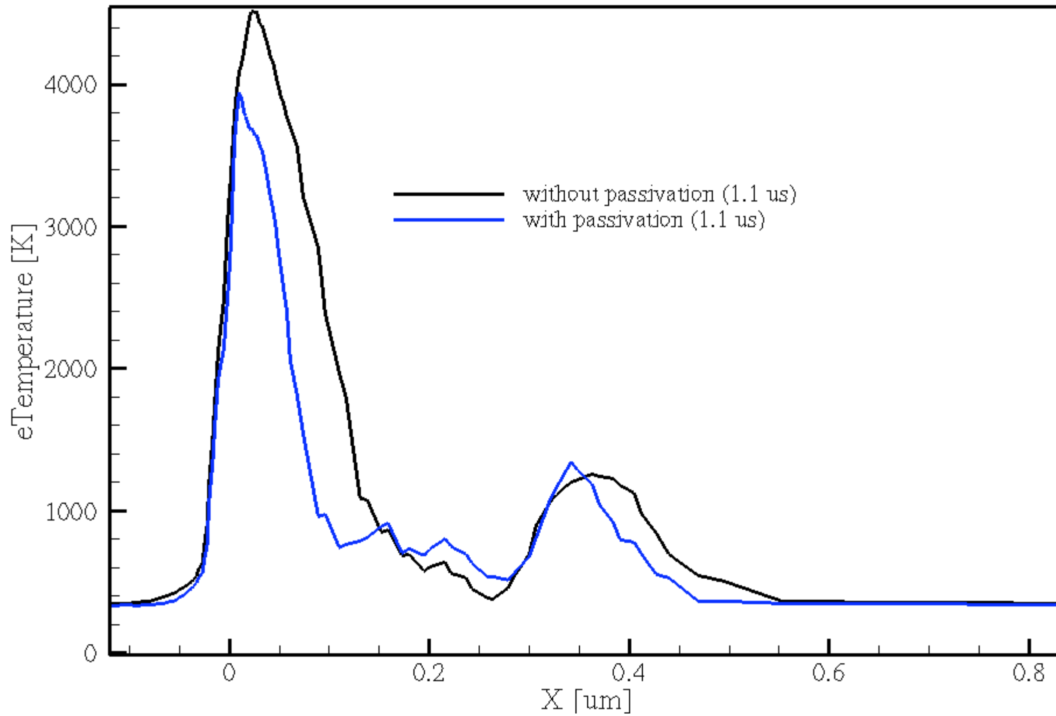


Fig. 65. Electron temperature horizontal cross section plot, 0.01 μm under the 2DEG for the two cases.

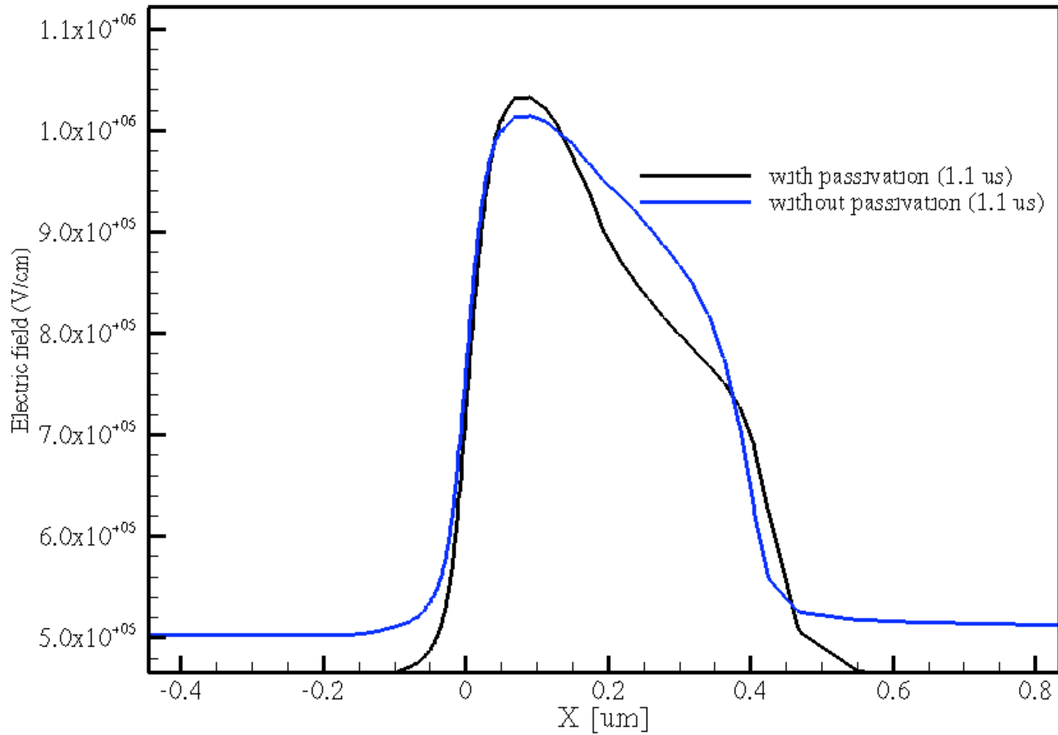


Fig. 66. Electric field horizontal cross section plot, 0.01 μm below the 2DEG.

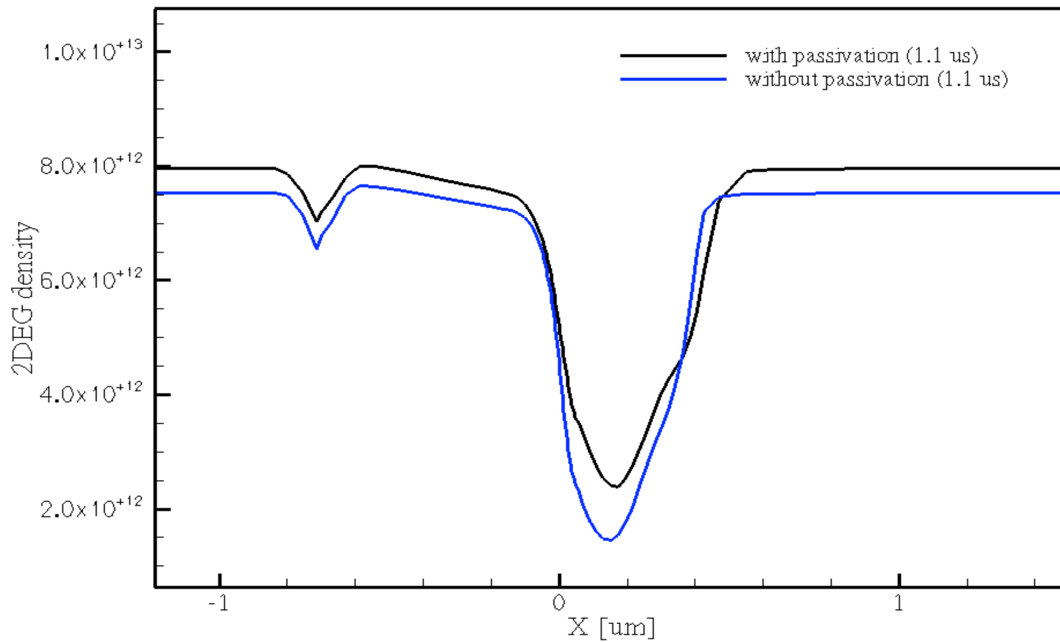


Fig. 67. 2DEG density as a function of position in the device.

From the above figures we see that the electron temperature along the 2DEG is much higher when there is no passivation layer. The passivation layer smoothes and reduces the electric field near the gate-drain edge. The simulation results suggest that a larger dielectric constant reduces the electric field and electron temperature near the gate-drain edge by reducing the coupling between the gate-field and the channel. The passivation layer also reduces the electric field between the gate and the channel. Figure 68 show the electron-temperature near the gate-drain region for the two cases at 0 s. The hot electron temperature near the gate-drain edge is much higher for the no passivation layer case. The presence of a passivation layer can reduce the high fields generated at the gate-drain access region and reduce gate-lag.

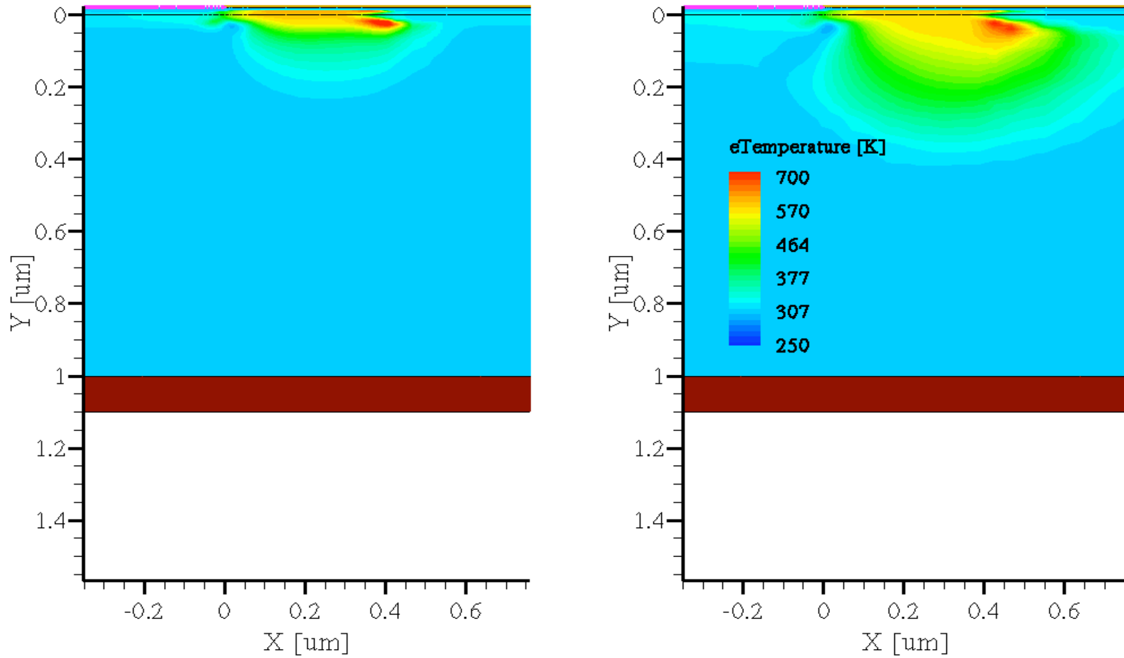


Fig. 68. Electron temperature at 0 s comparing the passivation and no passivation cases, respectively.

7.2.1.4 Comparison between experiment and simulation

Figure 69 is a plot of the gate-lag for large trap densities. The plot also includes the experimentally observed gate-lag, as well as simulated results for the surface-trap simulations (described in the next section). The traps were assumed to be acceptor-like and were 1.0 eV from the conduction band. These simulations suggest that a bulk trap density in excess of 10^{19} cm^{-3} near the gate-drain edge is needed to observe the magnitude of gate-lag seen in the experiment. Finally, the defect density data presented earlier in this section suggest that for MOCVD growth the maximum bulk impurity density in the device is on average around 10^{18} cm^{-3}. Simulations in this dissertation with defect densities of this order do not show gate-lag comparable with the experimental data. At these defect densities we see a collapse of only about 20%. On the other hand the experimental gate-lag observed is of the order of 50%. In summary, simulations suggest that the trapping of hot electrons in the bulk is a viable mechanism, but only if there are

bulk defect densities in the device that are an order of magnitude more than typically seen in the III-Nitride system.

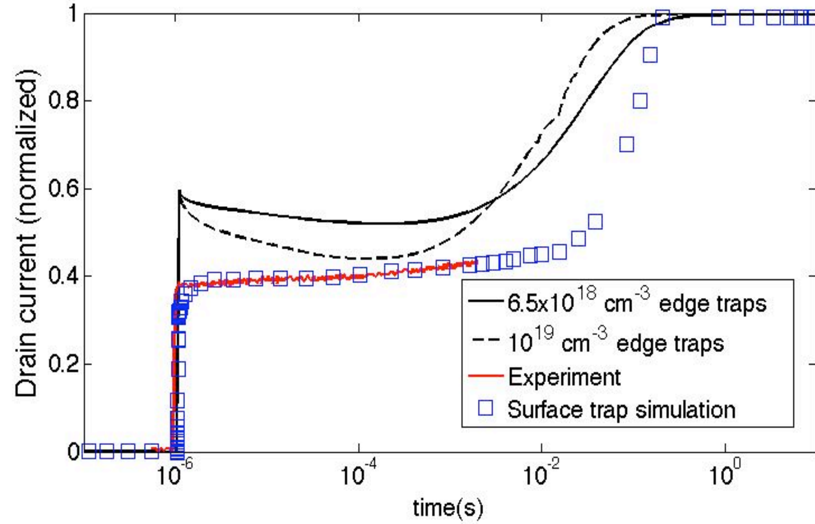


Fig. 69. Gate-lag comparison between experiments and simulations for the two mechanisms discussed.

7.2.1.5 Analysis of results for bulk trapping mechanism

Bulk traps in the GaN buffer contribute to the gate-lag by capturing hot electrons from the 2DEG, consistent with the results of hydrodynamic simulations. The temperature of these hot electrons is closely coupled to the trap distribution and the trap energy. These traps are acceptor type and above midgap. Gate-lag increases due to enhanced edge trapping near the gate-drain and gate-source edges. This increase in the gate-lag due to the edge-increased trapping is modeled in the simulations by superimposing a Gaussian trap distribution near the edges on a uniform trap distribution. Simulations also indicate that the maximum gate-lag is observed for acceptor traps that are ~1 eV above the midgap in GaN and AlGaN.

The amount of gate-lag due to this mechanism also depends on the presence or absence of a passivation layer on top of the device. The absence of a passivation layer implies higher fields at the gate-drain and gate-source edges. This increases the electron temperature near the gate-drain and gate-source edges and leads to more electrons leaking out of the 2DEG. Some of these electrons are captured in the bulk traps, leading to the observed gate-lag in the simulation.

The dip in the drain current in the bulk trap simulations between 1.1 μs and 10 ms in the gate-lag simulation plots is attributed to the reduction in mobility caused by the increase in the carrier temperature. The carrier temperature is higher at 1.1 μs when compared to the DC steady state bias. The increase in carrier temperature occurs because of the trapped electrons in the bulk near the gate edges. These trapped electrons cause an increase in the electric fields. This increase in field causes an increase in the electron temperature. Thus, trapped electrons near the gate-edge cause a temporary reduction in the mobility. This shows up as a dip in the bulk trap simulations.

7.2.2 Surface trap mechanism

The surface trap mechanism involves a change in the net charge density at the AlGaN/passivation interface. The mechanism can be described using a chart of the various space-charge components in the device, as shown in Figure 70. The diagram corresponds to a vertical cut line along the gate-drain access regions. The various space charge components are described along the cut line. The Nitride, AlGaN, AlN and GaN regions are indicated. The solid arrows pointing downwards imply negative space-charge components. The angled arrows indicate free electron and hole densities near the

interfaces. The dashed arrows pointing upwards imply positive space charge components. The blue line indicates the AlGaN/GaN interface.

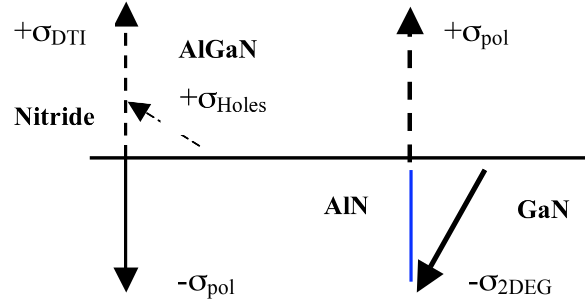


Fig. 70. Qualitative diagram of space charge components in the GaN HEMT device studied.

Here $\pm\sigma_{pol}$ is the fixed charge density due to the polarization charge at the interfaces. σ_{2DEG} is the 2D electron gas density, σ_{Holes} is the free hole accumulation charge density at the surface, and σ_{DTI} is the ionized donor trap density at the surface. The relationship between the surface components is described below in equation 35 [66]. The surface described here is the AlGaN surface.

$$\sigma_{net} = -\sigma_{pol} + \sigma_{Holes} + \sigma_{DTI} \tag{35}$$

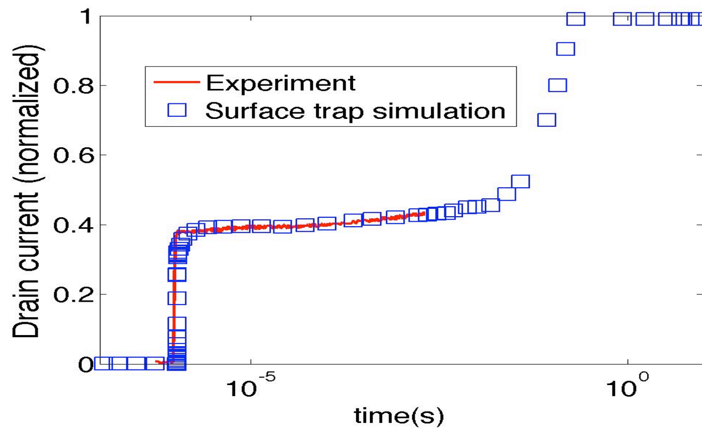


Fig. 71. Gate-lag transient simulated using the surface trap mechanism.

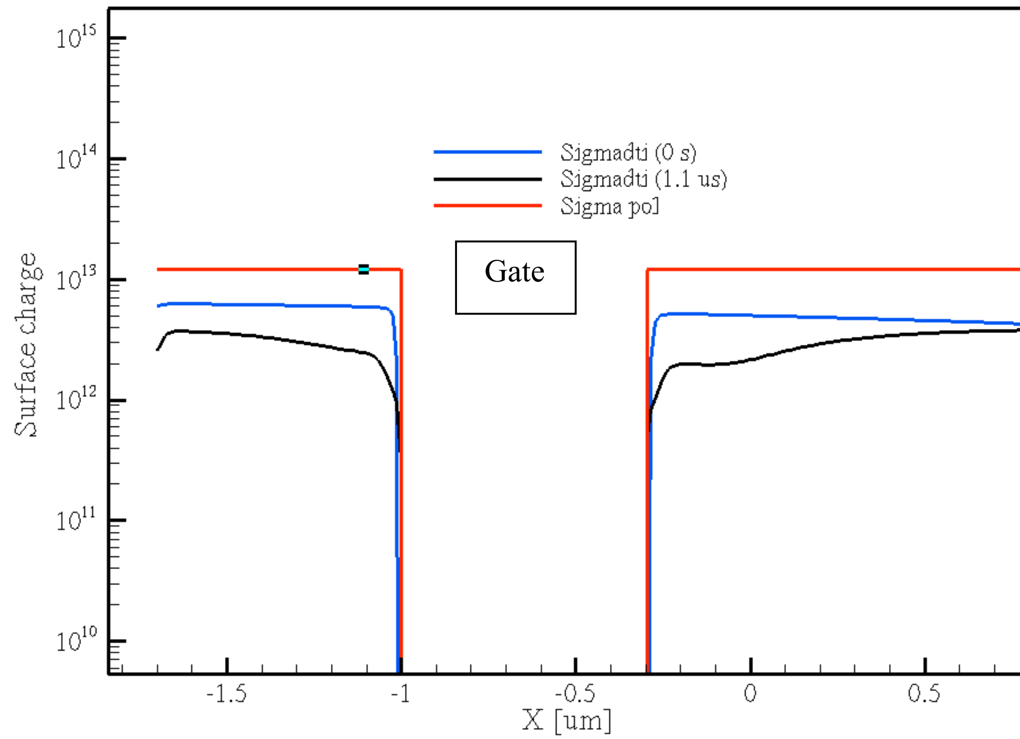


Fig. 72. Horizontal cross-section plot at the surface comparing at 0 s and 1.1 μs.

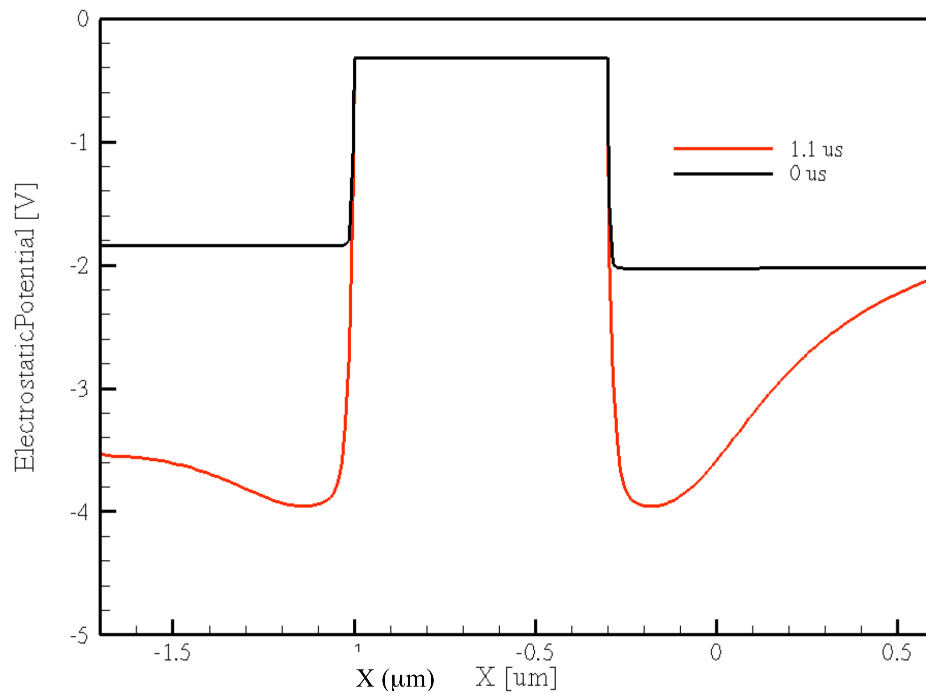


Fig. 73. Horizontal cross-section plot at the surface comparing potential at the surface at 0 s and 1.1 μs.

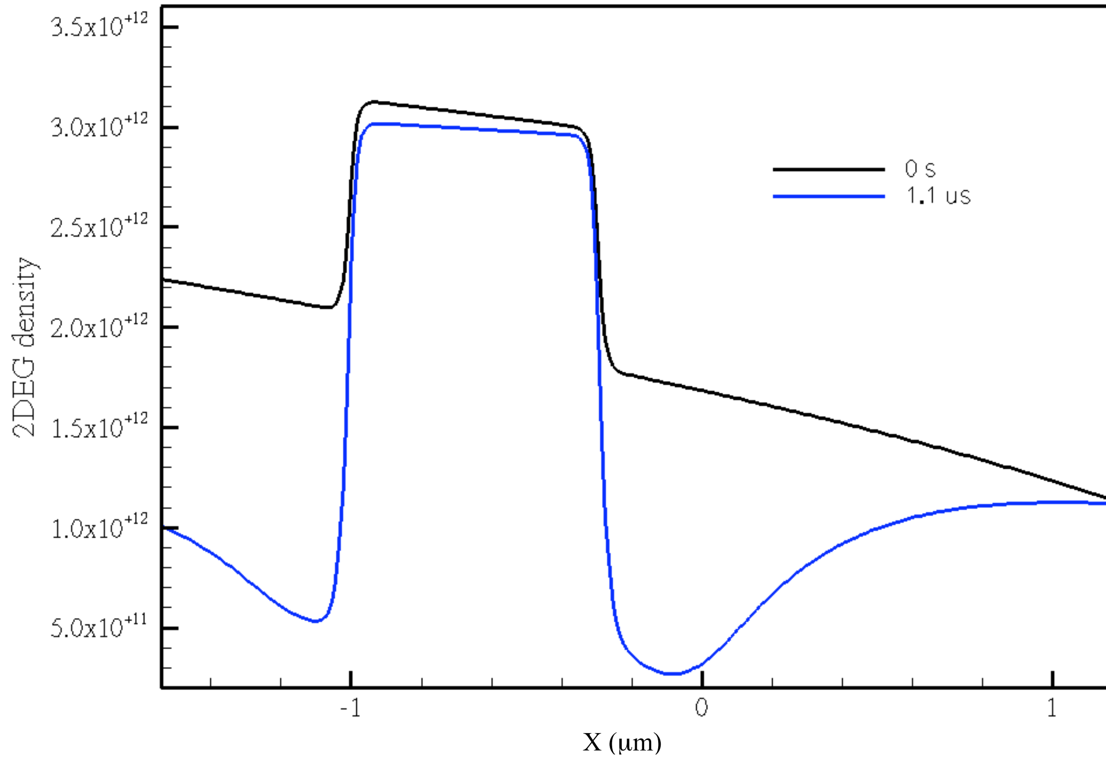


Fig. 74. 2DEG density as a function of position at 0 s and 1.1 μs.

Figure 71 is a plot comparing the experiment and the simulated gate-lag transient. The current has been normalized to the drain current measured in the DC characterization. The gate-pulse in the experiments and simulations in this section is from V_G= -8 V to -1 V. There is good qualitative agreement between experiment and simulation between the 0 and 10 ms times. The experiment data ends at 10 ms. The signal generator used in the experiment cannot generate a pulse longer than 10 ms. The simulation included a surface fixed charge density of -1×10^{13} cm^{-2}, and donor trap densities of 2×10^{13} cm^{-2} and 10^{13} cm^{-2} for traps at 0.3 eV and 0.5 eV, respectively, were chosen. The donor trap energies are specified with respect to the valence band edge.

These parameters were chosen to get qualitative agreement with the measured gate-lag transients.

A net change in the space charge at the surface will affect the 2DEG density in the channel. Figure 72 is a plot of the two components described above at 0 and 1.1 μs, σ_{pol} and σ_{dti}. These are the major space charge components at the surface; the hole concentration is negligible at the surface. At 0 s, there is a net negative charge on the surface. The two main components of this negative charge are the fixed $-\sigma_{pol}$ that does not change with time and the σ_{DTI}, which is the number of ionized donor traps at the surface. These donor traps change their state from neutral to positive once they are ionized. At 1.1 μs the σ_{DTI} decreases, which causes the surface to become more negative. This leads to the formation of a net negative charge on the surface that depletes the 2DEG. Figure 73 is a plot of the potential at the surface at these times. Finally, figure 74 is a plot of the 2DEG density. These two plots show the formation of the virtual gate and the impact it has on the 2DEG. This sequence of results suggests that the change in σ_{DTI} is the major mechanism responsible for the "virtual gate" modeled in these simulations [66]. The virtual gate refers to the temporary surface potential as described in figure 73.

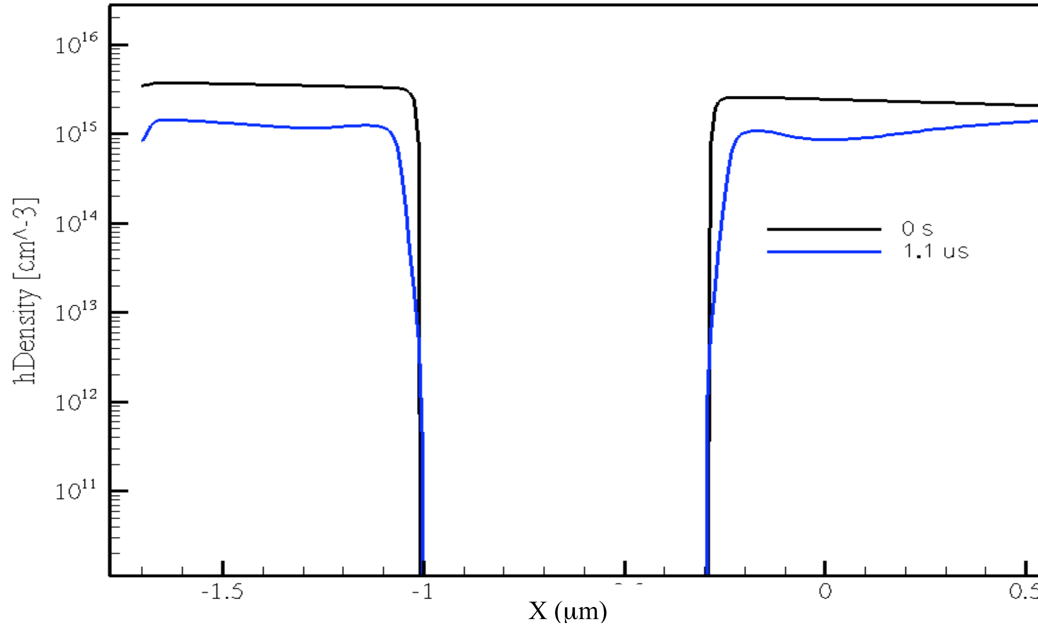


Fig. 75. Hole density as a function of position at the AlGaN surface at 0 s and 1.1 μs.

The free hole-density at the surface also provides positive charge at the surface, but the magnitude of holes at the surface is much smaller than σ_{DTI}. Figure 75 plots the free-hole density at the surface at 0 and 1.1 μs. The most likely reason for the variation in σ_{DTI} is hole capture or electron emission [67, 69]. Finally, the bias condition will have a large role to play in how many of these traps get ionized. The bias condition will determine the quasi-Fermi level at the surface for the holes. This will eventually affect the amount of σ_{DTI}.

7.2.2.1 Trap energy and gate-lag

The energy of the trap relative to the valence band also affects the amount of gate-lag in the device. Figure 76 is a plot of the simulated gate-lag in the device for three different trap energies. Figure 77 is a plot of the simulated band diagram for various donor trap energies.

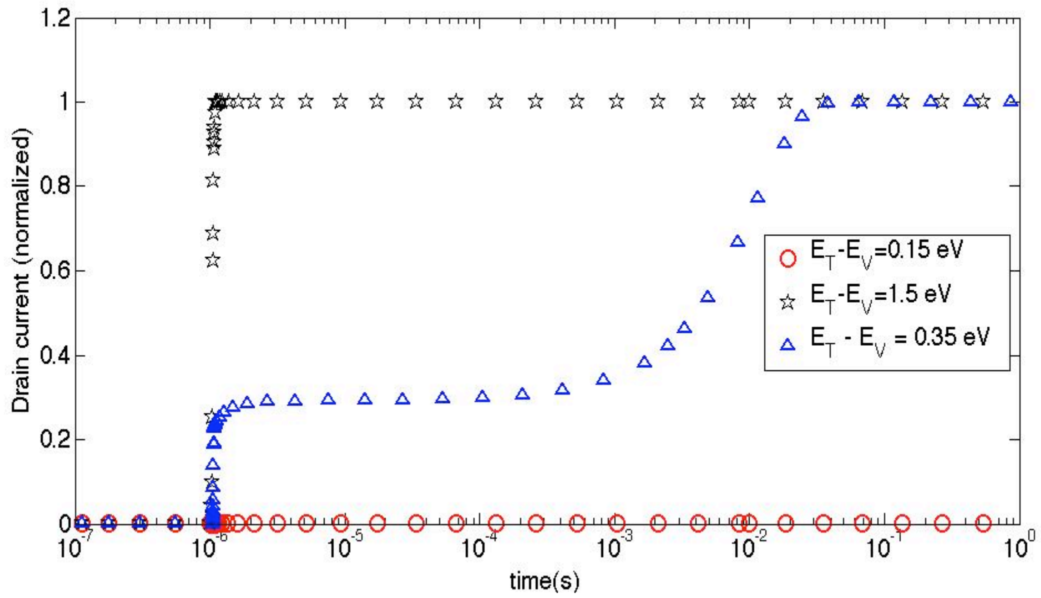


Fig. 76. Gate-lag for surface donor traps at different energies.

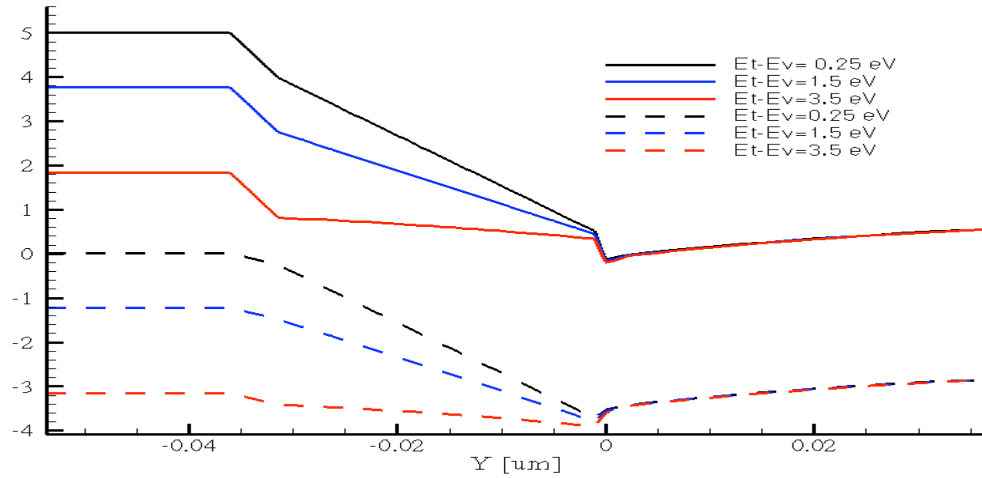


Fig. 77. Band diagrams for three trap energies at ($V_G = V_D = 0$ V) along a vertical cut in the middle of the gate-drain access region; the energy zero is the Fermi level position. Solid lines are the conduction band and the dashed lines are the valence band energies.

The placement of the trap in the band has the following effects. For traps close to the valence band edge, most of the donors at the surface are neutral, leading to a larger net negative surface charge (σ_{pol} - σ_{DTI}). This net negative surface charge causes the bands to bend. The bending of the bands causes the accumulation of holes at the surface. The increase in the net negative charge also causes a reduction in the 2DEG density. The

formation of a net negative charge on the un-gated surface in the above-mentioned fashion is called the "virtual gate" model. As donor traps get farther away from the valence band, σ_{DTI} increases and the net negative charge at the surface decreases. This reduces the hole accumulation at the surface. The band bending is less severe and consequently the 2DEG is not depleted as much.

7.2.2.2 Effects of surface traps

Figure 72 compares measured and simulated gate-lag. The data match well; these results are consistent with studies suggesting that surface traps are the dominant mechanism responsible for gate-lag in these devices [28, 35, 66, 67, 69]. These studies suggest donor trap densities of the order of ~10^{13} cm^{-2} and a fixed charge density of about -10^{13} cm^{-2} at the AlGaN surface [35, 66, 67, 69]. Also, the trap energy ranges and the mechanism suggested in these studies are the same as the results in this dissertation [28, 66, 67, 69]. In summary our results suggest donor traps very close to the valence band (within 0.3 eV) at the surface cause the most dramatic gate-lag.

7.3 Impact of proton irradiation induced bulk traps on gate-lag

This section discusses the impact of proton-irradiation induced bulk defects on gate-lag. Low energy (1.8 MeV) proton irradiation allows a controlled introduction of defects in the device structure. Figure 78 is a plot of the measured and simulated gate-lag at three different proton fluences. Increasing fluences correspond to an increased number of bulk traps in the GaN HEMT structure. With increasing fluence the amount of gate-lag becomes worse. There is no appreciable change in the shape of the

pulse, suggesting that adding bulk traps reduces the 2DEG density by mainly degrading mobility and band bending. This suggests that the bulk traps created in these devices due to proton irradiation are not enough to cause a substantial change in the gate-lag due to the bulk trap gate-lag mechanism. The calibrated TCAD input deck for the gate-lag uses the surface trap mechanism. The pre-irradiation case has the same calibrated characteristics as described in Chapter 4. This deck is used to study the impact of proton irradiation-induced bulk traps on gate-lag. Trap density information for a given fluence is obtained from SRIM simulations. As an example, at 5×10^{14} cm^{-2} fluence, the bulk trap density in the GaN layer is 5×10^{17} cm^{-3} and 10^{18} cm^{-3} in the AlGaN. The energies of these bulk traps are obtained from proton implantation studies in GaN and AlGaN [54, 57]. In p-type GaN, the defects are formed at 0.9 eV and 0.3 eV from the valence band edge. These defects are donor-like and make the material less p-type. On the other hand, defects in the n-type AlGaN layer are predominantly formed at 3.7 eV and 2.3 eV from the conduction band edge.

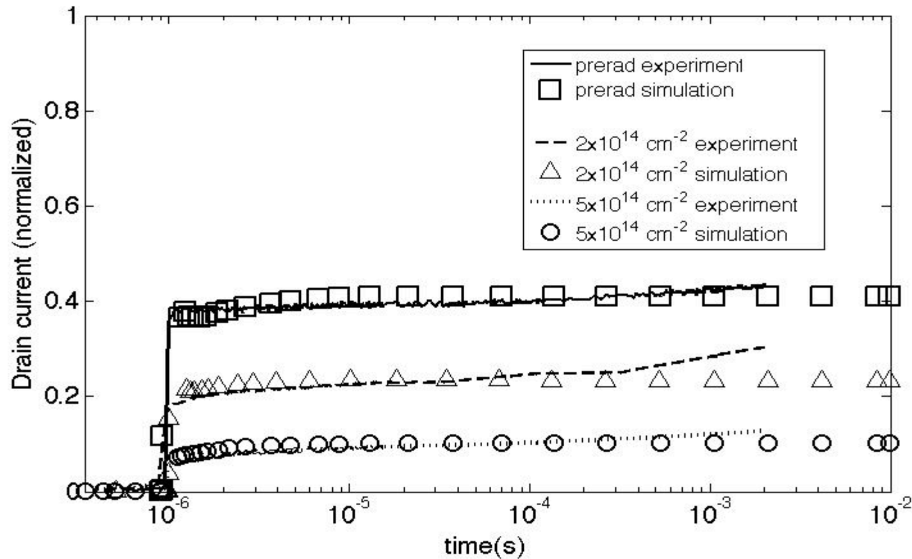


Fig. 78. Gate-lag simulation and experiment transients at different fluences.

In summary, gate-lag increases with increasing proton fluence in the device due to the electrostatic effects of the bulk traps. Although the primary mechanism for gate-lag is the surface trapping mechanism, the introduction of bulk defects in the structure reduces the 2DEG density because of band bending and mobility degradation [3]. This is responsible for the increase in the experimentally observed gate-lag at higher fluences. Simulations suggest that, at fluences used in the experiments in this dissertation, the bulk trap density is not large enough to affect the gate-lag by the bulk trapping mechanism. The amount of gate-lag can only be accounted for by the bulk trap mechanism if the bulk trap density is ~ 10^{19} cm^{-3}. This number is an order of magnitude greater than the defect density suggested in the literature [35].

7.4 Conclusion

This chapter discusses the impact of bulk traps and surface traps on gate-lag. It also discusses the impact of proton irradiation induced bulk defects on gate-lag. The bulk trapping mechanism can be thought of as the capture of energetic or “hot” electrons from the 2DEG in the bulk of the device. This causes the formation of a quasi-space charge region that reduces the 2DEG density. This mechanism is very closely related to the bulk trap density, distribution, and the presence or absence of a passivation layer. The sensitivity of gate-lag to the above-mentioned parameters is quantified. The capture of electrons in bulk traps is a possible mechanism for gate-lag but not the dominant mechanism. This chapter also discussed the surface trapping mechanism. This mechanism involves the time-dependent change in the net negative surface charge. This time dependent change in the net negative charge at the surface reduces the 2DEG

density. This eventually causes the gate-lag observed. Simulations and experiments suggest that the surface trapping mechanism is the dominant mechanism in the device. Putting in bulk traps via proton irradiation into the device degraded the gate-lag further. Simulations suggest that this is due to electrostatic effects of bulk traps.

CHAPTER 8

CONCLUSIONS

TCAD simulations and experiments were used to study the relationship between bulk traps and the DC and RF characteristics of GaN HEMTs. Charged bulk traps in the GaN bulk and other regions of the device degrade the 2DEG density and the mobility in the device. The band bending decreases the 2DEG density, which in turn reduces the drain current in the device. The effect of the defect energy levels on the 2DEG density was also studied. Charged bulk traps also degrade the mobility in the 2DEG. Band bending and mobility degradation cause a reduction in the drain current. Mobility degradation is closely coupled with the self-heating in the device.

Experiments and simulations showing the impact of bulk traps on current collapse in AlGaN/AlN/GaN HEMTs were also studied. Two different mechanisms explaining gate-lag were discussed. These were the bulk trapping mechanism and surface trapping mechanism. The bulk trapping mechanism can be thought of as the capture of energetic or "hot" electrons from the 2DEG in the bulk of the device. This causes the formation of a quasi-space-charge region that reduces the 2DEG density. This mechanism is very closely related to the bulk trap density, distribution, and the presence/absence of a passivation layer. The sensitivity of gate-lag to the above-mentioned parameters was quantified. Simulations and experiments suggest that the capture of electrons in bulk traps is a possible mechanism for gate-lag but not the dominant mechanism. The surface trapping mechanism was also discussed. This mechanism involves the time-dependent

change in the net negative surface charge. This time dependent change in the net negative charge at the surface reduces the 2DEG density. This eventually causes the majority of the gate-lag observed. These results should help to understand and improve the performance, reliability, and radiation response of GaN-based HEMTs.

REFERENCES

[1] J. C. Zolper, "Status challenges and future opportunities for compound semiconductors," *IEEE GaAs IC symposium Technical Digest,* pp. 3-6, 2003.

[2] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs," *Proceedings of the IEEE,* vol. 90, pp. 1048-1058, Jun 2002.

[3] A. Kalavagunta, A. Touboul, L. Shen, R. D. Schrimpf, R. A. Reed, D. M. Fleetwood, R. K. Jain, and U. K. Mishra, "Electrostatic mechanisms responsible for device degradation in AlGaN/AlN/GaN HEMTs," *IEEE Transactions on Nuclear Science,*vol 55, pp. 2106-2112, Aug 2008.

[4] M. A. Khan, M. S. Shur, Q. C. Chen, and J. N. Kuznia, "Current-voltage characteristic collapse in AlGaN/GaN heterostructure insulated gate field-effect transistors at high drain bias," *Electronics Letters,* vol. 30, pp. 2175-2176, Dec 8 1994.

[5] N. Braga, R. Mickevicius, R. Gaska, M. S. Shur, M. A. Khan, and G. Simin, "Simulation of gate lag and current collapse in gallium nitride field-effect transistors," *Applied Physics Letters,* vol. 85, pp. 4780-4782, Nov 2004.

[6] M. A. Khan, J. N. Kuznia, J. M. Vanhove, N. Pan, and J. Carter, "Observation of a 2-dimensional electron-gas in low-pressure metalorganic chemical vapor-deposited GaN-AlGaN heterojunctions," *Applied Physics Letters,* vol. 60, pp. 3027-3029, Jun 1992.

[7] M. A. Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, "High-electron-mobility transistor based on a GaN-AlGaN heterojunction," *Applied Physics Letters,* vol. 63, pp. 1214-1215, Aug 1993.

[8] M. A. Khan, J. N. Kuznia, D. T. Olson, W. J. Schaff, J. W. Burm, and M. S. Shur, "Microwave performance of a 0.25 µm gate AlGaN/GaN heterostructure field-effect transistor," *Applied Physics Letters,* vol. 65, pp. 1121-1123, Aug 1994.

[9] Y. F. Wu, B. P. Keller, S. Keller, D. Kapolnek, S. P. Denbaars, and U. K. Mishra, "Measured microwave power performance of AlGaN/GaN MODFET," *IEEE Electron Device Letters,* vol. 17, pp. 455-457, Sep 1996.

[10] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMT's," *IEEE Electron Device Letters,* vol. 21, pp. 268-270, Jun 2000.

[11] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, "10-W/mm AlGaN-GaNHFET with a field modulating plate," *IEEE Electron Device Letters,* vol. 24, pp. 289-291, May 2003.

[12] A. Chini, D. Buttari, R. Coffie, S. Heikman, S. Keller, and U. K. Mishra, "12W/mm power density AlGaN/GaN HEMTs on sapphire substrate," *Electronics Letters,* vol. 40, pp. 73-74, Jan 2004.

[13] Y. F. Wu, W. S. Keller, G. Parish, N. Zhang, J. J. Xu, B. P. Keller, S. P. DenBaars and U. K. Mishra, "Gallium nitride based high power heterojunction field effect transistor: Process development and present status at UCSB," *IEEE Transactions on Electron Devices,,* vol. 48, pp. 552-559, 2001.

[14] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," *IEEE Spectrum,* vol. 2, p. 49, 1965.

[15] L.Lu, *IEEE MTT-S Digest,* pp. 1709-1712, 2001.

[16] S. C. Binari, K. Doverspike, G. Kelner, H. B. Dietrich, and A. E. Wickenden, "GaN FETs for microwave and high-temperature applications," *Solid-State Electronics,* vol. 41, pp. 177-180, Feb 1997.

[17] B. Luo, J. W. Johnson, F. Ren, K. K. Allums, C. R. Abernathy, S. J. Pearton, R. Dwivedi, T. N. Fogarty, R. Wilkins, A. M. Dabiran, A. M. Wowchack, C. J. Polley, P. P. Chow, and A. G. Baca, "DC and RF performance of proton-irradiated AlGaN/GaN high electron mobility transistors," *Applied Physics Letters,* vol. 79, pp. 2196-2198, Oct 2001.

[18] B. Luo, J. W. Johnson, F. Ren, K. K. Allums, C. R. Abernathy, S. J. Pearton, A. M. Dabiran, A. M. Wowchack, C. J. Polley, P. P. Chow, D. Schoenfeld, and A. G. Baca, "Influence of Co-60 gamma-rays on dc performance of AlGaN/GaN high electron mobility transistors," *Applied Physics Letters,* vol. 80, pp. 604-606, Jan 2002.

[19] B. D. White, M. Bataiev, S. H. Goss, X. Hu, A. Karmarkar, D. M. Fleetwood, R. D. Schrimpf, W. J. Schaff, and L. J. Brillson, "Electrical, spectral, and chemical properties of 1.8 MeV proton irradiated AlGaN/GaN HEMT structures as a function of proton fluence," *IEEE Transactions on Nuclear Science,* vol. 50, pp. 1934-1941, Dec 2003.

[20] A. P. Karmarkar, B. D. White, D. Buttari, D. M. Fleetwood, R. D. Schrimpf, R. A. Weller, L. J. Brillson, and U. K. Mishra, "Proton-induced damage in gallium nitride-based Schottky diodes," *IEEE Transactions on Nuclear Science,* vol. 52, pp. 2239-2244, Dec 2005.

[21] D. Delagebeaudeuf and N. T. Linh, "Charge control of the heterojunction two-dimensional electron-gas for Mesfet application," *IEEE Transactions on Electron Devices,* vol. 28, pp. 790-795, 1981.

[22] D. Delagebeaudeuf and N. T. Linh, "Metal-(N) AlGaAs-GaAs two-dimensional electron-gas FET," *IEEE Transactions on Electron Devices,* vol. 29, pp. 955-960, 1982.

[23] W. D. Hu, X. S. Chen, Z. J. Quan, C. S. Xia, W. Lu, and P. D. Ye, "Self-heating simulation of GaN-based metal-oxide-semiconductor high-electron-mobility transistors including hot electron and quantum effects," *Journal of Applied Physics,* vol. 100, pp.074501-1-074501-9, Oct 2006.

[24] J. B. Walker, "High-Power GaAs FET Amplifiers," *Artech House, Norwood MA,* p. Chapter 1, 1993.

[25] P. B. Klein, S. C. Binari, K. Ikossi-Anastasiou, A. E. Wickenden, D. D. Koleske, R. L. Henry, and D. S. Katzer, "Investigation of traps producing current collapse in AlGaN/GaN high electron mobility transistors," *Electronics Letters,* vol. 37, pp. 661-662, May 2001.

[26] A. Tarakji, G. Simin, N. Ilinskaya, X. Hu, A. Kumar, A. Koudymov, J. Yang, M. A. Khan, M. S. Shur, and R. Gaska, "Mechanism of radio-frequency current collapse in GaN-AlGaN field-effect transistors," *Applied Physics Letters,* vol. 78, pp. 2169-2171, Apr 2001.

[27] T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, and K. Maezawa, "A study on current collapse in AlGaN/GaN HEMTs induced by bias stress," *IEEE Transactions on Electron Devices,* vol. 50, pp. 2015-2020, Oct 2003.

[28] R. Vetury, N. Q. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of A1GaN/GaN HFETs," *IEEE Transactions on Electron Devices,* vol. 48, pp. 560-566, Mar 2001.

[29] I. P. Smorchkova, L. Chen, T. Mates, L. Shen, S. Heikman, B. Moran, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "AlN/GaN and (Al_x,Ga_{1-x}) N/AlN/GaN two-dimensional electron gas structures grown by plasma-assisted molecular-beam epitaxy (vol 90, pg 5196, 2001)," *Journal of Applied Physics,* vol. 91, pp. 4780-4780, Apr 2002.

[30] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, A. J. Sierakowski, W. J. Schaff, L. F. Eastman, R. Dimitrov, A. Mitchell, and M. Stutzmann, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *Journal of Applied Physics,* vol. 87, pp. 334-344, Jan 2000.

[31] B. E. Foutz, O. Ambacher, M. J. Murphy, V. Tilak, and L. F. Eastman, "Polarization induced charge at heterojunctions of the III-V nitrides and their alloys," *Physica Status Solidi B-Basic Research,* vol. 216, pp. 415-418, Nov 1999.

[32] E. J. Miller, E. T. Yu, C. Poblenz, C. Elsass, and J. S. Speck, "Direct measurement of the polarization charge in AlGaN/GaN heterostructures using capacitance-voltage carrier profiling," *Applied Physics Letters,* vol. 80, pp. 3551-3553, May 2002.

[33] I. P. Smorchkova, C. R. Elsass, J. P. Ibbetson, R. Vetury, B. Heying, P. Fini, E. Haus, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization-induced charge and electron mobility in AlGaN/GaN heterostructures grown by plasma-assisted molecular-beam epitaxy," *Journal of Applied Physics,* vol. 86, pp. 4520-4526, Oct 1999.

[34] L. Shen, "Advanced polarization based design of AlGaN/GaN HEMTs Ph.D dissertation University of California Santa Barbara," 2004.

[35] S. J. Pearton, J. C. Zolper, R. J. Shul, and F. Ren, "GaN: Processing, defects, and devices," *Journal of Applied Physics,* vol. 86, pp. 1-78, Jul 1999.

[36] P. B. Klein, "Photoionization spectroscopy in AlGaN/GaN high electron mobility transistors," *Journal of Applied Physics,* vol. 92, pp. 5498-5502, Nov 2002.

[37] P. B. Klein and S. C. Binari, "Photoionization spectroscopy of deep defects responsible for current collapse in nitride-based field effect transistors," *Journal of Physics-Condensed Matter,* vol. 15, pp. R1641-R1667, Nov 2003.

[38] P. B. Klein, S. C. Binari, J. A. Freitas, and A. E. Wickenden, "Photoionization spectroscopy of traps in GaN metal-semiconductor field-effect transistors," *Journal of Applied Physics,* vol. 88, pp. 2843-2852, Sep 2000.

[39] P. B. Klein, J. A. Freitas, S. C. Binari, and A. E. Wickenden, "Observation of deep traps responsible for current collapse in GaN metal-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 75, pp. 4016-4018, Dec 1999.

[40] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in

AlGaN/GaN heterostructure field effect transistors," *Applied Physics Letters,* vol. 77, pp. 250-252, Jul 2000.

[41] A. Kalavagunta, R. D. Schrimpf, and M. Neifeld, "Design considerations for optical systems in ionizing and nonionizing radiation environments," *IEEE Transactions on Nuclear Science,* vol. 51, pp. 3595-3602, Dec 2004.

[42] A. Koudymov, V. Adivarahan, J. Yang, G. Simin, and A. A. Khan, "Mechanism of current collapse removal in field-plated nitride HFETs," *IEEE Electron Device Letters,* vol. 26, pp. 704-706, Oct 2005.

[43] J. F. Ziegler, "Stopping and Range of Ions in Matter," *Bulletin of the American Physical Society,* vol. 23, pp. 1020-1020, 1978.

[44] A. P. Karmarkar, B. G. Jun, D. M. Fleetwood, R. D. Schrimpf, R. A. Weller, B. D. White, L. J. Brillson, and U. K. Mishra, "Proton irradiation effects on GaN-based high electron-mobility transistors with Si-doped $Al_xGa_{1-x}N$ and thick GaN cap layers," *IEEE Transactions on Nuclear Science,* vol. 51, pp. 3801-3806, Dec 2004.

[45] ISE Integrated Systems Engineering AG, "DESSIS ISE TCAD Manual," Release 10.06, 2005.

[46] U. V. Bhapkar and M. S. Shur, "Monte Carlo calculation of velocity-field characteristics of wurtzite GaN," *Journal of Applied Physics,* vol. 82, pp. 1649-1655, Aug 1997.

[47] A. Koudymov, G. Simin, M. A. Khan, A. Tarakji, R. Gaska, and M. S. Shur, "Dynamic current-voltage characteristics of III-NHFETs," *IEEE Electron Device Letters,* vol. 24, pp. 680-682, Nov 2003.

[48] K. Blotekja, "Transport equations for electrons in 2- valley semiconductors," *IEEE Transactions on Electron Devices,* vol. Ed17, pp. 38-&, 1970.

[49] C. D. Wang, L. S. Yu, S. S. Lau, E. T. Yu, W. Kim, A. E. Botchkarev, and H. Morkoc, "Deep level defects in n-type GaN grown by molecular beam epitaxy," *Applied Physics Letters,* vol. 72, pp. 1211-1213, Mar 1998.

[50] X. W. Hu, A. P. Karmarkar, B. Jun, D. M. Fleetwood, R. D. Schrimpf, R. D. Geil, R. A. Weller, B. D. White, M. Bataiev, L. J. Brillson, and U. K. Mishra, "Proton-irradiation effects on AlGaN/AlN/GaN high electron mobility transistors," *IEEE Transactions on Nuclear Science,* vol. 50, pp. 1791-1796, Dec 2003.

[51] B. Jun and S. Subramanian, "Carrier-removal rate and mobility degradation in heterojunction field-effect transistor structures," *IEEE Transactions on Nuclear Science,* vol. 49, pp. 3222-3229, Dec 2002.

[52] L. Shen, S. Heikman, B. Moran, R. Coffie, N. Q. Zhang, D. Buttari, I. P. Smorchkova, S. Keller, S. P. DenBaars, and U. K. Mishra, "AlGaN/AlN/GaN high-power microwave HEMT," *IEEE Electron Device Letters,* vol. 22, pp. 457-459, Oct 2001.

[53] A. Y. Polyakov, N. B. Smirnov, A. V. Govorkov, S. J. Pearton, and J. M. Zavada, "Proton implantation effects on electrical and luminescent properties of p-GaN," *Journal of Applied Physics,* vol. 94, pp. 3069-3074, Sep 2003.

[54] A. Y. Polyakov, N. B. Smirnov, A. V. Govorkov, N. V. Pashkova, S. J. Pearton, J. M. Zavada, and R. G. Wilson, "Proton implantation effects on electrical and optical properties of undoped AlGaN with high Al mole fraction," *Journal of Vacuum Science & Technology B,* vol. 21, pp. 2500-2505, Nov-Dec 2003.

[55] H. J. Stein and R. Gereth, "Introduction rates of electrically active defects in N- and P-Type Silicon by electron and neutron irradiation," *Journal of Applied Physics,* vol. 39, pp. 2890-2898, 1968.

[56] S. T. Bradley, A. P. Young, L. J. Brillson, M. J. Murphy, and W. J. Schaff, "Role of barrier and buffer layer defect states in AlGaN/GaN HEMT structures," *Journal of Electronic Materials,* vol. 30, pp. 123-128, Mar 2001.

[57] A. Y. Polyakov, N. B. Smirnov, A. V. Govorkov, A. V. Markov, S. J. Pearton, N. G. Kolin, D. I. Merkurisov, and V. M. Boiko, "Neutron irradiation effects on electrical properties and deep-level spectra in undoped n-AlGaN/GaN heterostructures," *Journal of Applied Physics,* vol. 98, pp. -, Aug 2005.

[58] W. Lu, J. W. Yang, M. A. Khan, and I. Adesida, "AlGaN/GaN HEMTs on SiC with over 100 GHz f(T) and low microwave noise," *IEEE Transactions on Electron Devices,* vol. 48, pp. 581-585, Mar 2001.

[59] U. K. Mishra, P. Parikh, and Y. F. Wu, "AlGaN/GaN HEMTs - An overview of device operation and applications," *Proceedings of the IEEE,* vol. 90, pp. 1022-1031, Jun 2002.

[60] Y. F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "Very-high power density AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices,* vol. 48, pp. 586-590, Mar 2001.

[61] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical-simulation of nonplanar devices," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 7, pp. 1164-1171, Nov 1988.

[62] A. F. M. Anwar, S. L. Wu, and R. T. Webster, "Temperature dependent transport parameters in short GaN structures," *Physica Status Solidi B-Basic Research,* vol. 228, pp. 575-578, Nov 2001.

[63] A. F. M. Anwar, S. L. Wu, and R. T. Webster, "Temperature dependent transport properties in GaN, $A1_{(x)}Ga_{(1-x)}N$, and InxGa1-xN semiconductors," *IEEE Transactions on Electron Devices,* vol. 48, pp. 567-572, Mar 2001.

[64] L. Shen, "Advanced polarization based design of AlGaN/GaN HEMTs," 2004.

[65] J. W. Johnson, J. Han, A. G. Baca, R. D. Briggs, R. J. Shul, J. R. Wendt, C. Monier, F. Ren, B. Luo, S. N. G. Chu, D. Tsvetkov, V. Dmitriev, and S. J. Pearton, "Comparison of AlGaN/GaN high electron mobility transistors grown on AlN/SiC templates or sapphire," *Solid-State Electronics,* vol. 46, pp. 513-523, Apr 2002.

[66] J. M. Tirado, J. L. Sanchez-Rojas, and J. I. Izpura, "Simulation of surface state effects in the transient response of AlGaN/GaN HEMT and GaN MESFET devices," *Semiconductor Science and Technology,* vol. 21, pp. 1150-1159, Aug 2006.

[67] J. M. Tirado, J. L. Sanchez-Rojas, and J. I. Izpura, "Trapping effects in the transient response of AlGaN/GaN HEMT devices," *IEEE Transactions on Electron Devices,* vol. 54, pp. 410-417, Mar 2007.

[68] J. R. L. M.A.Mastro, N.D.Bassim,C.R.Eddy Jr, "Simulation on the effect of non uniform strain from the passivation layer on AlGaN/GaN HEMT," *Microelectronics Journal,* vol. 36, pp. 705-711, 2005.

[69] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. K. Mishra, C. Canali, and E. Zanoni, "Surface-related drain current dispersion effects in AlGaN-GaNHEMTs," *IEEE Transactions on Electron Devices,* vol. 51, pp. 1554-1561, Oct 2004.