SINGLE-EVENT CHARACTERIZATION OF DIGITALLY-CONTROLLED OSCILLATORS (DCOS)

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CHAPTER I

INTRODUCTION

I.1. Background and Statement of Research Problem

With the scaling of CMOS technology, the major issues being addressed in IC designs are low-cost, low-voltage, and low-power. Digital circuits are more favorable over other heterogeneous parts because of their abilities to be manufactured economically in high volumes. Recently, there has been an additional emphasis on integration of heterogeneous parts that constitute a communication transceiver [1] , such as the phase-locked loop based frequency synthesizers. Traditionally, a Voltage-Controlled Oscillator (VCO) is commonly used as the core part of a phase-locked-loop-based frequency synthesizer that generates high-frequency output signals through resonance. The frequency of the output signal of a VCO is under the control of the biasing voltage that is continuously applied to it. In the late 20th century, the concept of a digitally controlled oscillator (DCO) was proposed as the digital counterpart of a VCO. DCOs have only digital inputs/outputs (I/Os) operating in the discrete-time domain. Instead of using a control voltage, a DCO uses digital words to discretely change the output signal frequency, thus performing digital-to-frequency conversion. Since appearance, DCOs have drawn growing attention. All-digital phase-locked loops (ADPLLs), the digital counterparts of conventional charge-pump phase-locked loops (CPPLLs), have been applied in cell phones, bluetooth radio and other communication applications [9] [10].

A single-event (SE) effect occurs when a high-energy ionizing particle, such as a heavy ion, strikes a circuit. One type of effect resulting from SEs in an IC is a single-event transient (SET); SETs are undesirable asynchronous signals that can propagate through signal paths and result in a variety of circuit responses. Single-event effects (SEEs) have been a growing concern for the space, military, and commercial electronic sectors since

the 1970s [11]. Above all, the single-event vulnerabilities of clock circuits like Delay-Locked Loops (DLLs) and Phase-Locked Loops (PLLs) are of particular concern, as SETs occurring within a clock distribution system can result in global errors across the entire IC. In the past, there have been quite a few studies on SEE on traditional CPPLLs, including studies focusing on the core VCO part. Y. Boulghassoul et.al was one of the first group of researches to closely examine VCO circuit design topologies as examples to compare the single-event robustness over technology nodes in bulk Si-process[12]. Radiation responses of different types of VCOs were characterized and different methods against SEEs in VCOs were proposed later on in [4][13].

However, there has been no radiation-effect related research on DCOs so far. As the key building block of an ADPLL, a radiation-tolerant DCO is essential to preserve clock signals against SEEs in communication applications and potentially in military applications. The goal of this work is to perform a single-event characterization on different topologies of ring-based DCOs to provide designers guidance on designing rad-hard DCOs.

I.2. Overview of the Thesis

In Chapter 2, the definition and common structures of DCOs are discussed.

Chapter 3 is a background introduction chapter on the definition of Single-event Effects(SEEs) and SEEs in clock circuits.

Chapter 4 demonstrates the single-event error signatures in DCOs, and the related quantification metrics.

Chapter 5 illustrates the single-event harmonic error mechanisms in any ring oscillator circuits.

Chapter 6 goes on by illustrating the simulation setup. Simulation results on the designed DCO are demonstrated in this chapter, based on which analysis are provided to validate the proposed error mechanisms.

In Chapter 7, electrical testing data on discrete components are provided the support

the simulation results and harmonic theories.

In Chapter 8, the single event vulnerabilities of the two designed DCO topologies (capacitive-tuning topology and drive-tuning topology) are compared.

In Chapter 9, a rad-hard design requirement against SE harmonic errors is proposed and two techniques are implemented to validate the design requirement. Simulation results of the hardened designs are shown and design tradeoffs are discussed.

Chapter 10 is the conclusion chapter.

CHAPTER II

THE DIGITALLY CONTROLLED OSCILLATORS

Throughout the past decades, there has been a drastic trend of implementing analog functions in digital or digital-intensive circuits. ADPLLs have drawn growing attentions as a substitute of traditional charge pump phase-locked loops (CPPLLs). Although ADPLL cannot achieve as high frequency as its analog counterpart, it provides a faster lock-in time and better testability, stability, and portability over different process [2]. The DCO is a key component in an ADPLL, which is a replacement of the conventional voltage or current controlled oscillator for CPPLLs. They are more exible and usually more robust than the conventional VCO.

II.1. Circuit Topology Description

The principle to design a DCO is to make sure that the oscillation frequency f_{DCO} is linearly proportional to input control word D with an offset. Therefore, the oscillation frequency can be rewritten as

$$f = f_0 \pm \Delta f \cdot D, \tag{II.1}$$

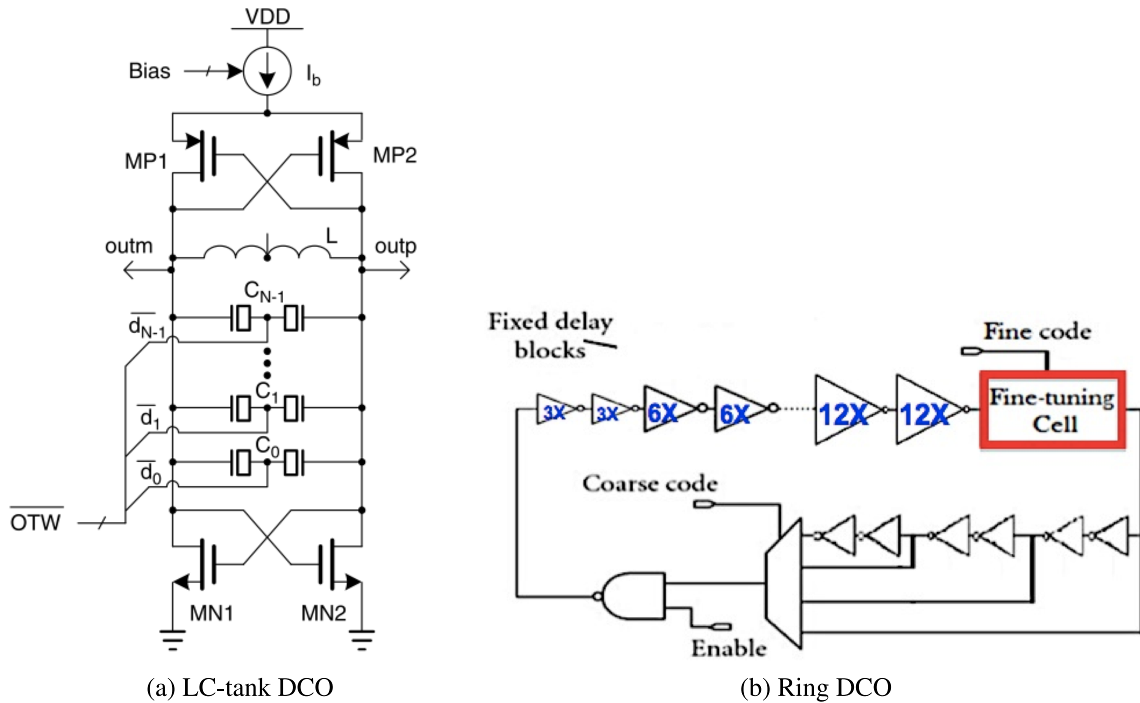
where Δf is the change of output frequency per LSB and D is an N-bit binary number $\overline{d_{N-1}d_{N-2}\cdots d_0}$,

$$D = 2^{(N-1)} \cdot d_{N-1} + 2^{(N-2)} \cdot d_{N-2} + \cdots + d_0 \tag{II.2}$$

where $d_{N-1}, d_{N-2}, \cdots, d_0$ are the digits in the binary number D [1].

Based on this principle, a DCO is commonly constructed of two major parts - the register for storing the digital word and the actual oscillator that generates a signal at the frequency corresponding to the word. DCOs are distinguished from one another by the actual oscillators, which are usually LC tank based or ring-based. The LC-tank oscillator is based on resonance between L and C components in the circuit. As shown in Fig. II.1a,

the oscillating frequency changes with digital control word because different number of capacitors are active in the capacitor bank corresponds to different control word to resonate with the inductor during circuit operation. On the other hand, in Fig. II.1b, the ring-based topology is based on the resonance of odd number of inverting gates tied in a loop fashion. Control words are applied to adjust the number of inverting gates in the ring or the delay of each inverting gate to manipulate the frequency of oscillation. Even though LC-tank based oscillators have good inherent phase noise performances, ring-based DCOs are chosen for the purpose of this work because they are more digital intensive in nature and easier to integrate.



(a) LC-tank DCO

(b) Ring DCO

Figure II.1: Different DCO structures: (a) LC-tank based DCO [1] (b) Ring-based DCO [2]

II.2. DCO Design Metrics

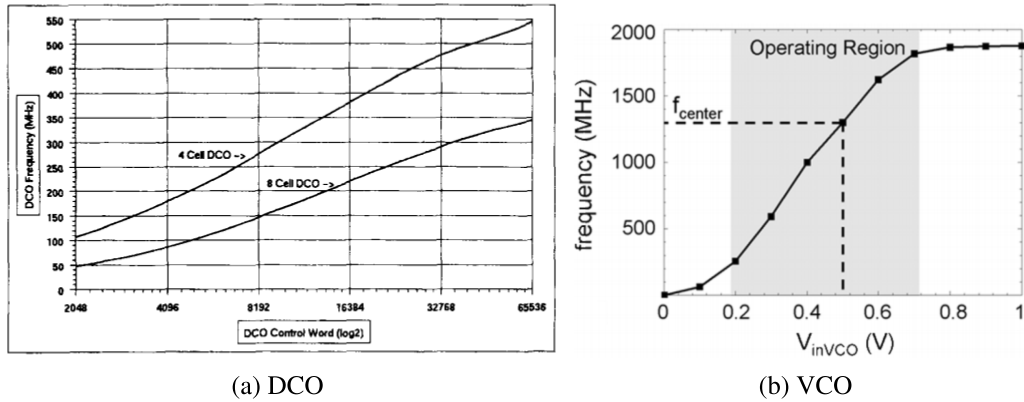
Frequency tuning range, tuning linearity and tuning resolution are three major design metrics of DCOs.

Frequency tuning range is defined as the frequency span from the minimum to the maximum control words.

$$\Delta f = f_{MAX} - f_{MIN} \tag{II.3}$$

Frequency resolution is the maximum frequency tuning step the DCO takes when the control word is being adjusted by 1 least significant bit (LSB) throughout the whole sweeping range, which is always in the unit of Hz/LSB.

Frequency tuning linearity is evaluated by whether the output frequency of oscillation changes linearly with the change of control word, i.e. whether the frequency resolution remains constant throughout the whole span of control words. DCOs could have drastically different frequency tuning linearities, but generally speaking, the better frequency tuning linearity the DCO is, the better. Fig. II.2a is an example of frequency versus control words for DCOs , which is usually used by researchers to illustrate or compare the electrical functionalities of DCOs. In conventional VCOs, frequency versus control voltages is always plotted as shown in Fig. II.2b.



(a) DCO (b) VCO

Figure II.2: (a) Frequency vs control words for DCOs [3] (b) Frequency vs control voltages for VCOs [4]

In addition, as with PLLs and delay-locked loops (DLLs), phase jitter, the amount of phase fluctuation of the output clock signal, is also a very important metric to evaluate a

DCO.

II.3. Custom DCO Design

According to the design principle mentioned above, for ring-based DCOs, the frequency/delay tuning is commonly implemented in one of the two or sometimes the combination of the two following ways: one is by changing the number of stages involved in the resonance; the other is by changing the delay of each stage, i.e. the resistance or the capacitance that is related to each stage. The former approach usually changes the output signal frequency in greater steps comparing with the latter one. Thus, in the literature, the former approach is used as coarse frequency controlling scheme, while the latter one is referred to as fine frequency controlling scheme.

The coarse controlling scheme is usually implemented in a fully-synthesizable manner. This could be simply achieved by using a control word to select different feedback paths in the ring oscillator through a multiplexers to alter the length of the ring as show in Fig. II.1b. However, only with coarse frequency controlling scheme would result in high frequency tuning non-linearity. This is because this tuning scheme is almost always implemented in such a way that an LSB increment /decrement in the control word is equivalent with a change of two inverters in the length of the ring to minimize the frequency tuning resolution.(Two inverters is the minimum change to maintain odd number of stages in the loop.) Thus, an LSB change in oscillation period ΔT is related with change in frequency Δf as illustrated in the following equation :

$$\Delta f = f_1 - f_0 = \frac{1}{T_1} - \frac{1}{T_0} = \frac{T_0 - T_1}{T_1 \cdot T_0} = \frac{\Delta T}{T_1 \cdot T_0} = \Delta T \cdot f_1 \cdot f_0 \tag{II.4}$$

As indicted in Eqn. II.4, the frequency tuning resolution changes quadratically with the operating frequency - the higher the operating frequency, the larger the frequency tuning resolution. Although [14] talked about using different inverter number changes per LSB in different operating frequencies to achieve good frequency tuning linearity, this imposes

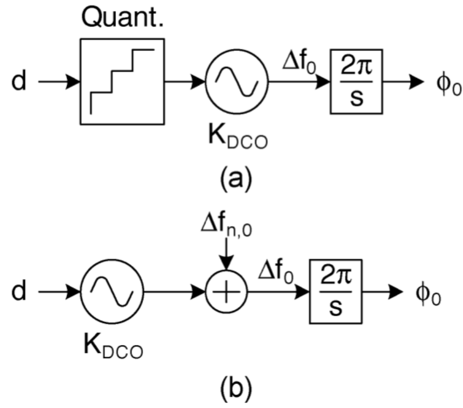


Figure II.3: DCO quantization noise model. [5]

both design and hardware complexities.

Linear frequency tuning of the DCO is commonly required when the DCO is used in the ADPLL. Because it guarantees low hardware complexity in the control circuit to calculate the control word corresponding to a certain oscillating frequency. In addition, according to quantization noise model from [5], shown in Eqn. II.5, left hand side $L_{\{\delta\omega\}}$ is the phase noise, Δf_{res} is the frequency tuning resolution of the DCO and f_R is the reference frequency of the ADPLL. For a given reference frequency, the larger the frequency resolution of the DCO, the higher the phase noise of the DCO and also the whole ADPLL.

$$L\{\Delta\omega\} = \frac{\Delta f_{res}{}^2}{12 f_R} \tag{II.5}$$

Thus adding a fine-tuning module to minimize the frequency tuning resolution becomes necessary. One of the most important design requirement when designing the fine-tuning module is that, for adjacent coarse words, the tuning range corresponding to the whole span of fine words should be slightly overlapping so that no frequencies are left out of the tuning range. Two common techniques are stated in the literature to accomplish fine frequency tuning. One technique changes the driving strength dynamically with fixed capacitance loading [15], which we shall call "drive-strength tuning" scheme in the future chapters. As

shown in Fig. II.4 (a), in this technique, the control word/inverted control word is applied to the headers/footers of the current starved inverter. Since each bit in the control word is binary weighted, the sizes of the headers and footers are binary weighted correspondingly. And the PFET/NFET in the middle of the headers and footers are the sizes of the headers/footers adding together to sustain the total current.

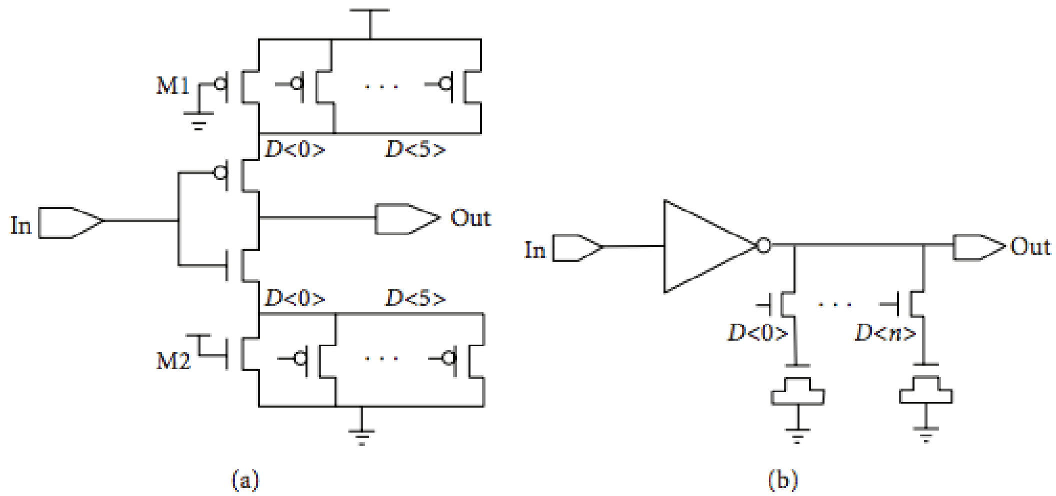


Figure II.4: Fine frequency tuning cell structures. (a) Driving-strength controlled (b) Shunt-capacitance controlled[2]

The other technique uses shunt capacitors to tune the capacitance loading[16], which we shall call "capactivie-load tuning" scheme in the future chapters. As illustrated in Fig. II.4 (b), the control word is applied to control a bank of switches to control the capacitor tank that is tied to the node. In this case, both the switches and the connected capacitors are sized according to binary weights because of the usage of binary control word. Combining both coarse frequency tuning scheme and fine frequency tuning scheme in the DCO leads to a good linear frequency resolution and a reasonable frequency operating range.

CHAPTER III

SINGLE EVENT EFFECTS IN RING OSCILLATORS AND INVERTER CHAINS

III.1. Definition of Single-Event Effects

III.1.1. Single-Event (SE)

A single event happens when either a charged or uncharged particle strikes a device and causes charge collection.

Direct ionization occurs when an ionizing particle passes through a semiconductor creating electron-hole pairs (EHPs) along its strike path until it has lost all its energy or left the semiconductor [7]. The primary ionizing particles of concern for space environment are heavy ions, protons, alpha particles and electrons.

Meanwhile, non-ionizing particles can cause“indirect ionization” by nuclear reactions resulted from particle collisions or generating secondary ionizing particles when striking the device. In the terrestrial environment, neutrons are the primary non-ionizing particles responsible for single-event radiation effects.

The metric linear energy transfer (LET) is commonly used to calculate the energy loss of the particle in the single event process. LET is the energy loss per unit length normalized by the density of the target material, typically described in units of MeV-$(cm)^2$/mg or pC/μm.

III.1.2. Single-Event Effects (SEEs)

The charge deposited by the particle is often collected by the circuit, resulting in a current transient that can lead to soft errors, depending on the circuit response, which is always referred to as single-event effects (SEEs). Depending on the position of the single particle strike, a single, high-energy particle can directly flip the stored state of a memory element, resulting in a SEU [17], or it can also cause a voltage glitch resulting in incorrect value being latched in the sequential logic, which is referred to as a SET. Based on whether

the result of the disruption in combinational logic or analog circuitry, an SET is distinctively called a digital SET (DSET) or an analog SET (ASET).

The concerns with SEEs have increased with modern-day integrated circuits (ICs) because they have been reported to show an increased susceptibility to SEE as feature sizes decrease and frequencies increase. Sensitive junctions within the material, usually reverse-biased p/n junctions, can collect these extra carriers causing harmful effects, such as, erroneous pulses and even complete failure of the device, based on the circuit topology and the amount of charge collected[7].

III.2. Single-Event Circuit Simulation

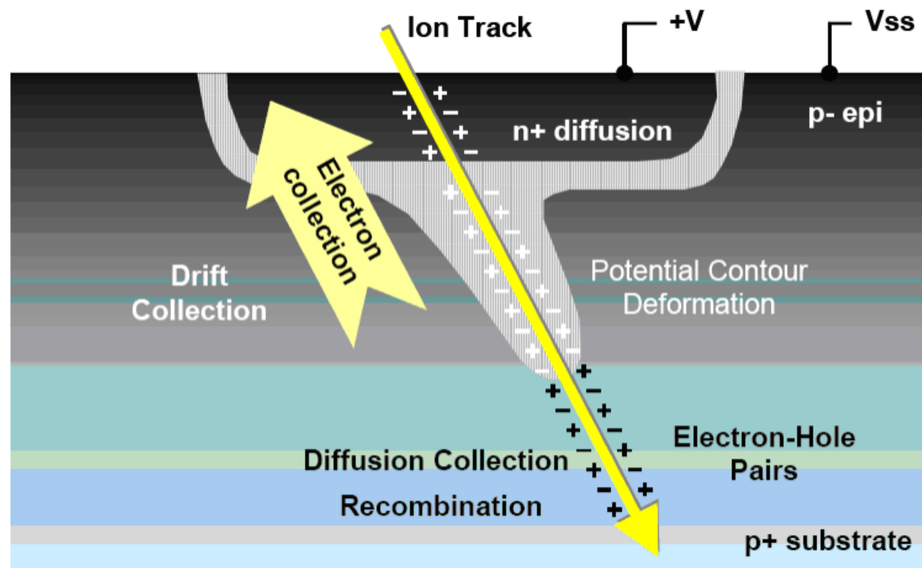


Figure III.1: Illustration of an ion strike on a reverse-biased n+/p junction[6]

After charge is generated from the particle strike, two major mechanisms are involved in charge collection - drift and diffusion. As illustrated in Fig. III.1, near a p-n junction, the built-in electric field causes drift current holes and electrons to be swept into the p- and n-regions, respectively. This current is only present for a picosecond-scale time period, and is limited by the number of excess carriers in the material [18]. On the other hand, in the absence of an electric field, but within a diffusion length of a junction, the diffusion process

dominates. This process takes on order of hundreds of picoseconds to nanoseconds. The effect of a SE with respect to time involves fast (drift) and slow (diffusion) components as illustrated in Fig. III.2. The total charge is the integral of the current over time [7].

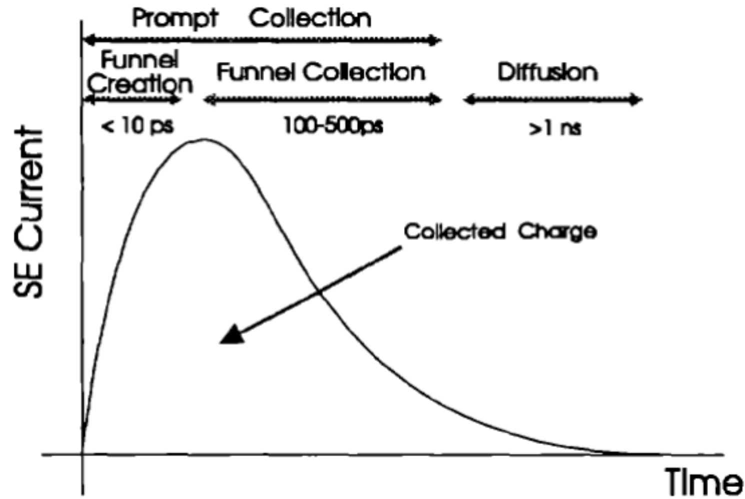


Figure III.2: Diagram of a typical transient resulting from an ion strike on a reverse-biased n+/p junction [7]

Current-based models have been used for many years to emulate the charge generated during a SE strike on a device in a circuit. Originally, a double-exponential current source was used [7], then a technology computer-aided design (TCAD) calibrated model [19] was implemented. More recently, a voltage-dependent current source model has been developed to accurately simulate the characteristics of an ion strike, shown in Fig. III.3 [20]. The voltage-dependent model is the primary SEE model used in this work.

III.3. SET Generation and Propagation in ROs and Inverter Chain Circuits

Although there has been no research conducted on radiation performance analysis of DCOs, this work was built upon previous results on similar circuits, such as inverter chains and ring oscillators (ROs). This work aims to explore the single-event-induced harmonic mechanism in DCOs, and provides a technology-independent analytical model that may be used to determine the sensitivity any RO structure to a single-event (SE) harmonic response.

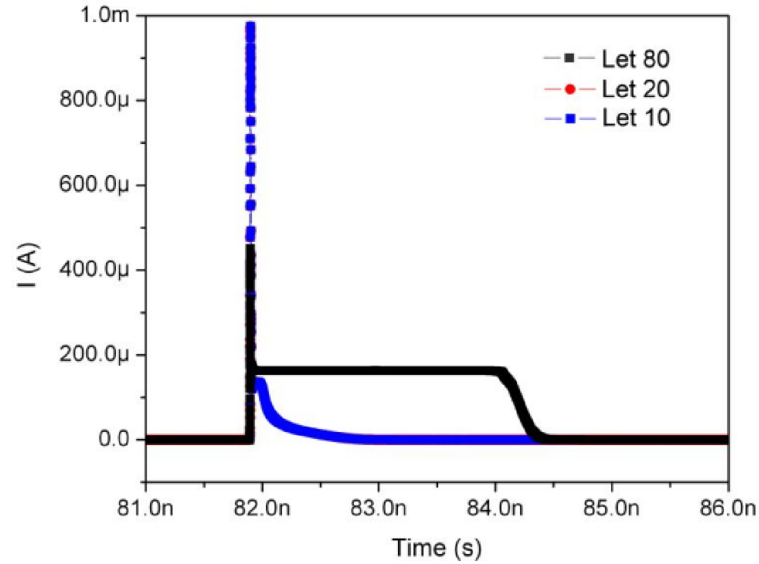


Figure III.3: Ion-induced current profiles obtained from 3D TCAD models for LET values of 10 MeV-$(cm)^2$/mg, 20 MeV-$(cm)^2$/mg and 80 MeV-$(cm)^2$/mg.

III.3.1. Inverter Chains

A portion of SEUs are induced by SETs generated in combinational logic elements being latched in the sequential logic elements. With the increasing of circuits' operating frequency, studies have shown that it has become more and more likely for SEUs to be induced by SETs latched in the memory elements than SEU of the memory element themselves [21]. Over the years, inverter chains have always been the favorite test structure of researchers to study SET generation and propagation, because of its simplicity in constructing, data collecting and analysis.

Throughout the years, researchers have done extensive studies. Massengill et.al has given a review in [22] on different conditions when SET pulses would be attenuated or broadened. Analytical method was used in [23] to carefully deduce the criteria for SET pulse to propagate in inverter chains. Specifically, it was mentioned in the paper that SET pulses could be attenuated due to inverters of different drive strength/capacitive loading in the chain. The theories mentioned above are the basis of analysis of SET pulse propagation

in ring-based DCOs consisting of inverters.

III.3.2. Ring Oscillators (ROs)

In [8], the authors claimed to have witnessed all $3^{rd}, 5^{th}$ and 7th harmonic oscillating signals induced by a single particle strike. M. Casey further analyzed that higher harmonic oscillation is also possible to be introduced to ROs by manipulating the power supply and enable voltage when the laser beam was blocked. And that harmonic is more likely to occur in ring oscillators with a large, odd number of stages than with a small or even number. This work further explores the error mechanism and provides a technology-independent analytical model that may be used to determine the sensitivity any RO structure to a SE harmonic response.

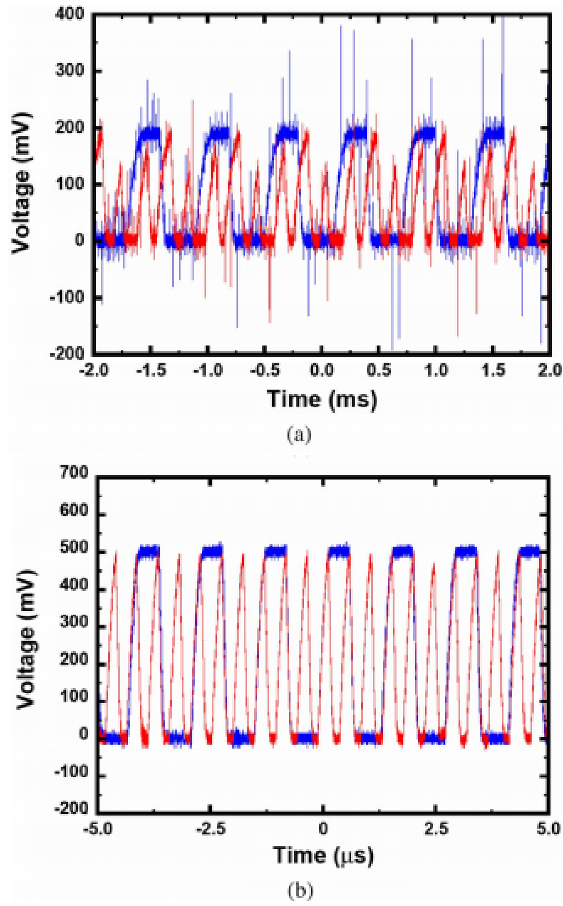


Figure III.4: Change of frequency due to laser strikes in a 201-stage ring oscillator operating at (a) 200 mV and (b) 500 mV. The blue (red) curves are pre-strike (post-strike) oscillator outputs.[8]

CHAPTER IV

ERROR SIGNATURES AND QUANTIFICATION IN DCOS

As previously stated, DCOs are consisted of two major parts, namely the register and the actual oscillator. A single particle strike could result in either SEUs in the memory elements or SETs in the actual oscillator. We categorize the errors following an ion strike on a DCO into two categories based on these two mechanisms: SEU-induced errors and SET-induced errors.

IV.1. SEU-induced Oscillating Frequency Error

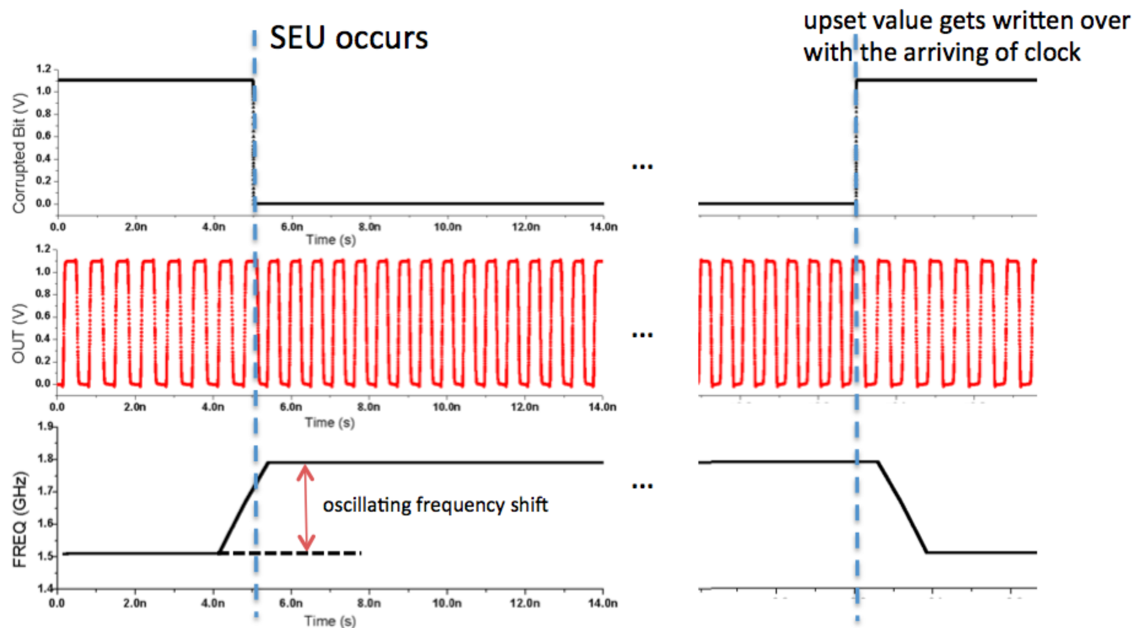


Figure IV.1: SEU induced oscillating frequency error.

Flip-flops (FFs) with master-slave structures are typically used in the registers to store the control words in DCOs. If the particle strike happens in the slave latches, it could only affect the output of the FF when the latch itself is in the transparent phase. In this case, the SET would directly be shown on the output. The latch would recover quickly if the voltage

disturbance is small. However, if the latch is corrupted from a large voltage disturbance, the control word would not be restored until the next clock cycle when a new value is written. The other case is when the strike happens in the master latch. Like in the previous case, the master latch could only be corrupted when it is transparent. Although the slave latch is opaque in this case, the wrong bit value could be latched in the slave latch for the next whole clock cycle until the new value is written into the FF.

In both of these cases, as depicted in Fig. IV.1, the perturbed bit causes the output signal to oscillator to oscillate at a different frequency until a new value is written into the FF with the arrival of the next clock edge. Depending on the system clock frequency (in the KHz∼MHz range for a typical ADPLL), according to which the digital control word is refreshed, the output frequency of the oscillator could be corrupted for more than 10 ns. In addition, if the corrupted bit is the most significant bit (MSB), the output frequency deviation of the DCO from the expected value could be as large as the half of the frequency tuning range, which would cause the PLL system to go through the locking cycle, including both frequency and phase tracking, if it is implemented in an ADPLL.

IV.2. SET-induced Errors

When a single-particle strike happens in the actual oscillator, three different types of transient errors can occur from the resulted SET: erroneous (missing) pulses, duty cycle errors and harmonic errors.

IV.2.1. Error Signatures

IV.2.1.1. Duty Cycle and Missing Pulse Errors

Duty-cycle errors refer to cases when the logic HIGH/LOW pulse widths differ from the original signal resulted from voltage perturbations. Similarly, missing pulses represent the case when one or more pulse(s) are absent from the output. These error signatures have been reported in clock circuits like CPPLLs and DLLs[24][25]. As shown in Fig. IV.2, these types of transient errors are usually not persistent, but they can affect the original

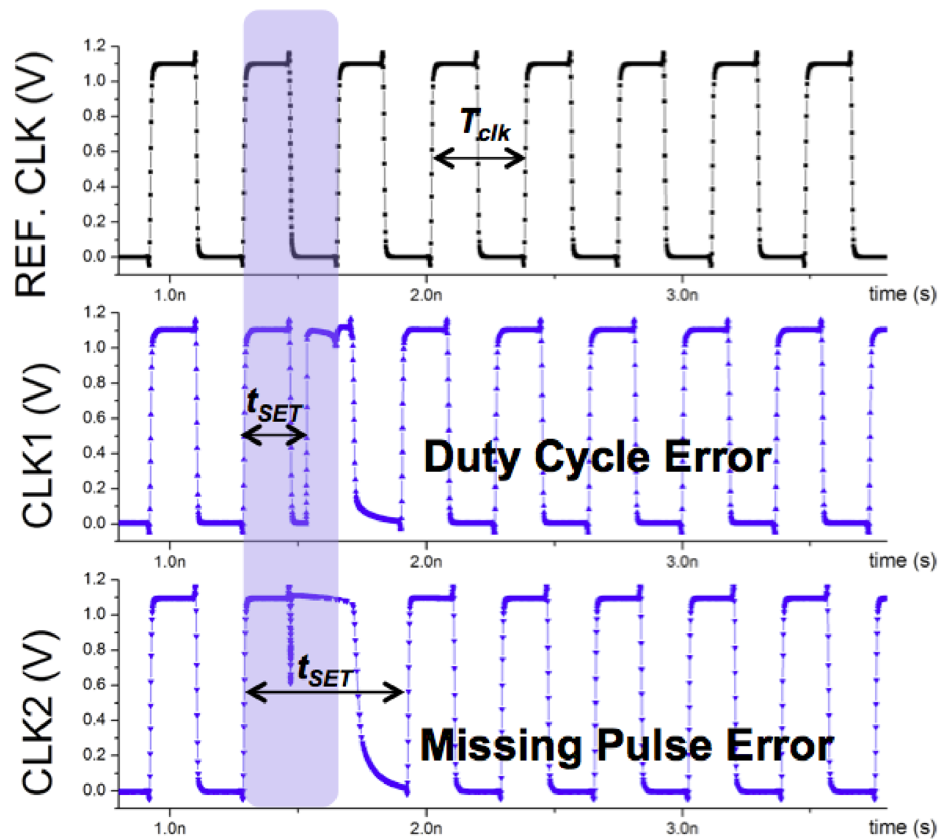


Figure IV.2: Single-event induced duty cycle error (middle) and missing pulse error (bottom) in reference to the unperturbed clock (top)

signal by shifting the signal in phase.

IV.2.1.2. Harmonic Errors

SE Harmonic errors are additional pulses induced by single-event transients (SETs) in each clock cycle, as illustrated in Fig. IV.3. They would result in the oscillator operating at a harmonic frequency, thus data corruption in the system dependent on it. As opposed to missing pulse errors, harmonic errors can persist for many clock cycles. Consecutive erroneous (additional) pulses will result in accumulated phase deviation from the unperturbed clock.

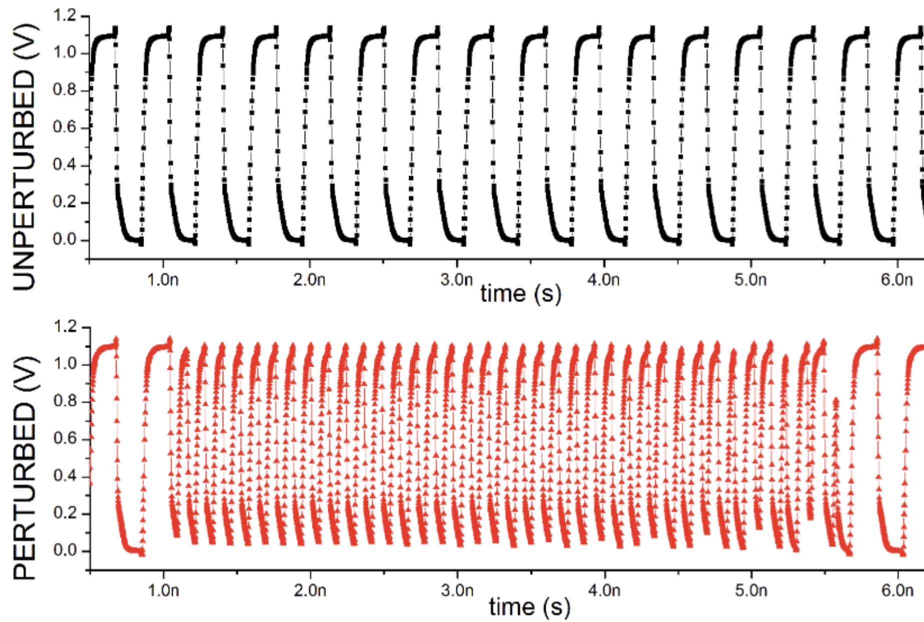


Figure IV.3: Single-event harmonic error persists for many clock cycles

IV.2.2. Error Quantification

Phase displacement metric has been used to quantify missing pulse and duty cycle errors[24][25]. It is a metric that represents the phase difference between the erroneous rising (or falling) edge of oscillating output and the previous normal rising (or falling) edge, normalized by the average period of this signal. By quantifying and comparing the

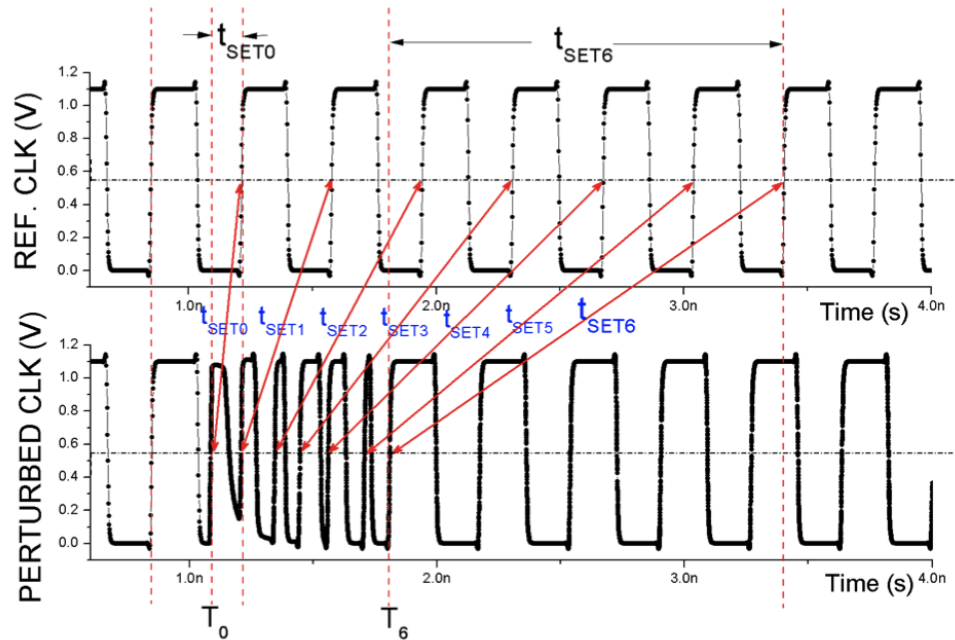
worst-case phase displacement shown on the output signal resulted from single-event strike on each component of the DCOs, the single sensitivity of them to the single-event induced missing pulse and duty cycle errors can be analyzed.

In this work, we propose the accumulated phase error metric to quantify the SE harmonic errors. The frequency and timing error of the harmonic oscillation, which are important for applications with strict phase noise and jitter requirements, may be extracted directly from accumulated phase error. Figures provided in this section are examples to illustrate the metric.

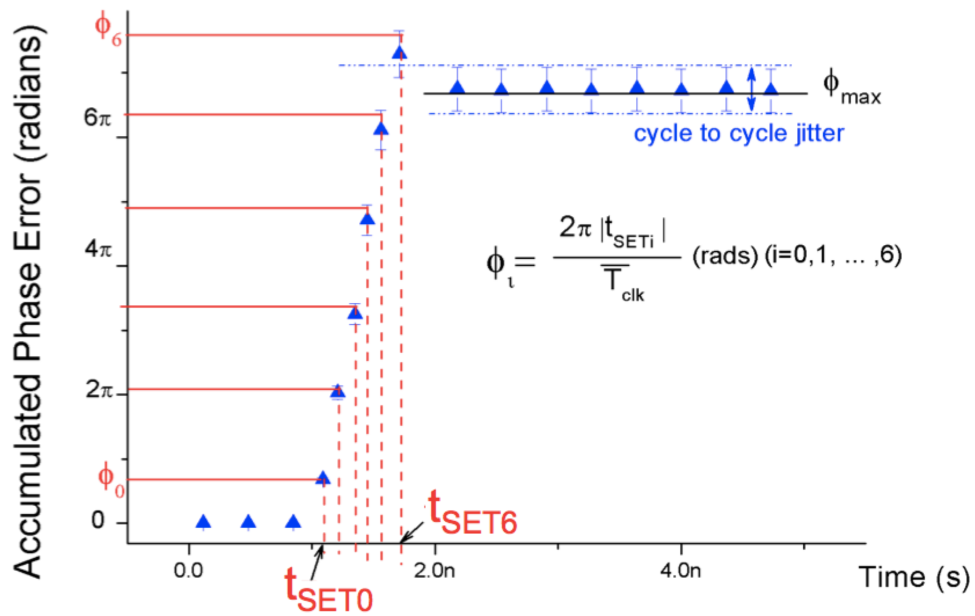
Each erroneous pulse in a perturbed clock corresponds to a certain time error, i.e. phase displacement, when compared with the unperturbed (reference) clock [6]. In the case of harmonic errors, as illustrated in Fig. IV.4a, the time difference t_{SETi} (i=0,1,$\cdots$,6) accumulates with the previous time difference $t_{SET(i-1)}$, thus the phase displacement, ϕ_i , corresponding to each t_{SETi} is cumulative with time, as plotted in Fig. IV.4b. Since the signal eventually settles back to the original clock period, the accumulated phase difference between the two signals would eventually become constant. Taking cycle-to-cycle jitter into consideration, we define the average of the final constant phase difference ϕ_{MAX}, the maximum accumulated phase difference due to the SE hit. Fig. IV.5 illustrates that different collected charge would result in different maximum accumulated phase difference ϕ_{MAX}.

The mathematical relationship between ϕ_i and t_{SETi} is illustrated in Eqn. IV.1, in which T_{clk} is the average clock period without any perturbation and the absolute value of t_{SETi} is used. While harmonic errors would usually result in positive t_{SETi}, duty cycle or missing pulse errors could sometimes lead to negative t_{SETi}.

$$\phi_i = \frac{2\pi|t_{SETi}|}{T_{clk}}(i = 0, 1, \cdots, 6) \tag{IV.1}$$



(a) t_{SETi}



(b) ϕ_i

Figure IV.4: The time differences t_{SETi} between the rising edges of the perturbed and unperturbed clock (a) and phase differences ϕ_i corresponding to them (b).

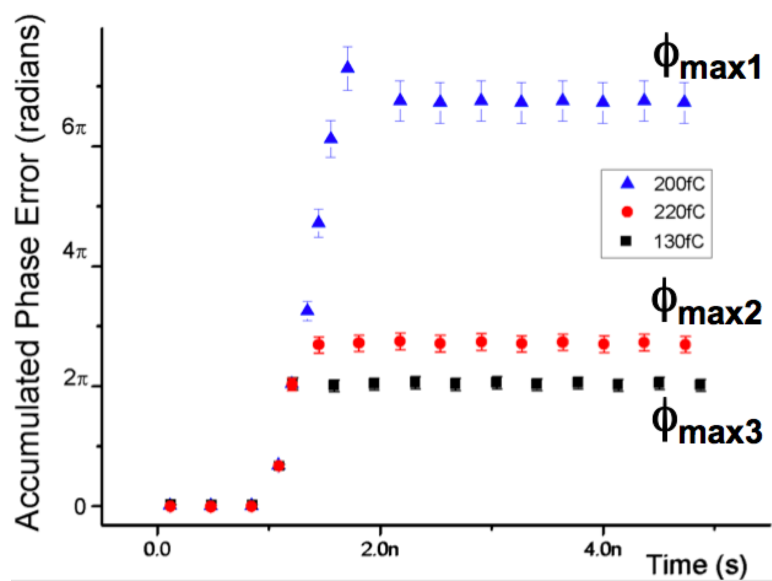


Figure IV.5: The maximum accumulated phase error for different collected charge values.

CHAPTER V

ERROR MECHANISMS IN ROS

V.1. General description

The operation of ring oscillators forces most nodes to be either high or low, but there will always be at least one node that is in a transition state [26]. In another words, If there is only one transition state in the ring at any given time, the frequency of oscillation is fundamental. In fact, this transition usually corresponds to the transition introduced through the extra input of NAND gate to start up the oscillation.

When a single-event voltage perturbation happens to a certain node in the oscillator, there are two clock edges - the perturbing transition and the recovering transition - being injected into the circuit. Assuming there is a conflict between the two new transients and the original clock edge, because the two injected transients are the opposite of each other, one of them could potentially overlap the previous or the following clock edge, which would result in only one transient again. This leads to missing pulse or duty cycle errors, where changes of phase other than frequency takes place in the oscillating signal. In another case where both transitions are intact upon injected into the circuit, the three transients would start to propagate in order throughout the ring. Therefore, three transitions in a clock cycle would be observed at the output, which is what we define as harmonic errors.

When m single-event pulses, i.e. 2m clock edges, are injected to the system, and if the clock edges are evenly spaced throughout the ring, the oscillating clock period would be shortened to $\frac{1}{2m+1}$ of the original period. Thus the perturbed signal would be the $(1+2m)^{th}$ harmonic frequency.

This explains why 3rd, 5th and 7th harmonic oscillating signals were witnessed in [8] from SET. It is quite likely that the frequency of the laser strike (single event strike) was on the same order with the oscillating frequency of the RO under test. Multiple SETs

were caught in the duration of harmonic error, causing the frequency to jump from the fundamental frequency to the 3rd, 5th, and then 7th harmonics.

If the clock edges are not evenly spaced, the frequency of oscillation would fluctuate with time but average around the frequency of the $(1+2m)^{th}$ harmonic. The odd harmonics and only the odd harmonics are stable for ring-based oscillators because that the Fourier transformation of original square wave includes only odd harmonics[26]. In this thesis we consider the case where only one node in the circuit is collecting charge at one time due to a single particle strike. Hence, without further illustration, the presented simulation results and experimental data are about 3rd harmonic oscillation resulted from a single pulse injection into the system.

V.2. Harmonic criteria

Assume the RO is constructed with n gates with propagation delays of $t_{d0}, t_{d1}, ..., t_{dn}$. The original(fundamental) frequency of the oscillation of this RO (f) is inversely proportional to the total time delay of the ring(T):

$$f = \frac{1}{T} = \frac{1}{2 \cdot (t_{d0} + t_{d1} + ... + t_{dn})} \tag{V.1}$$

$$t_{dmax} = max\{t_{d0}, t_{d1} ... t_{dn}\} \tag{V.2}$$

In addition to the criterion of injecting two edges into the system, the originating SET pulse width has to satisfy the following conditions for harmonic errors to occur from an SE strike at the output of the RO:

1. The pulse width of the SET (t_{SET}), measured at full-width half-rail, should be greater than the largest gate propagation delay (t_{dmax}) in the ring, as shown in Eqn. V.3.

$$t_{dmax} < t_{SET} \tag{V.3}$$

2. t_{SET} should be smaller than the total loop delay (T) subtracted by 2 times of the

t_{dmax}, as shown in Eqn. V.4.

$$T - 2t_{dmax} > t_{SET} \quad \text{(V.4)}$$

The two criteria above, which we call "harmonic criteria", confine the SET pulse width to be within a pulse width window in order to result in harmonic errors. If the criteria are not met, the SETs would result in duty cycle errors or missing pulse errors.

The mathematical analysis of the harmonic criteria roots from the criteria for pulse propagation in logic gates[22]. If the originated SET pulse width is smaller than the largest gate propagation delay (t_{dmax}), the SET will not be able to propagate through the ring. In this case, the voltage perturbation will be absent in the next half of clock cycle, as shown in Fig. V.1. Depending on the circuit design asymmetry, the pulse width of the minimum SET pulse ($t_{SET(min)}$) may be significantly larger than t_{dmax}. Therefore, criterion 1 is the lower limit of the SET pulse width that can induce harmonic errors, as illustrated in Fig. V.1.

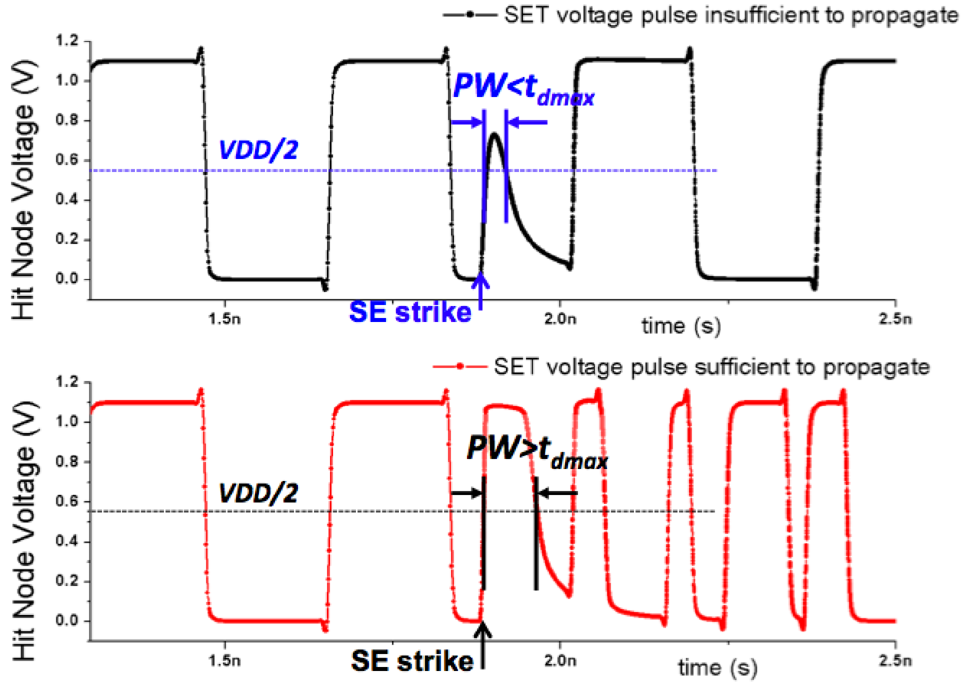


Figure V.1: SET pulse width on the verge of propagate through the ring.

As collected charge due to an ion strike increases, the SET pulse width will increase

such that either time segment t_a or t_b (shown in Fig. V.1) will become smaller than $t_{SET(min)}$. For such a case, time segments t_a and t_b represent the voltage pulse between the edges of the SET pulse to the previous and following clock edges. Since these pulses are smaller than $t_{SET(min)}$, they will be filtered out during propagation. As a result criterion Eqn. V.4 could be mathematically expressed as :

$$t_{SET(max)} < T - t_a - t_b < T - 2t_{dmax} \tag{V.5}$$

Eqn. V.5 also indicates that, depending on the striking time of the particle in reference to the oscillation period, the upper limit of the pulse width would shift around. However, it is bounded by the upper limit of $T - 2t_{dmax}$.

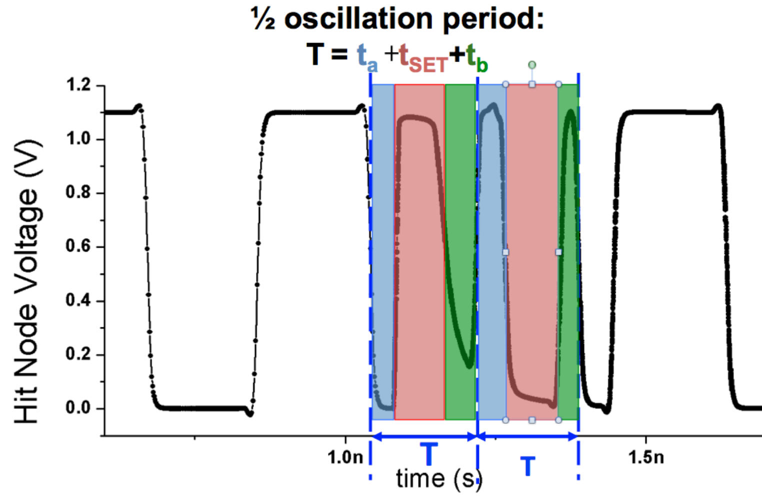


Figure V.2: SET pulse breaks the half of clock period into three parts a_1 and t_{set1}.

To sum up, both criteria need to be satisfied for harmonic errors to occur at the output node of the RO:

1). The SE perturbation must introduce two additional clock edges within half the oscillation period.

2). The single-event pulse width should be with in a time window, as illustrated in the

following equation:

$$T = t_{d0} + t_{d1} ... + t_{dn}, \tag{V.6}$$

$$t_{dmax} < PW_{SET} < T - 2t_{dmax}, \tag{V.7}$$

in which $t_{d0}, t_{d1} ... t_{dn}$ are the propagation delays of the n different delay stages in the ring, and T is the total propagation delay.

CHAPTER VI

HARMONIC ERROR VERIFICATION WITH SIMULATION RESULTS

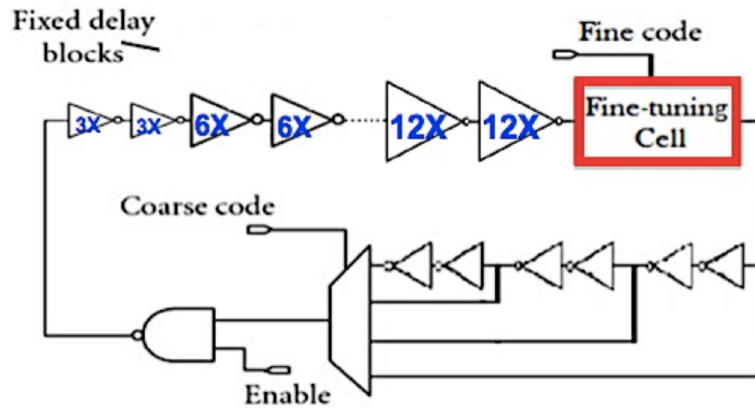
VI.1. Simulation Setup

Two ring-based DCO topologies were designed and laid-out in the UMC 40 nm bulk CMOS technology. As shown in Fig. VI.1, both DCOs incorporate the same coarse frequency tuning scheme by using a multiplexer to change the number of delay stages in the ring. The designs are differentiated by the fine frequency tuning schemes: one uses the drive-strength fine-tuning cell based on current-starved inverter delay and the other uses capacitive-load fine-tuning cell based on RC phase delay [2]. Fixed delay blocks are utilized in both topologies as buffers for the fine-tuning cells.

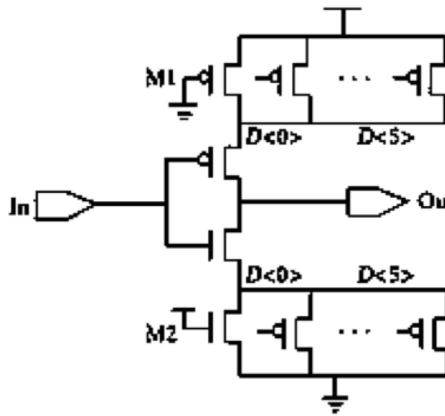
Both DCOs are designed to have a similar electrical performance. Since both designs have the same number of bits for their control words, the same coarse and fine frequency tuning range result in the same frequency tuning resolution for both designs. Fig. VI.2 illustrates a comparison of the electrical performances of the two DCOs by their frequency tuning range, which is a similar frequency tuning range of 2.5 GHz to 3.5 GHz at the nominal process design corner. After parasitic extraction, the frequency tuning range degrades (to1.5 GHz$\sim$2 GHz) for both designs. Simulation results on the DCO designs exhibit the same error signatures with or without parasitic extraction, as illustrated in Fig. VI.3. But their sensitivities ranges would be different. The SET simulation results presented in this thesis were acquired without parasitic extraction.

SET simulations were performed on two DCO designs using ISDE's bias dependent current model [20]. The current profile is injected to every node in the circuits over the clock period to determine the error signatures and worst-case SET responses of the output oscillating signal.

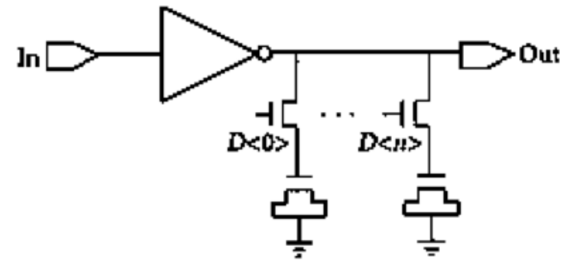
For both DCO topologies, the pull-up and pull-down networks of each circuit element



(a) Coarse tuning scheme



(b) Drive tuning fine scheme



(c) Capacitive tuning fine scheme

Figure VI.1: Two DCO designs: (a) Same coarse frequency tuning scheme (b) Drive tuning fine scheme (c) Capacitive tuning fine scheme. [2]

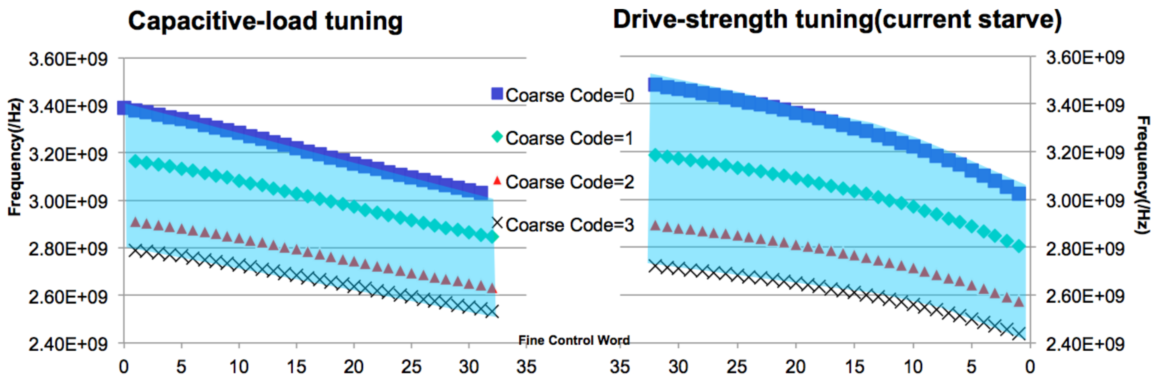


Figure VI.2: Electrical performance comparison of two DCOs.

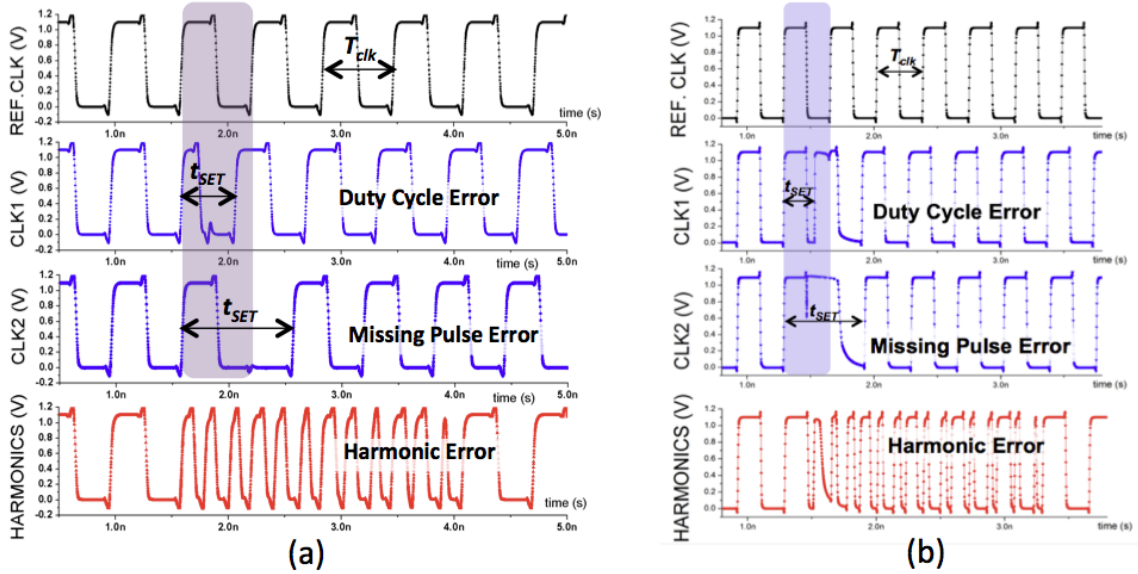


Figure VI.3: SET-induced error signatures simulation with (a) or without parasitic extraction (b) with the same control codes. The operating frequency degrades from 2.7GHz to 1.55GHz with parasitic extraction.

are sized to have approximately the same drive strength. The SET simulation is done on both PFETs and NFETs of all the circuit elements (including inverters, NAND gates and multiplexers) in the circuits. Since the results are similar with PFETs and NFETs, the results presented are based on strikes on PFETs in this thesis without loss of generality. In addition, since the performance of the DCOs under multi-node charge collection could be deduced from the scenario of single-node collection, the SET simulation in this work is conducted based on the assumption of only one node in the circuit is collecting charge at one time.

VI.2. SET Pulse Width Window

Fig. VI.4a illustrates the maximum accumulated phase error (ϕ_{MAX}) plotted over versus the initial voltage SET pulse width for strikes on an inverter sized to have 12 times the minimum drive strength (12x). A 12x inverter is selected as an example since every logic gate behaves similarly in the DCO in simulation. Comparing Fig. VI.4a with Fig. VI.4b, it

is seen that the SET pulse width window of a node downstream is narrower than that of the node under single event struck due to pulse attenuation.

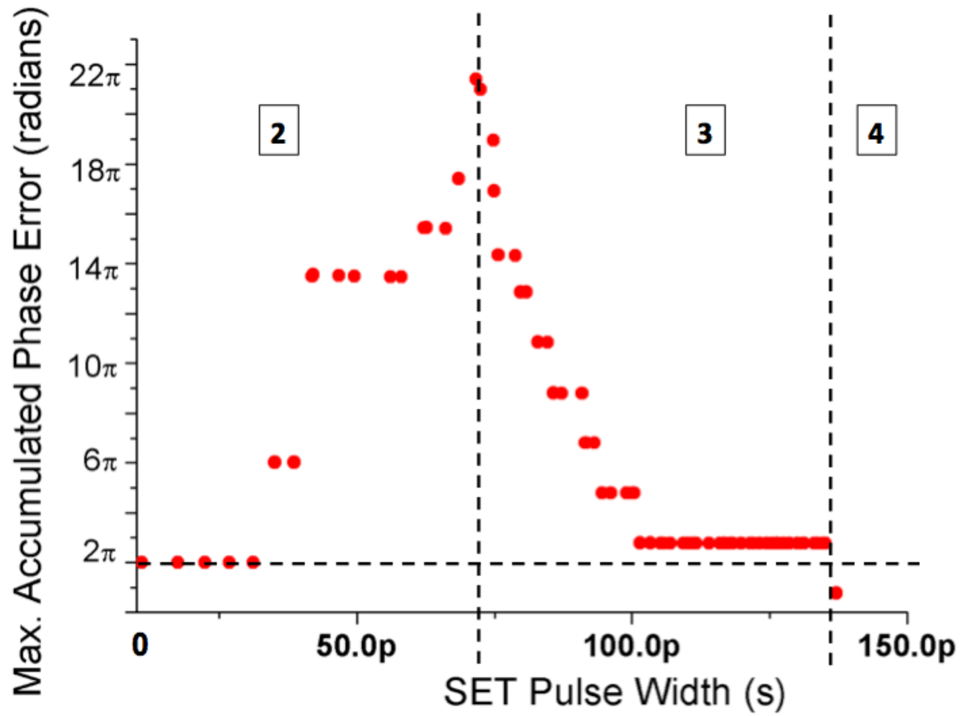
A harmonic response is determined to occur if the ϕ_{MAX} exceeds 2π radians of phase error (indicating at least one additional clock edge within the nominal cycle) at the output node, as indicated in region 1,2 or 3 of Fig. VI.4b. As Region 1 represents the onset of the harmonic response, though quickly attenuated, where the SET pulse width meets or exceeds the minimum pulse width ($t_{SET(min)}$) in order to result in 2π radians of accumulated phase error. Region 2 represents the values of SET pulse widths that result in a sustained harmonic. Region 3 represents the region of declined harmonic sensitivity. And when the SET pulse width exceeds $t_{SET(max)}$ or $t_{SET(threshold)}$, as shown by region 4 of Fig. VI.4b, the second edge of the initial SET pulse merges with the following clock edge and becomes a duty-cycle/missing pulse error.

VI.3. Verification of the Error Mechanisms with Simulation Results

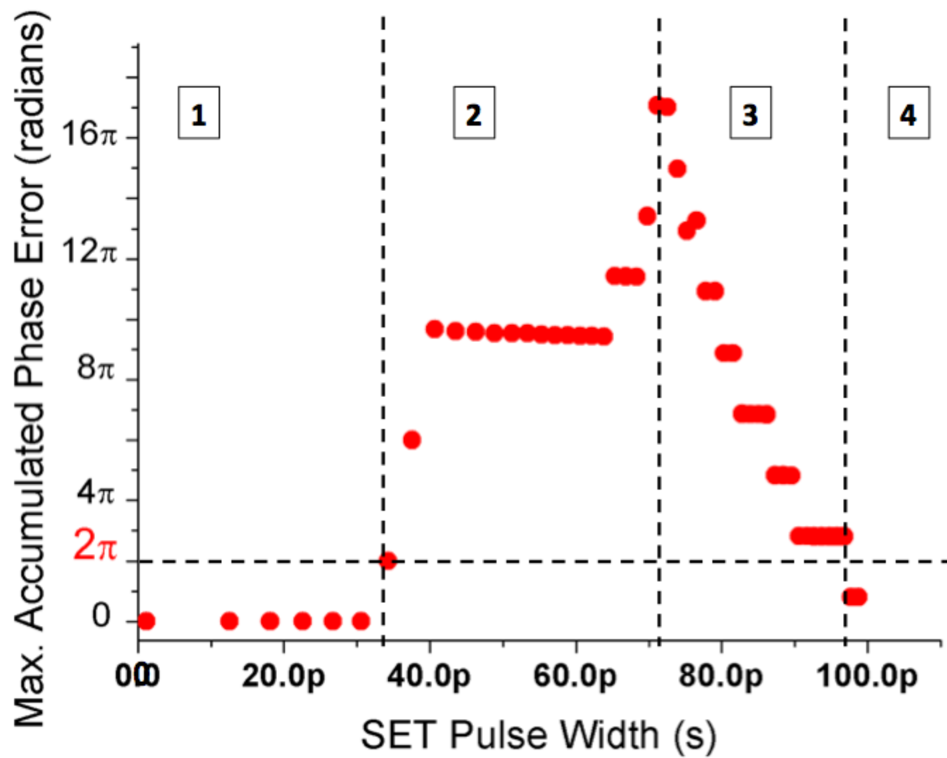
The proposed harmonic criteria state that if and only if the originated SET pulse width is within the lower and upper limits of the pulse width window, would the harmonic errors occur. The harmonic criteria are verified with the designed DCOs with the following methods:

1). Verify the lower limit of the pulse width window by varying locations of single particle strike while fixing control codes for the DCO: Since the structure of the DCO circuit is fixed by fixing the coarse and fine control codes, varying the particle strike locations should not change either the lower limit or the upper limit of the pulse width window, if the harmonic error mechanism holds true.

2). Verify the upper limit of the pulse width window by changing the coarse control code while keeping the same striking location: The number of stages in the ring changes with the changing of coarse control code. Thus the upper limit of the pulse width window should change with the changing of total loop delay, if the harmonic error mechanism holds



(a) SET pulse window of the hit node



(b) SET pulse window of the output node

Figure VI.4: The SET pulse width window at the hit node (a) and at the output node (b) of the DCO for a 12x inverter.

true.

3). Collected charge window is translated into pulse width window for each logic gate by measuring the output SET voltage pulse width at mid-rail resulted from a known collected charge deposited by the ISDE bias dependent current source[20].

Simulation conducted on both DCO topologies showed similar results. The results not only verified the correctness of the proposed mechanisms, but also provided insights on the single-event performance of the DCOs in different conditions. Following analysis is based on simulation results of the capacitive-tuning DCO .

VI.3.1. Verification On the Lower Limit of the Pulse Width Window

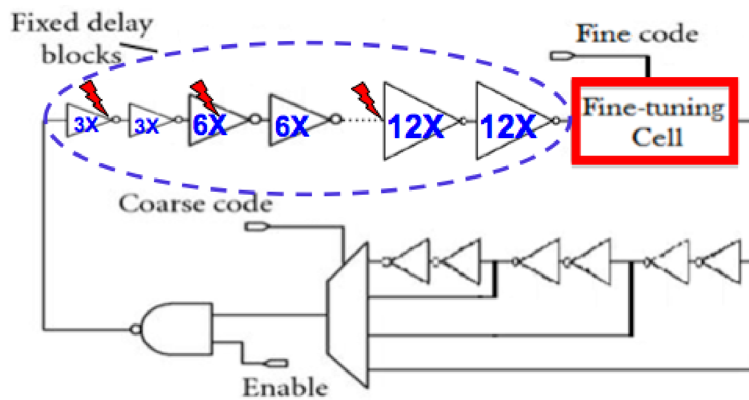


Figure VI.5: Single event particle strikes at different locations with fixed control codes in the drive-tuning DCO.

The capative-tuning DCO consists of inverters of different sizes, as shown in Fig. VI.5 above. Inverters with the sizes of 3, 6 and 9 times the minimal size in the technology, which would be named by “3x, 6x and 12x inverter” in the following text, are selected to analyze the collected charge windows of different components in the ring with fixed control codes. Plotted in Fig. VI.6a is the maximum accumulated phase error over collected charges for single-event strikes on these three inverters when the control codes bias the DCO to operate at 2.97 GHz. The simulation results are collected at the same output node for those different strikes.

According to Fig. VI.6a, the required collected charge to generate harmonic errors increases with the effective W/L ratio. On a system level, if gates of different sizes are used in the ring, a wide range of collected charge could result in harmonic errors.

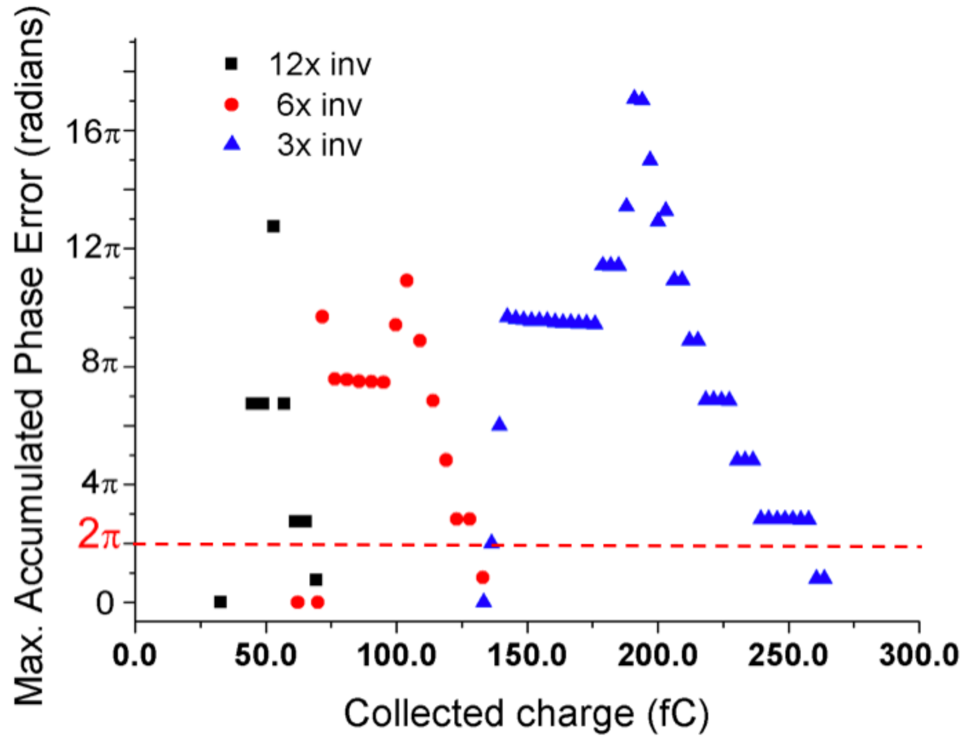
By measuring the SET pulse widths corresponding to the collected charges at the hit nodes, Fig. VI.6a can be replotted as Fig. VI.6b, in which the maximum accumulated phase errors are plotted over SET pulse widths. Fig. VI.6b shows that the upper boundary (around 98 ps) and lower boundary (around 38 ps) of the SET pulse width window (when the maximum accumulated phase error reaches 2π) are the same for the 3x, 6x and 12x inverters. That is to say, even though inverters of different sizes exhibit different ranges of collected charges to lead to harmonic errors, the corresponding ranges of SET pulse widths were almost the same.

The stage delay of each element in the capacitive tuning DCO is listed in the APPENDIX. The fine cell has the largest propagation delay because of the capacitive bank loading. The simulation result of input and output signals of the fine cell (under the same bias as in Fig. VI.5 and Fig. VI.6) is shown in Fig. VI.3.1.. The propagation delay from the input to the output is measured with the following equation for multiple times and an average number of 11.3ps was calculated:

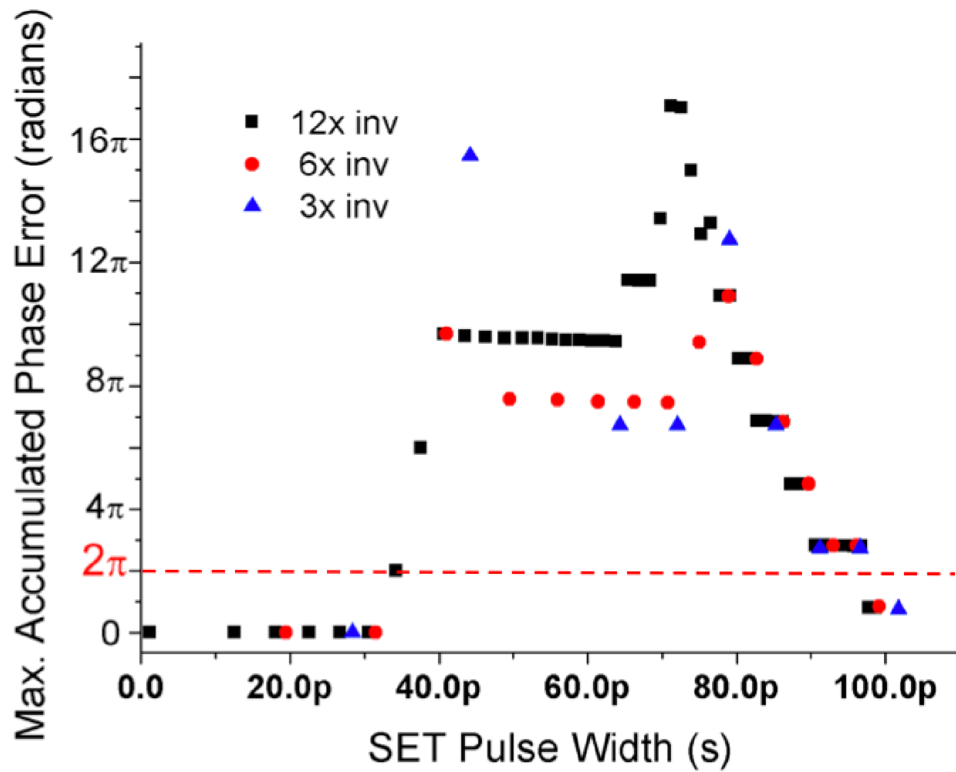
$$t_d = \frac{t_{PLH} + t_{PHL}}{2}, \tag{VI.1}$$

in whicht_d is the propagation delay time and t_{PLH} and t_{PHL} represent the propagation delays for a high-to-low, and a low-to-high transition, respectively, which is the time interval between the 50% VDD input and output voltages[27].

As a result, according to criteria Eqn. V.3 presented earlier, the smallest SET pulse width that will cause harmonic errors should be approximately 11.3 ps. The minimum output SET voltage pulse width to induce harmonic errors are almost the same for all three gates (3x, 6x, and 12x inverters) and are measured as 38 ps, which is larger than 11.3 ps.



(a) Collected charge window of the three inverters..



(b) SET pulse width window of the three inverters.

Figure VI.6: The maximum accumulated phase error for single-event strike at a 3X, 6X and 12x inverter in the capacitive-tuning DCO monitored at the output node at 2.97 GHz of frequency.

In this case, 38 ps is the $t_{SET(min)}$ that could propagate through the loop due to asymmetric circuit design of the logic gates.

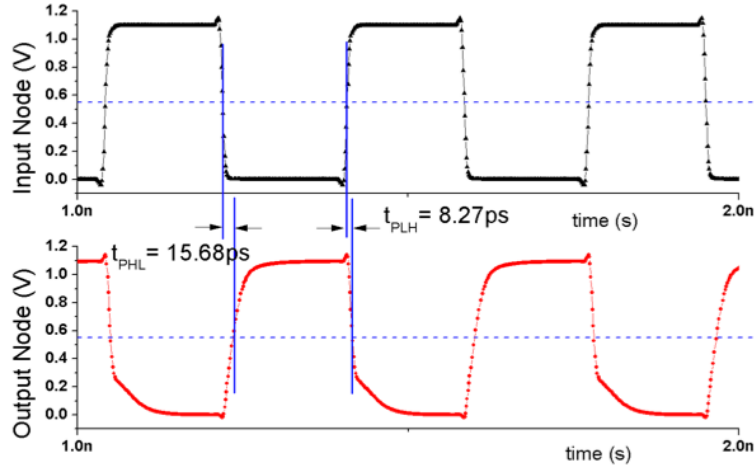
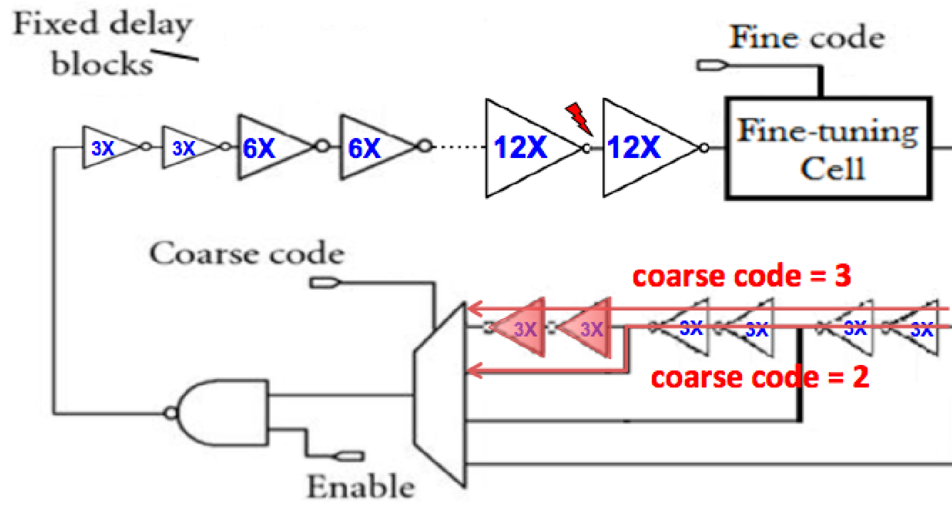


Figure VI.7: Propagation delay measurement for the fine cell in the capacitive-tuning DCO

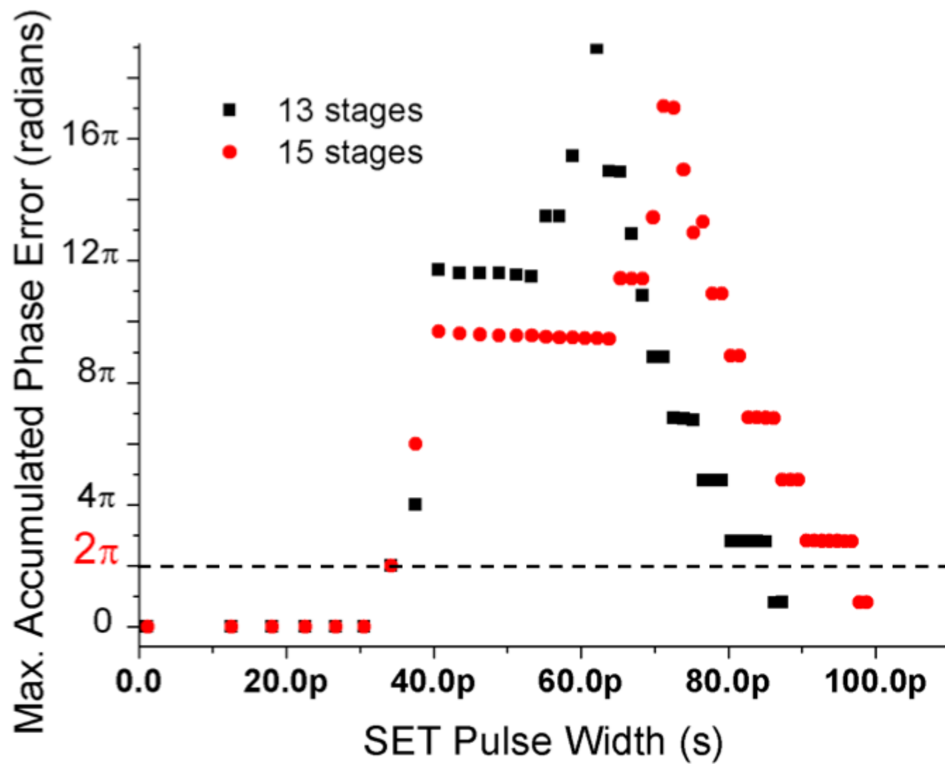
VI.3.2. Verification On the Upper Limit of the Pulse Width Window

According to Eqn. V.4, the longest SET pulse width that can cause harmonic errors is directly proportional to the clock period. For the DCO design, when the coarse code changes, the feedback path of the ring changes through the multiplexer. As shown in Fig. VI.8a, when the coarse code changes from 3 to 2, the number of stages in the ring changes from 15 to 13, eliminating 2 3x inverters. As expected, this resulted in the $t_{SET(max)}$ to induce harmonic errors increasing by 2 gate delays as seen in Fig. VI.8b. However, the fine code is kept the same thus the largest gate propagation delay was the same, because the 3x inverters are smaller comparing to the fine cell under this fine code.

The propagation delay time, which is around 14ps, is calculated from the input and output signals of two 3x inverters shown in Fig. VI.9, which means the total loop delay is changed by about 14ps when coarse code changes from 2 to 3. A thorough mathematical calculation is carried out to confirm the relationship between the total loop delay and the upper limit of the pulse width window.



(a) Comparison of 13 and 15 stages in the ring



(b) SET pulse width window for the 12x inverter

Figure VI.8: SET pulse width window for the 12x inverter corresponding to different coarse code and same fine code.

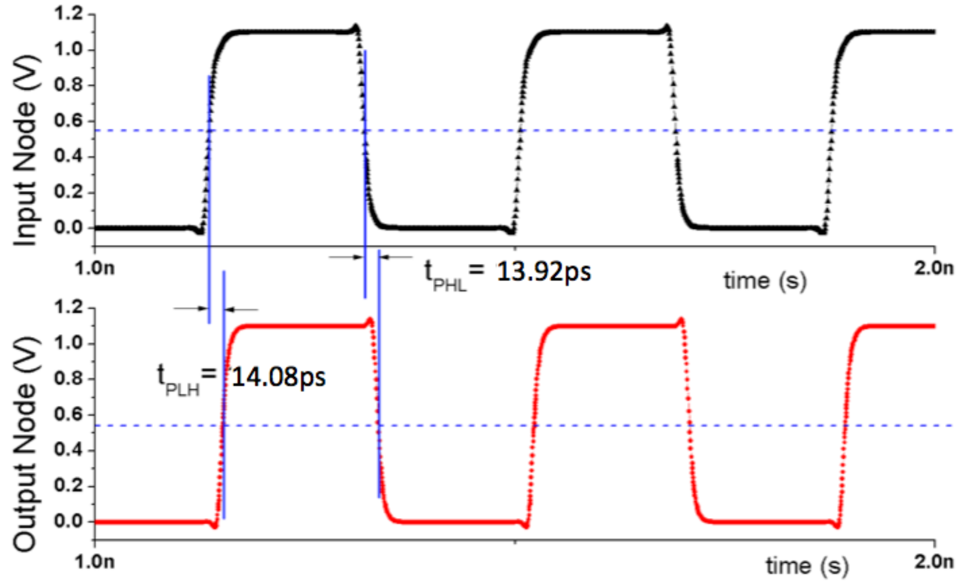


Figure VI.9: The propagation delay of two 3x inverters .

Further analysis of the hit node voltage transition at the upper boundary of the SET pulse width is shown in Fig. VI.10. $t_{a1}(t_{b1})$ or $t_{a2}(t_{b2})$ corresponds to the time intervals between the former (following) clock edge and the starting transition (recovering transition) of SET voltage pulse when the number of stages in the ring is 15 or 13. T_1 and T_2 is half of the clock period, and t_{SET1} and t_{SET2} are the SET pulse widths corresponding to the cases with 15 delay stages and 13 delay stages in the ring respectively. All three time segments a, b and t_{SET} in both cases are longer than the $t_{SET(min)}$ of 38 ps. When the SET pulse width is increased such that one of these time segments is smaller than $t_{SET(min)}$, only the duty-cycle error and missing pulse errors were observed, as seen in Fig. VI.8b.

Table VI.1: Comparison of the variables in Fig. VI.10 for 15 stages and 13 stages.

	T	t_a	t_{SET}	t_b
15 stages	T_1=183 ps	t_{a1}=42.42 ps	t_{SET1}=98.7 ps	t_{b1}=40.3 ps
13 stages	T_2=169 ps	t_{a2}=40.52 ps	t_{SET2}=87.4 ps	t_{b2}=39.8 ps

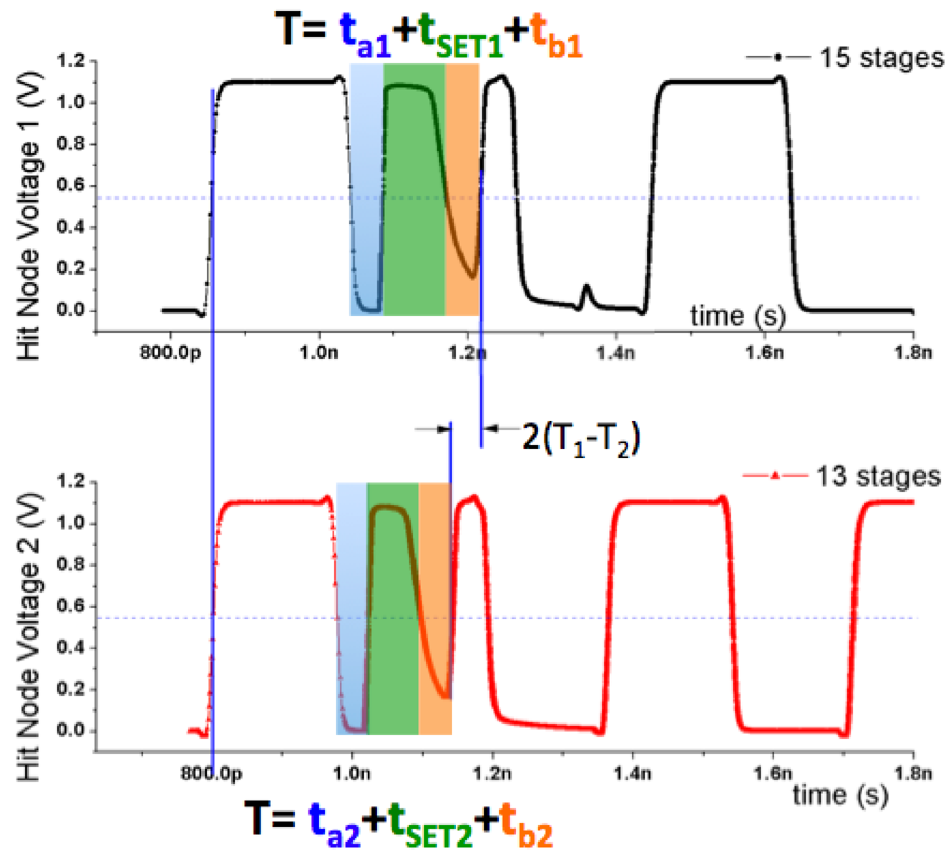


Figure VI.10: Hit node voltage transition at the maximum pulse width to result in harmonic errors in the cases of a15-stage (upper figure) and a 13-stage (lower figure) DCO.

CHAPTER VII

ELECTRICAL TESTING RESULTS WITH DISCRETE COMPONENTS

VII.1. Experimental Details

As shown in Fig. VII.1, harmonic errors could be introduced to the ring-based oscillator by toggling the enable input to one of the NAND gate.

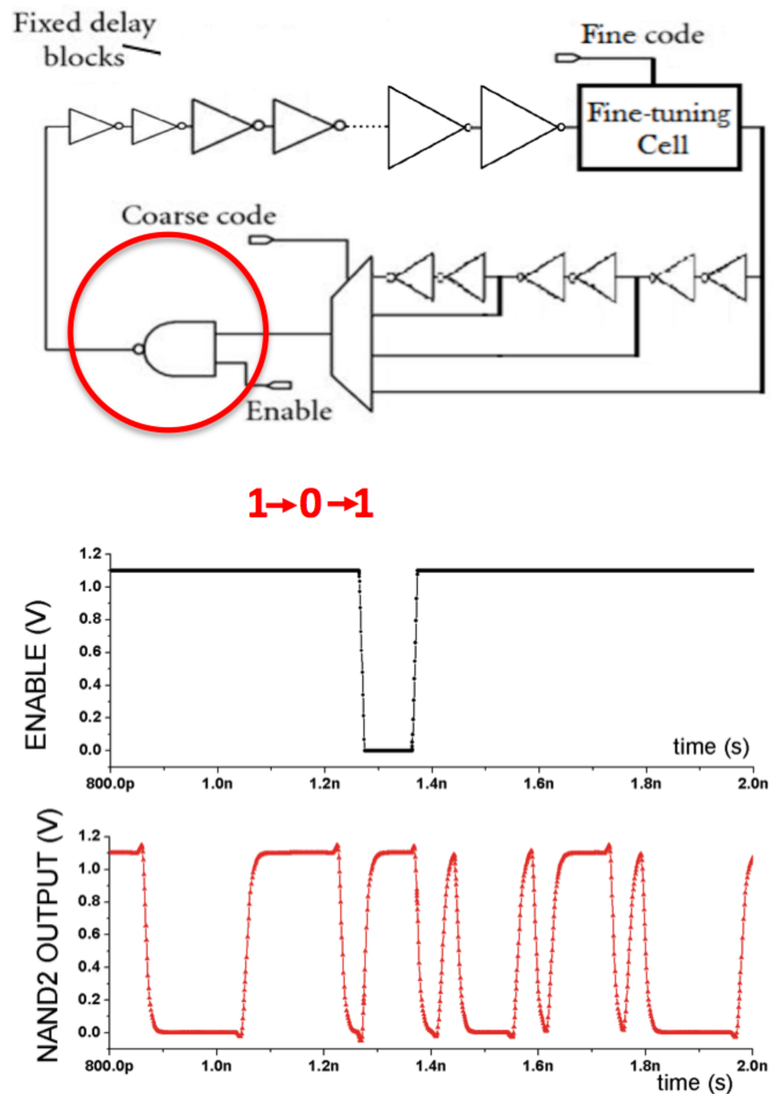


Figure VII.1: Harmonic error could be introduced by toggling the enable input to the NAND gate.

Three ROs were constructed with discrete inverters and NAND gates in order to demonstrate the harmonic theory and simulation results in a physical circuit, as shown in Fig. VII.2. Design specifications are provided in Table VII.1. An Altera DE2 FPGA board was used to inject a voltage pulse (emulating SETs) through the ENABLE input of the NAND gates into the test systems. Injected pulse widths ranged from 40 ns to 400 ns (by a step size of 20 ns) were synchronized to the DE2 50 MHz clock. A Tektronix 2.5 GHz oscilloscope was used to monitor the output of the NAND gate and the input error pulse. The three oscillators are referred to as RO1, RO2 and RO3 in the following text. Design specifications for these three oscillators (RO1, RO2 and RO3) are shown in Table VII.1.

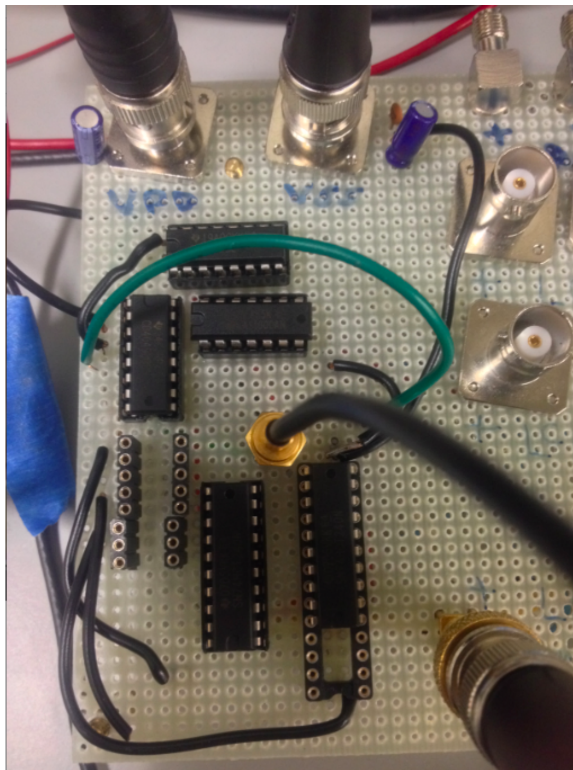
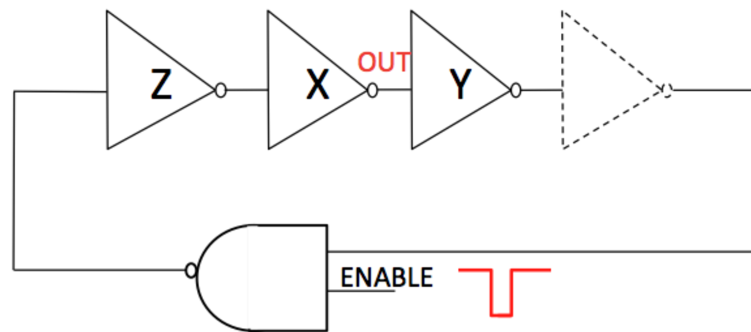


Figure VII.2: Ring oscillators formed from discrete inverters and NAND gates in Table VII.1.

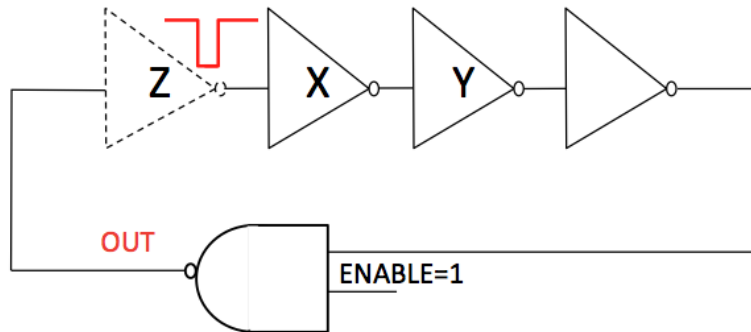
The largest gate propagation delays for all the three oscillators were measured to accurately verify the lower and upper limit of the harmonic window. Pulses with different pulse widths were injected by FPGA to see if they can propagate through each gate in the

Table VII.1: Design specifications for ring-based oscillator circuits RO1, RO2 and RO3.

Part Name	**Part Description**	**No. of Devices in RO1**	**RO2**	**RO3**
SN74HCT240	inverters	14	14	16
CD4049UB	inverters	12	7	7
CD4502UB	inverters	0	1	1
SN74AS1000A	NANDs	1	1	1



(a)



(b)

Figure VII.3: RO loop is broken up in different ways to measure the minimum pulse width that could propagate through the gate of interest X. The dashed lines indicates the gate being pulled out of the loop for each experiment in (a) and (b).

ring by breaking up the loop and keep the driving and loading conditions of the gate the same. As shown in Fig. VII.3, the logic gate of interest in the loop is X. Firstly, the gate after Y (the loading gate for X) is taken out of the board to break up the loop and guarantee the same driving and loading gate for X as in a closed loop. Pulses are sent into the chain through the ENABLE input of the NAND gate. By monitoring the output of the X gate, it could be confirmed whether the pulses were attenuated or broadened. Secondly, by taking out the gate before Z, the predecessor gate of X, and sending the pulses through Z, it could be confirmed whether a pulse could through pass through X and show up at the output of the NAND gate, seen in Fig. VII.3b. For RO1, RO2, and RO3, the smallest pulse width that could propagate around the loop was 40ns, 80ns and 40ns respectively. Shown in Table VII.2 is the deduced harmonic window from measured largest gates propagation delay and loop delay in comparison with the measured harmonic window. The theoretically deduced values matched the measured results of harmonic windows.

In the experimental measurement, just like in the SPICE simulation, cycle-to-cycle clock phase jitter, the amount of phase fluctuation the clock signal encounters every cycle, was included in the noise floor of the quantified results.

VII.2. Experimental Results

First, according to the previously proposed criteria for harmonic generation, the minimum pulse width required to generate a harmonic should be larger for RO2 than for RO1 because t_{dmax} in RO2 ($\sim 80ns$) is larger than the t_{dmax} in RO1 ($\sim 40ns$) although RO1 and RO2 have similar total delays and operating frequencies. The measured accumulated phase error versus input SET pulse width are displayed in Fig. VII.4a and Fig. VII.4b and clearly indicate that the minimum pulse widths to induce harmonic errors in RO1 and RO2 are 60 $\pm$20ns and 110 $\pm$20ns, respectively.

As to RO2 and RO3, though they operate at different frequencies, the lower limits of the windows werent significantly different ($\sim 100ns$) for both RO2 and RO3. This was

because the largest gate in RO2 and RO3 was the same inverter, which had a propagation delay of around 100ns, i.e. $t_{dmax} \approx 100ns$.Thus any pulses that had a pulse width of less than 100ns were not able to go around the loop and induce harmonic errors. This pulse width corresponds to the collected charge of Q_{min} in simulation results, shown in Fig. VI.4.

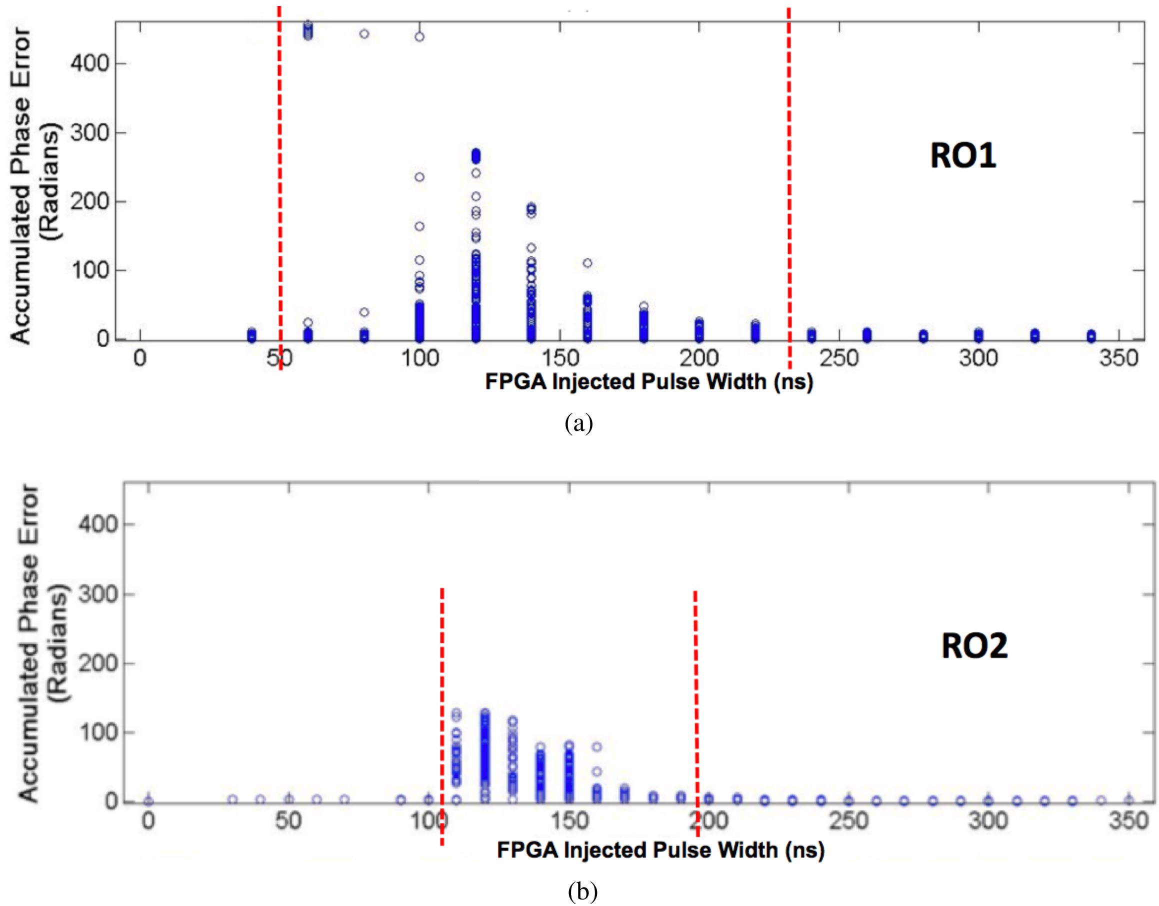
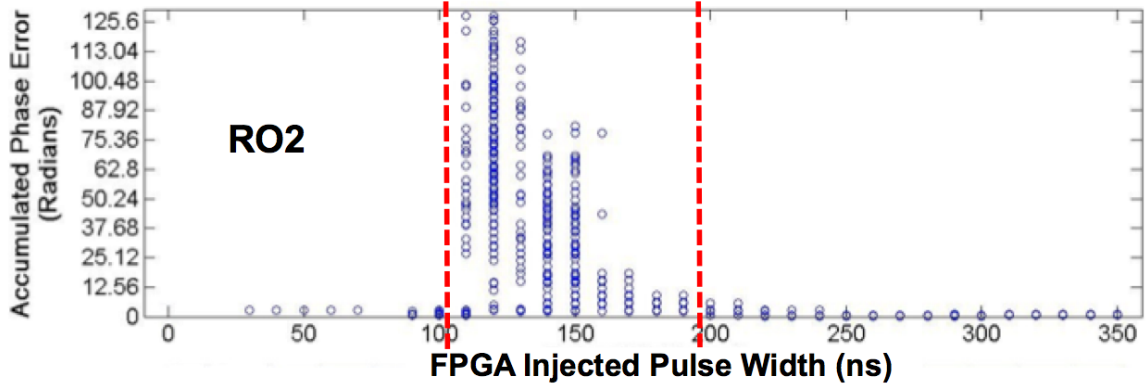
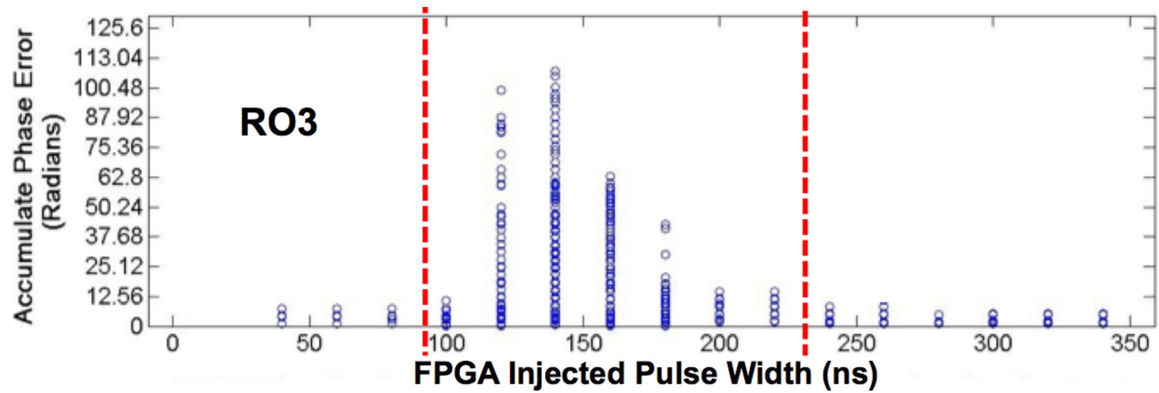


Figure VII.4: Measured maximum accumulated phase error versus FPGA input pulse width for (a) RO1 and (b) RO2.

Second, comparison between the upper limit of the harmonic windows of RO1 and RO2 is shown in Fig. VII.4a and Fig. VII.4b. Even though RO1 and RO2 have the same operating frequency, RO1 exhibits a larger pulse width window than RO2 as expected. The measured upper limits of the windows are respectively 220 ±20ns and 190 ±20ns, which agree with the theoretical values calculated from the harmonic criteria, as shown in Table VII.2.



(a)



(b)

Figure VII.5: Measured maximum accumulated phase error versus FPGA input pulse width for (a) RO2 and (b) RO3.

An additional comparison may be made between RO2 and RO3, as the t_{dmax} for the two oscillators are identical ($\sim 80ns$), while the total loop delays are different (because RO2 has fewer stages than RO3). Shown in Fig. VII.5a and Fig. VII.5b, the upper limit of the pulse width window exhibited a clear difference. While for RO2 the upper limit was around 190 ±20ns, the upper limit for RO3 was around 220 ±20ns. As expected, the calculated values of 130 ±40ns for RO2 and 160 ±40ns for RO3 agree with the experimental results.

Examination of curves in Fig. VII.4 demonstrates that ring oscillators with similar operating frequencies may exhibit very different SE responses. It is clear that the RO1 design is more vulnerable to SE-induced harmonic errors than the RO2 design based on the window of vulnerability. The main difference between the two designs is the incorporation of a longer delay gate to improve SE response based on Eqns. V.3 and V.4. Instead of designing the ring oscillator with inverters of identical sizes as is done conventionally, using a gate with a large delay can make the RO less susceptible to SE effects.

Table VII.2: Measured results for ring-based oscillator circuits RO1, RO2 and RO3.

Measured Period (ns)=2×(Total Loop Delay)		**538**	**539**	**640**
Measured Frequency (MHz)		**1.86**	**1.86**	**1.56**
Measured $t_{SET(min)}$ (ns)		40 ± 20	80 ± 20	80 ± 20
Measured Harmonic Window	**Lower limit (ns)**	60 ± 20	110 ± 20	100 ± 20
	Upper limit (ns)	240 ± 20	190 ± 20	220 ± 20
Calculated Harmonic Window	**Lower limit (ns)**	40 ± 20	80 ± 20	80 ± 20
	Upper limit (ns)	190 ± 40	130 ± 40	160 ± 40

CHAPTER VIII

SET VULNERABILITY COMPARISONS OF THE DCO TOPOLOGIES

While SEU-induced errors are directly related to the radiation hardness of the FF designs used in the DCOs, the SET-induced errors in DCOs are not as straight forward. This chapter mainly analyzes the susceptibility of DCOs to SET-induced errors.

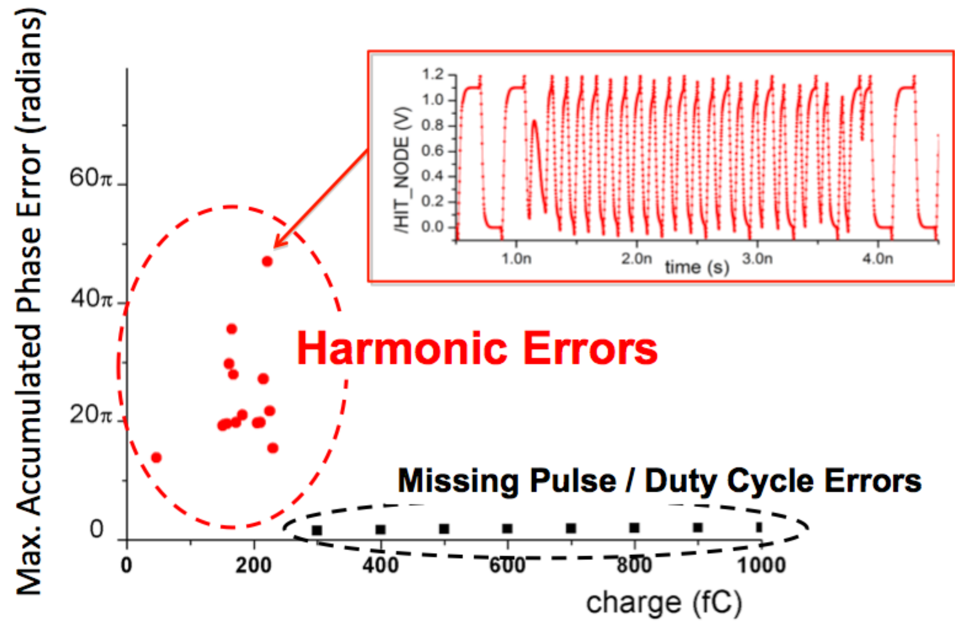
After each simulated ion strike, the perturbations induced in the output oscillating signal of the DCOs were measured. Due to the large amount of data produced by the simulations, the analysis was limited to worst-case simulated strikes. The worst-case phase displacement error in the cases of duty-cycle and missing pulse errors, and the worst-case maximum accumulated phase errors in the case of harmonic errors are plotted for each collected charge.

VIII.1. Overall SET-induced Errors Vulnerability Comparison

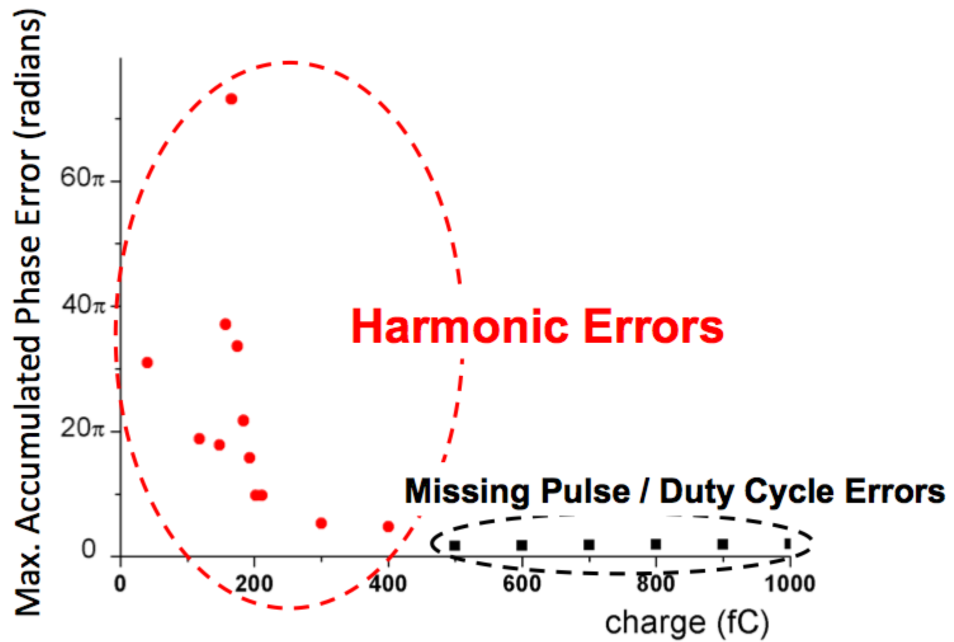
A direct SET sensitivity comparison between the two DCO topologies for all three error signatures by using the same accumulated phase error metric to quantize the duty cycle errors, missing pulse errors and harmonic errors at the same time. As stated in the previous chapters, different maximum accumulated phase error (ϕ_{MAX}) values could be attained for different collected charge when a single particle strike happens at a specific node in the circuit. For the simulation, collected charges in the range of 25 fC to 1 pC with a step of less than 3 pC were used to model the SE strike. Also, the strikes were simulated to occur temporally over the clock period and at every node in the circuit to obtain the worst-case maximum accumulated phase error for each value of collected charges for both DCO topologies at the same operating frequency, and that is plotted in Fig. VIII.1 .

The two plots represent two properties of the SET-induced errors in DCOs:

1. Harmonic errors exhibit phase errors a lot worse than duty cycle or missing pulse errors: Duty cycle errors result in phase errors less than 2π, and missing pulse errors result



(a) Capacitive-tuning DCO



(b) Drive-tuning DCO

Figure VIII.1: Single-event error comparison between capacitive-load DCO and drive-strength DCO.

in phase errors a little bit greater than 2π but smaller than 3π, while harmonic errors can reach 60π because of sudden clock edge injection.

2. Since each circuit component has its own collected charge window, harmonic errors dominate the single event performance of the DCOs when the collected charge stays in the collected charge window for harmonic error generation of the gate under struck. And when the particle charge is extremely high (low), i.e. out of the collected charge window, the DCOs only exhibit duty cycle and missing pulse errors.

VIII.2. SET Vulnerability to Missing Pulse and Duty Cycle Errors

VIII.2.1. Fixed Control Words

Different from traditional ROs, the main components of the designed DCOs are inverters of different sizes, MUXs controlling the length of the ring, NAND gates for initial start-up, and fine cells, which could be either the drive-tuning or the capacitive-load tuning cells. By digitally biasing the two designs to operate at 2.97 GHz and performing the simulated SE strikes with collected charge sweeping from 25 fC to 1 pC at each node, the SET vulnerability of the designs to missing pulse and duty cycle errors were compared using the phase displacement error metric from literature.

The maximum phase displacement errors for different elements over each value of collected charges collected at 2.97 GHz are plotted in Fig. VIII.2 for both DCO topologies. The two plots show that the maximum phase displacement errors for both topologies end up roughly in the same range of radians over the sweeping of collected charge. The capacitive-load DCO exhibits more distributed phase displacement error comparing with the drive-strength DCO, because the former design has more choices of the sizing of inverters comparing with the latter one. In addition, as expected, logic gate with smaller equivalent width to length ratio exhibit larger phase displacement error compared with larger gates. all the curves in both images shows similar trends that displacement error gets worse with increasing of deposited charges. And when the deposited charge is large

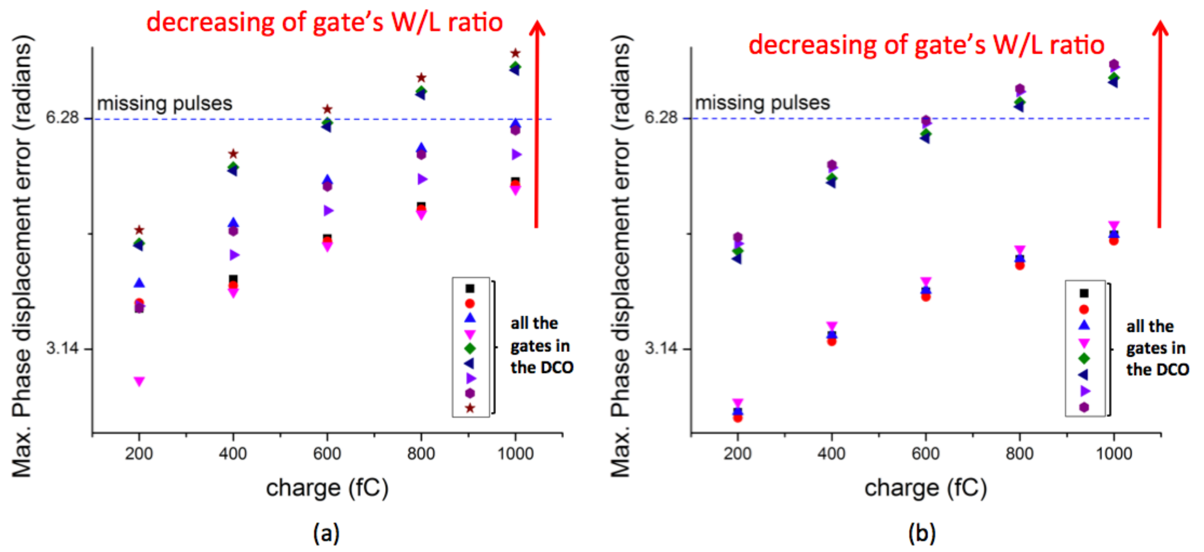


Figure VIII.2: Maximum phase displacement at 2.97 GHz for (a). Capacitive-load DCO (b). Drive-strength DCO. Different shapes correspond to different components in the circuit.

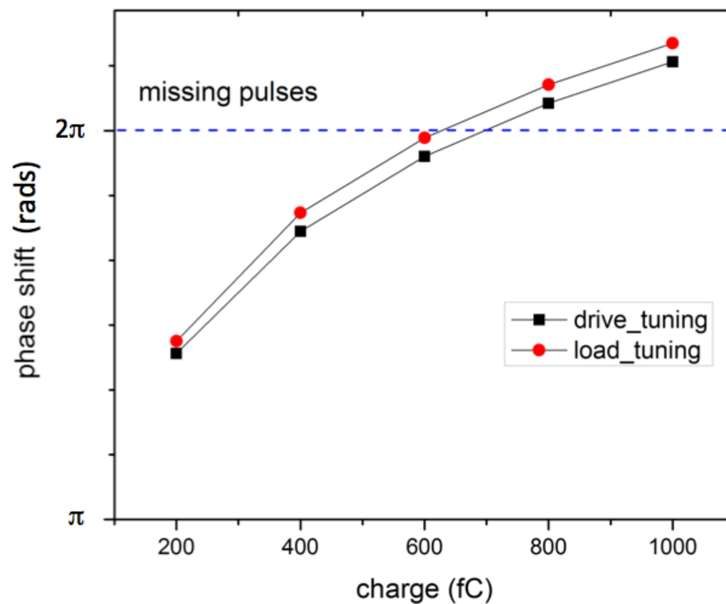


Figure VIII.3: Worst-case phase displacement in all duty cycle/missing pulse error cases of both capacitive-load DCO and drive-strength DCO.

enough, the both topologies of DCOs would start to have missing pulses, i.e. phase shift larger than 2π, rather than duty cycle errors (phase shift smaller than 2π).

The worst-case phase displacement for both topologies in this case, which is illustrated alone in Fig. VIII.3, is induced by striking the 3x inverter. This is because the 3x inverters are gates with the smallest W/L ratio in the both of circuits.

VIII.2.2. Changing Control Words

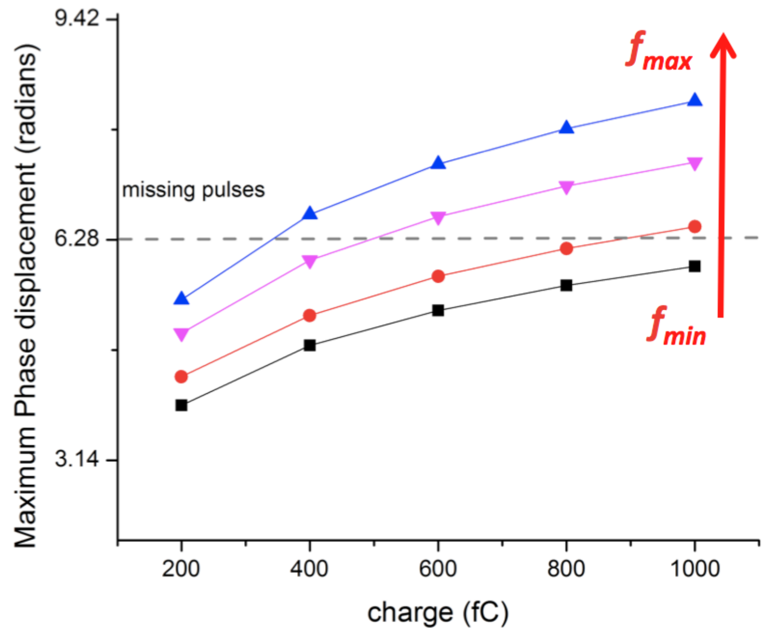
Changes in control words correspond directly to the changes of the operating frequency of the DCOs. SET simulation results were collected when both fine (0$\sim$31) and coarse (0$\sim$3) control words were at the extremes for both DCOs. The worst-case phase displacements in each condition for both DCO topologies are shown in Fig. VIII.4. The worst-case phase displacements resulted from duty cycle and missing pulse errors increase with the increasing of frequency because the SET pulse accounts for higher percentage of the clock period if the frequency is higher.

VIII.3. SET Vulnerability to Harmonic Errors

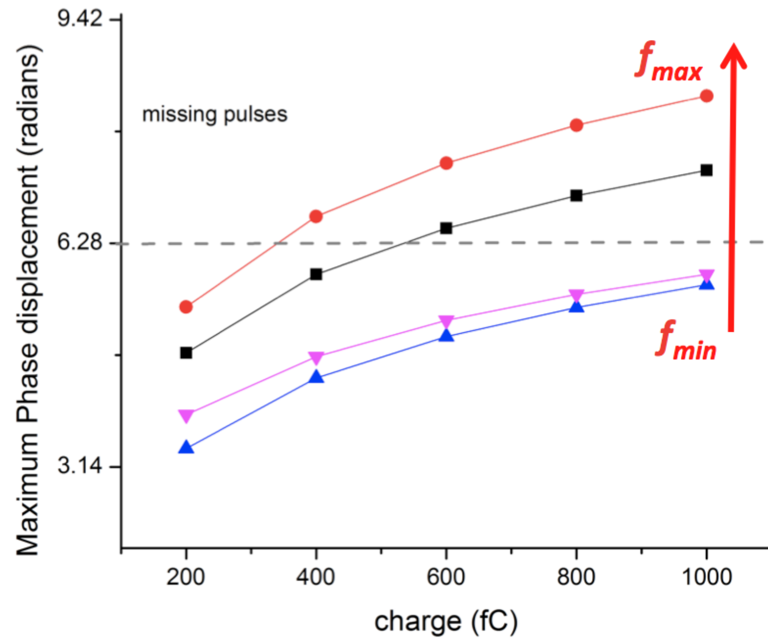
The SET vulnerability of DCOs to harmonic errors discussed in this section is based on the width of SET pulse width window and the corresponding collected charge window for each device. Because the wider the collected charge window, the more possible harmonic errors could be triggered by an originating SET.

VIII.3.1. Fixed Control Words

As stated in the previous chapter, only a window of pulse widths could result in harmonic errors. The pulse width window corresponds to different ranges of collected charges for devices of different W/L ratios. The different collected charge window for the different devices are additive in the sense that, as long as a value of collected charge falls in a collected charge window for one device, it is possible for that value of collected charge to induce harmonic errors for the DCO. As shown in APPENDIX, the drive-tuning DCO



(a)



(b)

Figure VIII.4: Worst-case phase displacement changes from the lowest frequency to the highest frequency for (a). Drive-strength DCO (b). Capacitive-load DCO.

topology utilizes more variety of sizes of inverters than the capacitive-tuning DCO. Therefore, as shown in Fig. VIII.1, the drive-tuning DCO exhibit a slightly narrower harmonic window (collected charge window) than the capacitive-load tuning DCO.

VIII.3.2. Changing Control Words

In the case of fixing striking locations but vary the control codes, two conditions should be included:

1. Differ the fine code while keeping the coarse code unchanged:

In this situation, both lower and upper limits of the SET pulse width window are affected since they are all related to the largest gate's propagation delay, which is merely controlled by the fine code. With the increasing of the largest gate's propagation delay, which in drive-strength (capacitive-load) DCO corresponds to decreasing (increasing) of fine code, the SET pulse width window become narrower for a fixed logic gate. This means if the frequency becomes lower by changing the fine code, the collected charge window become narrower.

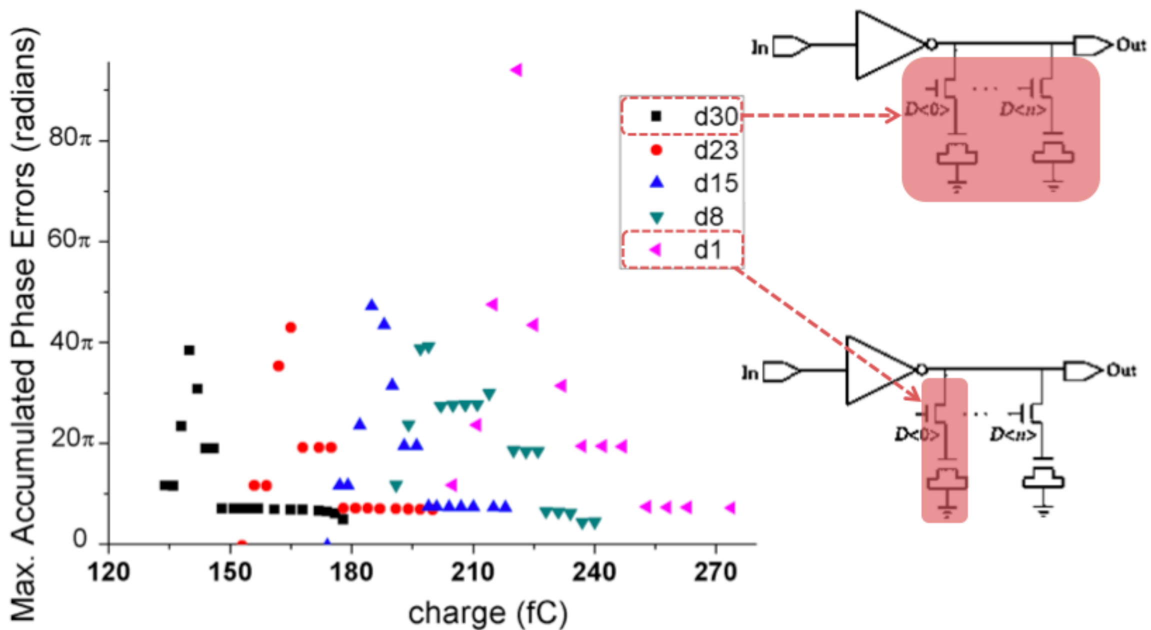


Figure VIII.5: Collected charge window for the fine cell in the drive-tuning DCO corresponding to different fine control codes while the coarse code is fixed

However, as shown in Fig. VIII.5, the collected charge window for the fine cell is shifted to the right but not becoming narrower as the fine code decreases, which corresponds to an increase in drive strength, i.e. the effective W/L ratio, in the capacitive-tuning DCO. This is because the charge required to generate harmonic errors increases with the increasing of the effective W/L ratio. And the increasing of effective W/L ratio counteract the narrowing of the pulse width window.

2. Fix the fine code while changing the coarse code.

In this situation, the number of the stages in the oscillator is changed by changing the coarse word but the digital control word on the fine cell is kept the same. As mentioned in Fig. VI.8b of the previous chapter, only the upper limit of the collected charge window changes with the fine code. With the increasing of the coarse code, which decreases the operating frequency for both DCOs, the collected charge window become wider for a fixed logic gate.

VIII.4. DCO SET Vulnerability Summary

To conclude, the worst-case scenario for duty cycle and missing pulse errors is not heavily dependent on the choice of fine-frequency tuning scheme for DCOs. And those types of errors become more severe with the increasing of collected charges and frequency.

Harmonic errors tend to exhibit larger accumulated phase errors than duty-cycle/missing pulse errors. The capacitive tuning topology has a slightly smaller collected charge window for harmonic errors because the propagation delay of the fine cell in the capacitive tuning topology is smaller than that of the drive-tuning topology at the same operating frequency. In addition, the collected charge windows become wider with the increasing of the coarse code for both DCOs, while they change in opposite directions for the two topologies with the changing of fine code.

CHAPTER IX

DESIGN TRADEOFFS AND CONSIDERATIONS

IX.1. Electrical Performance Comparison of the DCOs to PVT variations

Electrical performance and robustness comparisons of the two topologies of DCOs to process corners, supply voltage and temperature (PVT) variations were conducted using the UMC 40nm bulk PDK. For the three variants, frequency tuning range of the DCOs is selected as the main metric to quantify their impacts on the electrical performance of the circuits. Each group of simulation is carried out by varying one parameter only at one time while fixing the other parameters.

IX.1.1. Process Corner Simulation Results

When investigating process corner variations, Spectre models in the PDK were used for circuit elements at all the global corners. For capacitive-load-tuning DCO, process corners for both transistors (low threshold devices) and Metal Oxide Metal (MOM) capacitors were simulated. Meanwhile, process corners for transistors, including both low and high threshold devices, were simulated for the driving-strength-tuning DCO. High threshold devices were only used in the fine frequency tuning cells to increase the frequency tuning range. The colored boxes for both plots and for all subsequent plots indicate the frequency tuning range for both DCOs at the fastest (orange), typical (blue) and slowest (red) corner. Fig. IX.1 shows how the frequency tuning range varies with global corners at room temperature (27 °C) with standard supply voltage of 1.1V.

From slowest corner to the fastest corner, the driving-strength-tuning DCO exhibited worse average frequency change of 80% than 70% for the capacitive-load-tuning DCO. This is because a passive element like MOM caps tends to be less sensitive to process corner variations than active transistors.

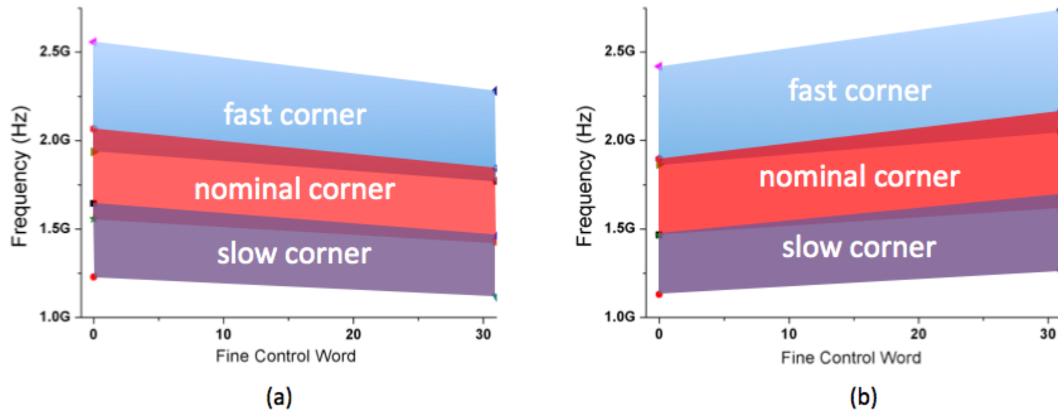


Figure IX.1: Frequency tuning range simulation at different corners for (a). Capacitive-load DCO (b). Drive-strength DCO. Each colored box symbolizes the frequency tuning range at each corner. The upper and lower sides of the box corresponds to the maximum and the minimum of the coarse control word, while the left and right are the minimum and maximum of the fine control word.

IX.1.2. Temperature Variation Simulation Results

As shown in Fig. IX.2, temperature variation simulation was carried out for both designs at typical corner with standard supply voltage of 1.1V. The temperature was set to vary from 0°C to 50°C, and 100°C. As expected, the operating frequencies of both DCOs increase with temperature. While the frequency tuning ranges for both design didnt change very much, the driving-strength-tuning DCO still showed slightly better temperature reliance. This is because, unlike in the case of process corners, passive elements exhibit more changes with the changing of temperature comparing with transistors.

IX.1.3. Supply Voltage Variation Simulation Results

Supply voltage variation simulation was carried out for V=1V, 1.1V and 1.2V at nominal corner for both designs with standard supply voltage of 1.1V. Unlike with temperature, the frequency tuning ranges for both designs varied a lot with the changing of supply voltage in Fig. IX.3. This time, the capacitive-load-tuning DCO showed less supply voltage reliance. When the supply voltage changed from 1V to 1.2V, the average frequency changed

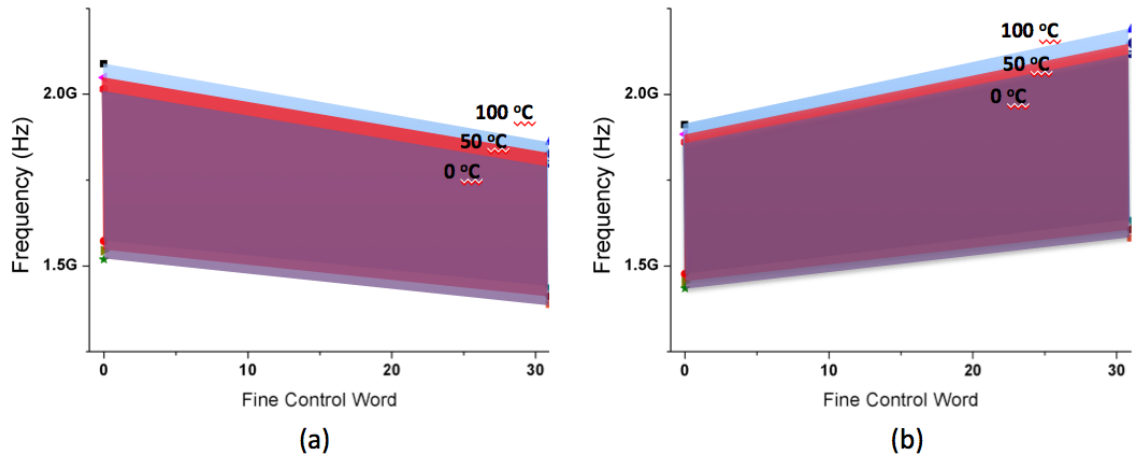


Figure IX.2: Frequency tuning range simulation at different temperatures for (a) Capacitive DCO (b) Drive-strength DCO. Each colored box symbolizes the frequency tuning range at each corner. The upper and lower sides of the box corresponds to the maximum and the minimum of the coarse control word, while the left and right are the minimum and maximum of the fine control word.

by 38.1% than 45% in the case of the driving-strength-tuning DCO.

To conclude, in all situations the frequency tuning ranges are shifted for two DCOs. However, in all cases, the tuning range is not narrowed or widened. Process corner and supply voltage have larger impact on the functionalities of the DCOs comparing with temperature. The overall electrical performance comparison to PVT variation is summed up in the following table.

Table IX.1: Electrical performance comparison of two DCO topologies to PVT variation

	Drive-tuning DCO	Cap-tuning DCO
Process corner dependency	worse	better
Supply voltage dependency	worse	better
Temperature dependency	better	worse

IX.2. Hardening Approach Against Harmonic Errors

As previously stated, DCOs are prone to harmonic errors in the SET pulse width window. In another word, by eliminating the pulse width window could effectively eliminate

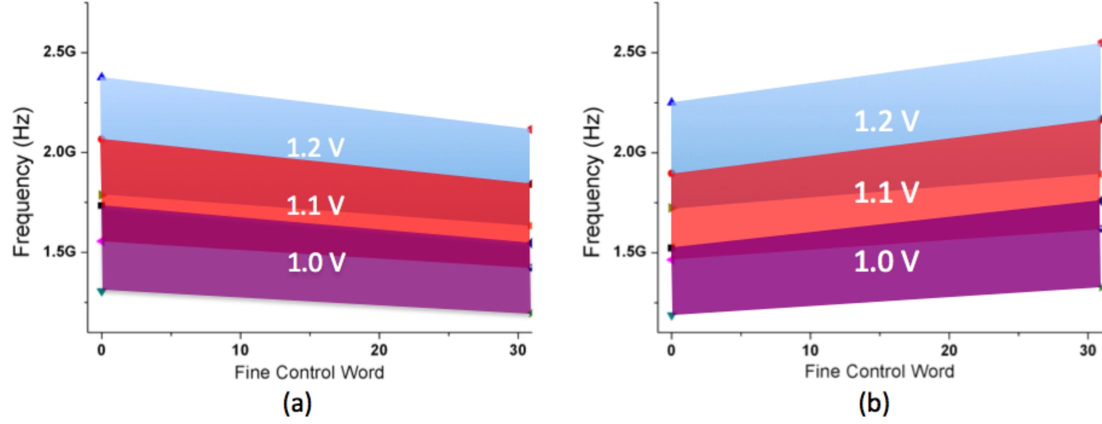


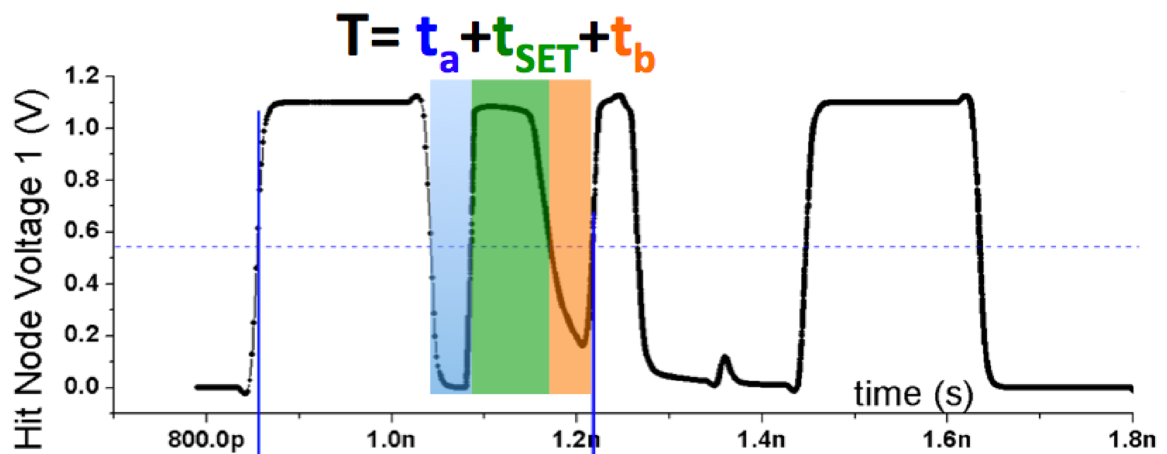
Figure IX.3: Frequency tuning range simulation at different supply voltages for (a). Capacitive-load DCO (b). Drive-strength DCO. Each colored box symbolizes the frequency tuning range at each corner. The upper and lower sides of the box corresponds to the maximum and the minimum of the coarse control word, while the left and right are the minimum and maximum of the fine control word.

the occurrences of harmonic errors.

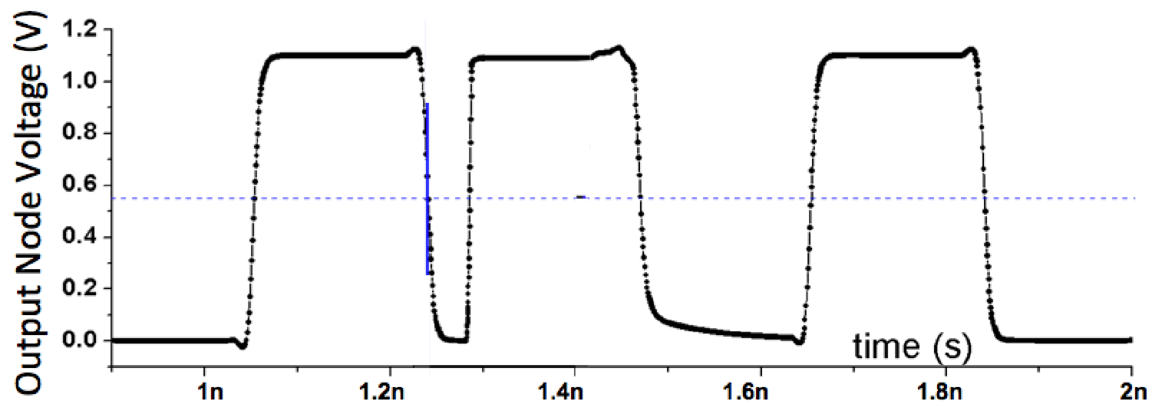
According the proposed harmonic criteria (Eqns. V.3 and V.3),

$$T = t_a + t_{SET} + t_b > 3t_{dmax}, \tag{IX.1}$$

in which t_{dmax} is the largest gate propagation delay in the ring and t_a, t_{SET} and t_b are the pulse widths of the three parts separated by the injected two clock edges. In particular,t_{SET} is the originated SET pulse width. That is to say, if the largest gate propagation delay t_{dmax} is larger than 1/3 of the total loop delay T, both of the SET induced clock edges can not propagate through the loop. Because as long as two out of the three components of T, which are t_a, t_{SET} and t_b, is larger than t_{dmax}, the third one has to be smaller than t_{dmax}, which would lead to immediate termination of harmonics, as shown in Fig. IX.4. This is effectively equivalent to making the PW_{MAX} smaller than PW_{MIN} in the SET pulse width window, thus eliminating the part of collected charge window that results in large accumulated phase errors.



(a) Hit node voltage transition



(b) Output node voltage transition

Figure IX.4: Nodal voltage transition of (a) hit node and (b) output node when at least one of the three time segment t_a, t_{SET} and t_b is smaller than t_{dmax}. The output node exhibit only duty cycle error in this case.

While the designing method could be applied to any RO structures, for DCOs, since the clock period changes with the changing of control words, designers need to make sure the Eqn. IX.1 holds true when the fine cell has the shortest delay while the number of stages in the ring reaches the maximum comparing with all other digital biasing cases. In that way, when the coarse code changes while fixing the fine code, the clock period would become smaller while the propagation delay of the fine cell is fixed, which could guarantee the statement is true. When the fine code changes while the coarse code is fixed, as shown in Eqn. IX.2, since the clock period (b) changes by the same amount (m) with the changing in the propagation delay time of the fine cell (a), the proportion of the delay time of the fine cell would remain larger than 1/3 of the total loop delay when it is biased to have long delays.

$$\frac{a+m}{b+m} > \frac{a}{b}, (a,b,m > 0) \tag{IX.2}$$

IX.3. Performance Tradeoffs

Two design techniques have been applied to the fine-tuning cell of the capacitive-tuning DCO to illustrate the hardening scheme against harmonic errors. Design tradeoffs are discussed in this section.

The design rules the two techniques both follow:

1). Use as few inverters as possible in the fixed delay block in Fig. VI.5.

2). Other than using similar sizes of inverters as in traditional RO designs, lengthen the propagation delay of one cell (in this case is the fine-tuning cell) to achieve the require delay of over 1/3 of the total loop delay.

The two techniques are differentiated by how the propagation delay of the fine-tuning cell is achieved. The first technique, the ”cap hardening technique”, enlarges the switches controlling the capacitive bank loading of the fine cell to allow large capacitive loading and guarantee the same frequency tuning resolution. Additional capacitive load is added at the output of the fine cell to guarantee the same frequency tuning range. The second technique,

the ”current-starve hardening technique”, uses a current starved inverters with digitally controlled headers and footers, as shown in Fig. IX.5, to drive the original capacitive bank for extended propagation delay.

Both of the hardened DCO have similar electrical performances with the unhardened one, as shown in Fig. IX.6. However, Fig. IX.7 illustrates clear advantage of the hardened DCOs in its single-event performance because SE harmonics in both cases are successfully eliminated.

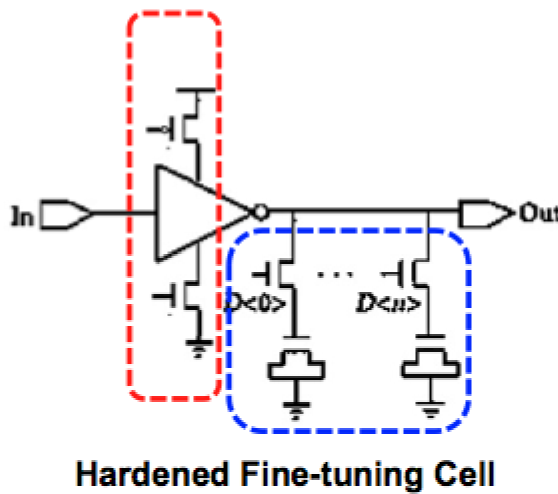


Figure IX.5: Schematic of fine-tuning cell with current-starved hardening technique.

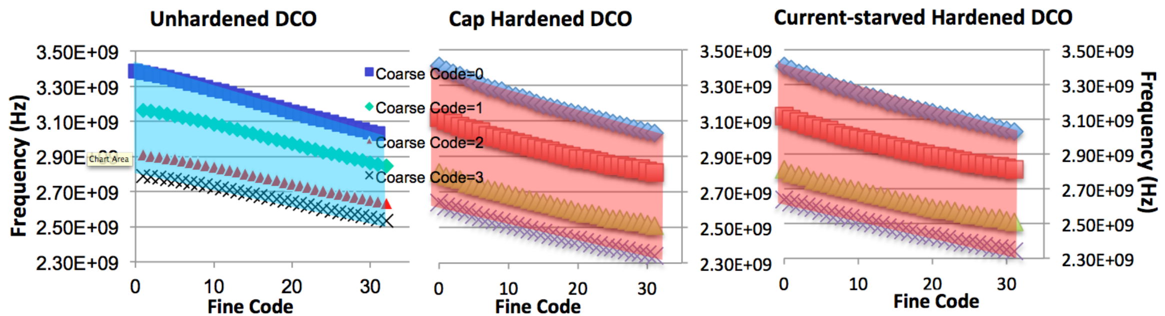
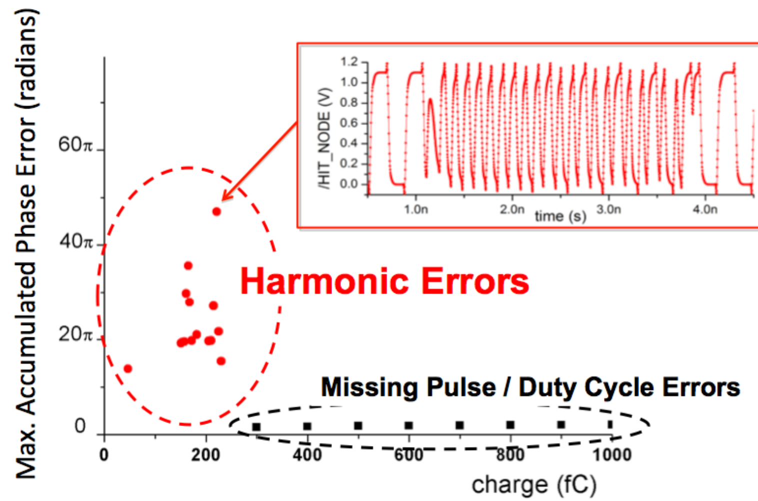
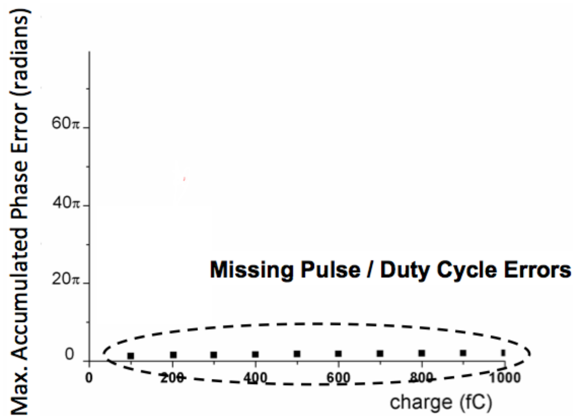


Figure IX.6: Electrical performance comparison of the hardened and unhardened capacitive DCOs.

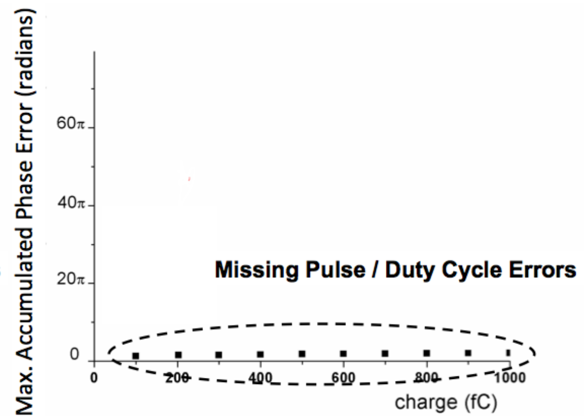
Design tradeoff comparisons are listed in Table IX.2. For the cap-hardening technique,



(a) Unhardened capacitive-load DCO



(b) Cap Hardened capacitive-load DCO



(c) Current-starved Hardened capacitive-load DCO

Figure IX.7: Comparison of single-event performance of (a). Unhardened capacitive-load DCO (b). ”Cap Hardened” capacitive-load DCO (c). ”Current-starved Hardened” capacitive-load DCO at 2.97 GHz.

estimate area increases by 90% because the major area of the DCO is taken up by the capacitive bank, which is doubled in the case of hardened DCO. Average estimate power increase is 75% because of the added capacitor. For the current-starved hardening technique, the only overhead is the added headers and footers. However, compared with the eliminated inverters in the fixed-delay block, the overhead is minimal. Clearly, between the two techniques, current-starve hardening technique is favored because of zero area and penalty. It is worthy of mentioning that because the propagation delay of the fine-tuning cell is deliberately increased. The output voltage of the fine-tuning cell may not be full-swing. A buffer external to the oscillator is necessary when this is used as the output node of the DCO. Overall, the results demonstrate the effectiveness of proposed design rule of making fine-tuning cell occupy over 1/3 total loop delay in terms of designing a ring-based DCO circuit against harmonic errors.

Table IX.2: Power and area tradeoff with the two implemented hardening techniques.

	Cap Hardening Technique	Current-starved Hardening Technique
Area penalty	90%	-10%
Power penalty	75%	-30%

CHAPTER X

CONCLUSIONS

SEEs in ring-based DCOs are characterized in this work. The SET characterization was performed for a wide range of collected charge values (from 25 fC to 1 pC). We observed oscillating frequency error resulted from single-event strikes happening in the FFs of the register of the DCOs. We also observed three other error signatures - duty cycle, missing pulse errors, or harmonic errors - resulted from SETs in actual ring-based oscillator.

Overall single event and electrical performance of the DCOs are not severely dependent on the fine-tuning topologies of the DCOs. SE harmonic errors exhibit larger accumulated phase errors comparing to duty-cycle errors and missing pulse errors in RO circuits. SE harmonic errors exhibit a type of vulnerability window with respect to pulse width, which we call the SET pulse width window. The lower limit of the SET pulse width window corresponds to the largest gates propagation delay in the loop. The upper limit of the SET pulse width window corresponds to the total loop delay subtracted by two times the largest gates propagation delay. By making one of the gate with a large delay rather than using the same W/L ratio for every gate that is used in the circuit, RO circuits can exhibit a smaller harmonic window and be less susceptible to harmonic errors.

Appendix A

STAGE DELAY IN TWO DCO TOPOLOGIES

I.1. Capacitive-tuning DCO

Table A.1: Propagation delay of each logic gate in capacitive-tuning DCO at 2.97 GHz.

No.	Logic gate description	Delay* (ps)	No.	Logic gate description	Delay* (ps)
1	3x inv	6.7	11	12x inv	7.5
2	3x inv	8.68	12	12x inv	6.4
3	3x inv	7.75	13	FINE CELL	11.3
4	3x inv	9.08	14	12x inv	5.4
5	3x inv	7.08	15	12x inv	5.2
6	3x inv	6.6	16	12x inv	5.4
7	MUX**	48.3	17	12x inv	5.1
8	NAND2	9.5	18	12x inv	5.3
9	6x inv	8	19	12x inv	5.8
10	6x inv	8.6	20	12x inv	5.2

***: Propagation delay per gate.**
****: Consisted of several NAND2 gate.**

I.2. Drive-tuning DCO

Table A.2: Propagation delay of each logic gate in drive-tuning DCO at 2.97 GHz.

No.	Logic gate description	Delay* (ps)	No.	Logic gate description	Delay* (ps)
1	3x inv	6.7	9	12x inv	8
2	3x inv	6.68	10	12x inv	7.2
3	3x inv	6.5	11	12x inv	7.6
4	3x inv	7.08	12	12x inv	6.7
5	3x inv	7.2	13	12x inv	7.4
6	3x inv	7.1	14	27x inv	8.8
7	MUX**	47.8	15	FINE CELL	19.8
8	NAND2	10.5	16	FINE CELL	19.3

***: Propagation delay per gate.**
****: Consisted of several NAND2 gate.**

Appendix B

HARDENED VS UNHARDENED CAP-TUNING DCO

Table B.1: Propagation delay of each logic gate of both hardened and unhardened capacitive-tuning DCO at 2.97 GHz.

Unhardened Cap-tuning DCO			Hardened Cap-tuning DCO		
No.	Logic gate description	Delay* (ps)	No.	Logic gate description	Delay* (ps)
1	3x inv	6.7	1	3x inv	6.7
2	3x inv	8.68	2	3x inv	8.68
3	3x inv	7.75	3	3x inv	7.75
4	3x inv	9.08	4	3x inv	9.08
5	3x inv	7.08	5	3x inv	7.08
6	3x inv	6.6	6	3x inv	6.6
7	MUX**	48.3	7	MUX**	48.3
8	NAND2	11.5	8	NAND2	11.5
9	6x inv	8	19	6x inv	8
10	6x inv	8.6			
11	12x inv	7.5			
12	12x inv	6.4	20	12x inv	8
13	FINE CELL	11.3	21	FINE CELL	71.3
14	12x inv	5.4			
15	12x inv	5.2			
16	12x inv	5.4			
17	12x inv	5.1			
18	12x inv	5.3			
19	12x inv	5.8			
20	12x inv	5.2			

***: Propagation delay per gate.**
****: Consisted of several NAND2 gate.**

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