Memristance Phenomenon in TiO_2-Porous Silicon Nanocomposites

By

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Chapter 1: Introduction

In recent years, resistive memory devices have received increased attention for their potential use in novel analog memory applications, such as hardware implementations of neuromorphic networks [1, 2] and as viable alternatives to conventional digital memory [3-8]. For the implementation of neural networks, these devices are promising because they can mimic the behavior of synaptic bonds of neurons in the brain, which are believed to play an essential role in learning processes. In a learning model, the more neurons communicate, the stronger their synaptic bonds become which in-turn allows for easier communication between the neurons. In the case of analog resistive memory, the neural network would be configured in such a way that the more the memory element is used, the stronger (less resistive) its bond becomes to a network of other components.

Although the analog memory applications are a novel and relatively unexplored topic, the primary focus for most resistive memory research is to develop a technology that can overcome the approaching speed and scaling limitations of traditional charge-based digital memory, such as dynamic random-access memory (DRAM) and flash, which experience degradation in performance at extremely small scales [9-11]. Digital resistive memory, such as resistive RAM (RRAM), operates based on the ability of the device to switch between two discrete resistance states, referred to as the high resistance state (HRS) and the low resistance state (LRS) [6, 8, 9, 12]. Exploration of new types of materials and memory mechanisms have made RRAM and other potential memory architectures promising and viable alternatives to charge-based devices by offering a way to continue shrinking feature sizes that combines high densities and high access speeds with low power consumptions [8, 9, 13, 14].

In recent years, variable resistive materials have been linked with the theory of memristive systems, which are two-terminal, passive electronic circuit elements that exhibit both analog and discrete nonvolatile resistance memory behavior [7, 14-16]. Such memristive devices have been implemented to realize binary RRAM architectures, and offer potential as multi-bit memory elements [4, 17]. As an example of multi-bit implementation, binary 00, 01, 10, 11 could be represented by a device possessing four distinct resistance states. This would allow the use of only one device where previously two were needed. Implementations of such a device would allow further chip scaling as the number of necessary elements could be greatly reduced.

Although much of the excitement over the prospects of memristive systems has been in the area of digital memory, it should be expected that there are numerous additional applications of nonvolatile, variable resistance devices that have yet to be fully explored such as applications associated with high power electronics or signal processing. In the area of high power applications it is necessary to develop large scale devices which can support high voltages and currents. However, issues arise due to the inability to observe variable resistance effects above the nanoscale. The main reason for this restriction of variable resistance phenomena to small scales is that very high electric fields would be needed to observe variable conductivity at a macroscale level. The necessity of the high electric field is due to the particular mechanism of ionic conduction associated with resistive memory devices, as will be discussed in section 4.2.3. In this thesis, however, it is shown that by coupling porous silicon (PSi), a material with a macroscopic footprint comprised of millions of nanoscale pores, with a metal oxide that exhibits memristive phenomena, such as titanium dioxide (TiO_2), it is possible to realize a macroscale device that exhibits memristive behavior.

1.1 Search for Alternative Memories

As it pertains to scaling digital components, Moore's law captures the necessity of developing alternative forms of computing and storage: every 18 months, transistor density doubles per square inch on integrated circuits (ICs). The law, put forth by Fairchild Semiconductor and Intel founder, Gordon Moore, in 1965, was based on observations Moore made on the increase in IC component density between 1959 and 1965 [18]. Though originally the doubling period was thought to be every year, it was later observed to be closer to 18 months; nonetheless, the "law" has held true for the past 50 years [18]. Inherent in this law is the fast-approaching scaling wall which terminates the trend at sizes approaching atomic dimensions. Yet, as transistor feature sizes are reduced with increasing component density, it is necessary that the performance of transistors be maintained or improved through successive generations. This continual performance improvement with size scaling has proved challenging. Charge-based memory such as DRAM and flash are encountering performance limitations due to scaling limits - leakage currents that reduce charge storage [9], power and heating issues [11], and parasitic cross-talk [10] all compromise device performance. In attempting to surmount these issues, much research has been devoted to the exploration of new materials for integration into existing memory technologies. For example, new high-k dielectrics materials capable of storing charge longer than conventional SiO_2 storage cells have been investigated [19]. However, in using new dielectric materials, the loss of simplicity in processing is sacrificed. Currently used charge-storing capacitors are fabricated by simple thermal oxidation of the Si substrate.

Another approach to overcoming scaling, speed, and power limits, which has gained increasing interest over the past few years, is the exploration of new mechanistic principles that can govern the storage of data. In this regard, the four main types of next generation nonvolatile memories

considered are discussed below: ferroelectric RAM (FRAM), magnetoresistive RAM (MRAM), phase change memory (PCM), and RRAM .

1.1.1 Ferroelectric Random Access Memory (FRAM)

The use of FRAM as nonvolatile memory is based on the principle of discrete polarization of a ferroelectric material, such as the perovskite $PbZr_{1-x}Ti_xO_3$ or the alloy $SrBi_2Ta_2O_9$ (SBT), by an external electric field [20, 21]. FRAM architectures have demonstrated high speeds (i.e., 160 ns for read plus write times) in terms of access cycles and also provide random access to memory locations [20]. Such memories have been commercialized and used in IC cards and radio-frequency identification (RFID) tags [22]. Drawbacks to this technology include the necessary high-stability of the oxygen barrier used to create the ferroelectric film and the need to process ferroelectric materials like SBT at low temperatures [21]. Furthermore, with continued scaling of feature sizes to atomic dimensions, it becomes increasingly difficult to maintain the amount of polarization charge needed for adequate signal sensing margin [23].

1.1.2 Magnetoresistive Random Access Memory (MRAM)

Magnetoresistive materials exhibit changes in their electrical resistance in the presence of an external magnetic field. MRAM takes advantage of the properties of magnetoresistive materials to store data as magnetic bits for nonvolatile memory [24]. Traditionally, MRAM architectures were based on the phenomenon of giant magnetoresistance (GMR); however, more recently, the magnetic tunnel junction (MTJ) phenomenon has taken precedence [24]. In MTJ devices, a tunnel junction is combined with a magnetoresistive material which exhibits a resistance change under the application of a magnetic field [20]. MTJ-based MRAM is comprised of devices that consist of a single transistor and resistor [20], replacing electric-charge storage with magnetic

storage [25]. The nonvolatile nature and better write operations of MRAM make it more favorable in comparison to DRAM and flash, respectively [24]. The major disadvantages of this type of nonvolatile memory are increased power consumption during write operations [20] and large memory cell sizes [23].

1.1.3 Phase Change Memory (PCM)

PCMs operate based on the ability to switch the phase of a material to one that possesses a distinctly different resistance value [26]. These memories are arguably a better contender for replacing flash in nonvolatile memory applications than FRAM and MRAM. Chalcogenides, such as $Ge_2Sb_2Te_5$, are the predominant class of materials used to implement PCMs, wherein the phase can be switched on application of current induced joule heating [20]. In order to differentiate between the two phases, a low magnitude current with effectively negligible joule heating is applied to read the two states [26].

The primary advantage of PCMs for use as nonvolatile memory is the ability to achieve high density with high performance [20]. In addition, the size-scaling challenges associated with FRAM and MRAM are not present in PCMs. PCM technology has been demonstrated to function at the 45 nm level and research suggests that phase change materials can be integrated into architectures at the 2-5 nm scale [27]. The major disadvantage of this technology is the increased programming current required for smaller feature sizes, which inhibits implementation of high density architectures for this memory type [23].

1.1.4 Resistive Random Access Memory (RRAM)

RRAM is the most recent next-generation nonvolatile memory in development, and has seen increased attention due to inherent advantages associated with processing, scaling and

performance metrics [5]. RRAM is based on the soft dielectric breakdown of an insulator, such as a metal oxide, and the reversibility of this process [5]. Breakdown and the reverse process yield distinct resistance states for the insulator, which in turn can be assigned to be an ON state (LRS) or an OFF state (HRS). Depending on the insulator used, the device can also exhibit different types of switching: bipolar resistive switching, where the switch between high and low resistance states is made by reversing the polarity of the applied signal, or unipolar resistive switching where the resistance can be switched with a single voltage polarity [5].

The greatest advantage of RRAMs over other alternative nonvolatile memory is the seamless compatibility with CMOS processing [9]. Resistance switching has been demonstrated in group IV and III-V semiconductors, organic compounds, and most prominently in metal oxides [5, 6, 9, 12]. The traditional RRAM also has a simple, easy-to-implement structure comprising an insulator or semiconducting material placed between metal electrodes [6]. Data retention times of over 10 years and write endurance of up to 10^6 cycles have been reported for RRAM devices, significantly outperforming most current flash memory devices [12].

1.2 Memristors

In 1971, Leon Chua postulated that for the sake of mathematical completeness, there should exist a fourth fundamental circuit element that embodies the missing relationship between two of the four fundamental circuit variables: electric charge (q) and magnetic flux (φ) [28]. As it stood previously, combinations of these two variables with the other fundamental circuit variables - voltage (v) and current (i) - had established the relationships that define the three fundamental circuit elements: the resistor ($v = \boldsymbol{R}\, i$), the inductor ($\varphi = \boldsymbol{L}\, i$), and the capacitor ($q = \mathbf{C}\, v$) where R is resistance, L is inductance, and C is capacitance. Chua claimed that a relationship between q

and φ defined a new element he termed the memristor, short for memory-resistor, given by the equation $\varphi = \boldsymbol{M}\, q$,where M is the memristance of the device. This element would exist as a two-terminal, passive electronic circuit element, which Chua believed should be considered as a fundamental circuit element [28]. The six relationships between the four fundamental circuit variables, v, i, q and φ are shown in Fig. 1.1 (adopted from [29]). Three of the relationships give rise to the three known fundamental circuit elements, the resistor, capacitor and inductor as discussed above. The memristor, shown in the bottom right corner, is hypothesized to embody the sixth and final relationship relating q and φ.

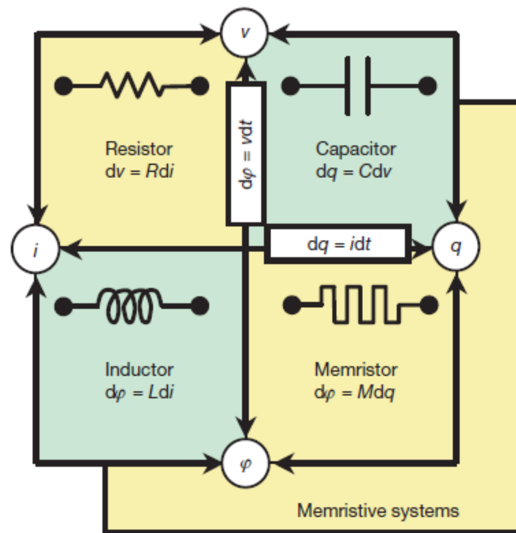


Figure 1.1 - Fundamental variables and their relationships (adopted from [29]). The six constitutive relationships between the four fundamental circuit variables are shown. The memristor, shown in the bottom right with its circuit symbol, is postulated to encompass a relation between q and φ.

1.2.1 Definition of Memristor

The theoretical memristor would behave similarly to a resistor, in that energy is dissipated by Joule heating, not stored, and given in units of Ohms (Ω). However, the device would exhibit

particular nonlinearities and dynamic resistance values which separate it from the traditional resistor. In other words, unlike a linear resistor, a memristor would possess the ability to change its resistance state as a function of the applied voltage or current. Chua also stated that the fingerprint of all memristors is a characteristic pinched hysteresis loop which must be zero-crossing at the origin since the memristor is a purely resistive, passive element. In 1976, Kang and Chua extended the definition of memristance to encompass a wide range of devices collectively named memristive systems [15]. These systems would be defined by the equations:

$$\frac{\mathrm{dx}}{\mathrm{dt}} = f(x, i)$$

$$v = R(x)i$$

where *R(x)* is the instantaneous resistance of a device measured when its internal state variable is denoted by *x*. According to the equation, by adjusting the internal state variable *x* - whose rate of change is a function of its current value - a memristor is able to retain its history as only a specific resistance value is associated with a particular state of the device [30].

Despite the existence of the mathematical basis for memristors as far back as in the 1970s, the realization of variable resistance devices and memristive systems did not occur until decades later. In 2008, a research group at Hewlett-Packard (HP) claimed to have found the missing memristor. Their device consisted of a thin film of TiO_2 sandwiched between two platinum (Pt) electrodes [29]. By observing the characteristic pinched hysteresis loop associated with memristive systems, HP claimed that their device could be termed a memristor that exhibits variable resistance. The proposed mechanism behind the variable conductivity of the HP device lay in the non-uniform distribution of charged dopants in the TiO_2 layer, namely oxygen vacancies. Under application of an electric field, the dopants were thought to migrate to a

particular Pt-TiO_2 interface separating the metal oxide layer into a dopant rich low resistance region and a dopant void high resistance region. By controlling the distribution of the dopants, the overall resistance of the device could be changed.

Following HP's paper, Chua extended the definition of what constitutes a memristor yet again in 2011 to include all resistance switching devices, whether unipolar or bipolar [31]. He stated that as long as a device's hysteresis was pinched, it could be termed a memristor.

1.2.2 Types of Memristors

Since the primary focus of memristive device research is to advance the capabilities of digital storage (e.g., RRAM applications), most studies focus on binary resistance states for memristors [5-8]. Such devices exhibit two resistance states - a high resistance OFF state and a low resistance ON state.

Even with the very realizable promise of binary resistive memory, there is also interest in developing memristive devices that could serve as multi-bit state devices wherein one device could store more than two discrete states [4, 17]. The resistive switching in such memristive devices can be achieved through a gradual application of voltage as opposed to abruptly applying a high voltage to turn the device ON or OFF as in the case of devices with two resistance states. Extending this notion of multi-bit states, if there exists an infinite number of states between limiting values, then the memristor could essentially operate as a passive analog memory element [30].

Chapter 2: Proposed Memristive System

In order to implement a material system that exhibits pronounced variable conductivity or memristance characteristics at a macro-scale, a titanium dioxide (TiO_2)-porous silicon (PSi) composite system was chosen. As will be discussed in section 2.1, the PSi host matrix is comprised of nanoscale void spaces that can be infiltrated with a metal oxide material, such as TiO_2, that exhibits variable conductivity only at nanoscale dimensions. Thus, the TiO_2-PSi system allows for an easily fabricated array of nanoscale memristive elements that collectively have a macroscale footprint. This type of composite material system may be most advantageous for its potential to be used in discrete power heavy devices which must maintain large loads – applications for which traditional nanoscale memristors would fail. A similar system was recently explored in n-type PSi/p-type NiO composite memristors [16].

Figs. 2.1 and 2.2 show a schematic representation of the TiO_2-PSi material system in which TiO_2-filled PSi pores serve as individual memristive elements spaced nanometers apart. When working together, these individual elements effectively operate as one memristor which allows them to operate at much larger scales - tens of microns - than conventional memristive devices which only exhibit effects at the nanoscale level.

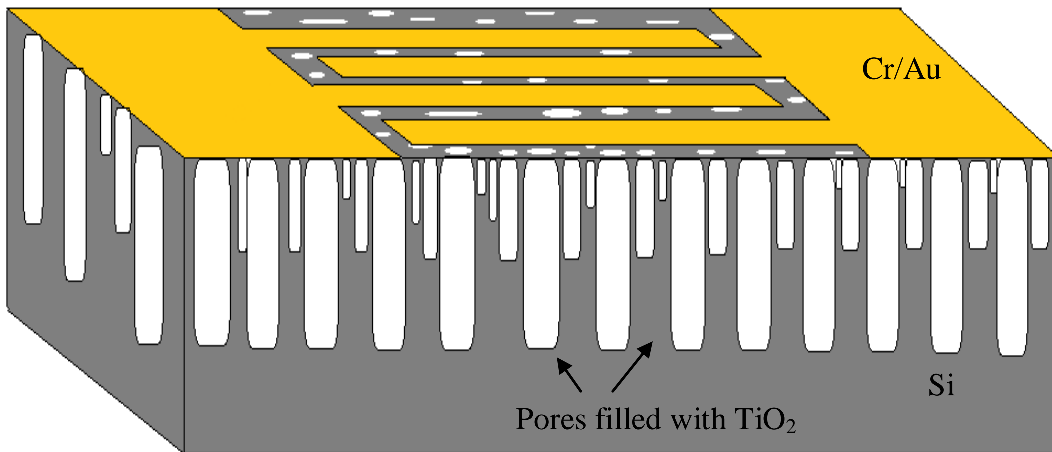


Figure 2.1 - Device structure. The TiO_2-filled pores (white) act as individual memristors in the Si substrate (gray) but the collective variable resistance of all the nanoscale structures produces a micron level device capable of memristance. The devices consists of two terminals (gold color) made of a gold-on-chromium layer.

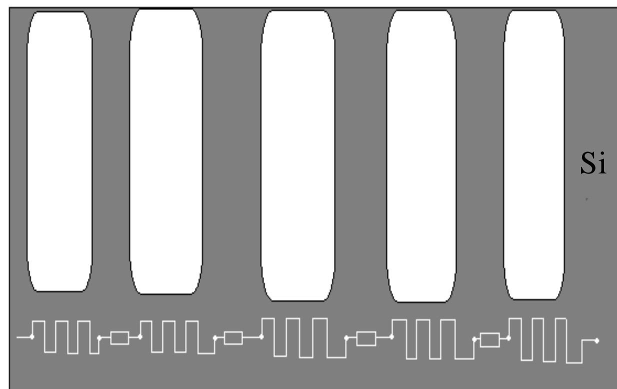


Figure 2.2 - Cross section of device. The TiO_2-filled pores (white) are configured next to each other to create a large array of nanoscale memristors.

To gain an understanding of the mechanism that leads to variable resistance in this composite material system, it is first necessary to acquire basic knowledge of the two materials involved in creating the nanocomposites - PSi and TiO_2.

2.1 Porous Silicon (PSi)

PSi is an ideal candidate as a host matrix as it comprises numerous nanometer scale pores which can be infiltrated with a memristive metal oxide. By doing so, the crystallization of the metal oxide is confined to nanoscale dimensions allowing it to retain its ionic conducting properties necessary for the observation of variable resistance. In effect each pore serves as an individual memristor but the combined memristance of all the pores results in memristance being observed at a macroscale. Fig 2.3 shows a top view image of PSi, taken by scanning electron microscopy (SEM), with the darker areas representing the pores and the lighter, web-like, structure representing the Si matrix

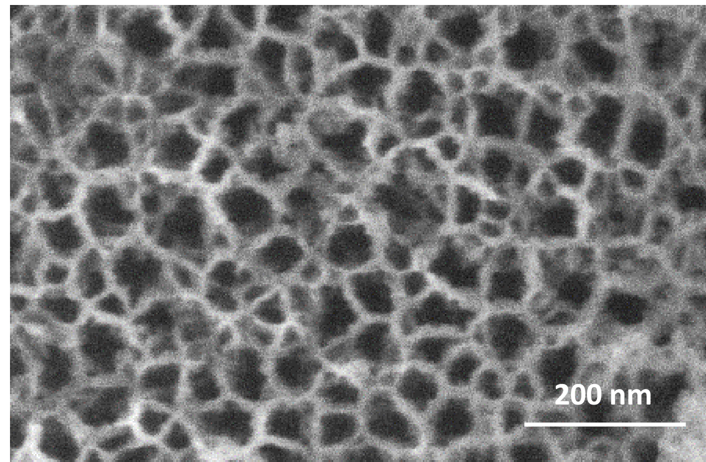


Figure 2.3 - Top view scanning electron microscopy image of PSi. The dark areas represent the locations of the pores and the lighter, web-like network the Si. The size, depth and shape of the pores can be controlled via adjustment of the etching parameters.

2.1.1 Formation of PSi

The discovery of PSi is attributed to husband and wife, Arthur and Ingeborg Uhlir, in 1956 while defining a method for polishing and shaping the surfaces of germanium and Si [32]. Although it

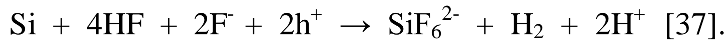
was shown that PSi could be formed through electrochemical etching in hydrofluoric acid (HF) in 1956, the exact mechanisms for pore formation were not understood until years later. Once interest in PSi was renewed in 1990 when photoluminescence in PSi was discovered by Canham [33], several mechanisms that aimed to explain the formation of the nanopores were put forth such as the Beale model [34], the diffusion-limited model [35] and the quantum wire model [36].

According to the Beale model, pore formation occurs when the difference in resistivity between the electrolyte and Si causes current to flow in a localized manner from the electrolyte in the pores to the substrate at the pore tips [34]. Since current is confined to flowing through the pores, dissolution is enhanced at the pores giving rise to a porous structure. The initial difference in resistivity is due to the depleted Si in the PSi matrix, giving PSi a higher resistivity than the surrounding electrolyte.

The diffusion-limited model bases the mechanism of pore formation on either a hole reaction with a Si surface atom or equivalently an electron separating from the Si surface [35]. Similar to the Beale model, the proclivity of holes and electrons to diffuse into or away from the porous regions enhances the formation of pores through dissolution of Si in those regions.

In contrast to the Beale and diffusion-limited models, the quantum confinement models suggests that dissolution and depletion based on transfer of charges causes the formation of pores in Si [36]. In n-type Si, the pores are formed due to depletion of holes owing to a space-charge region. In p-type Si however, the process is more complicated. Quantum confinement in the Si walls between the pores causes an increase in the effective band-gap thereby making it difficult for holes and electrons to migrate to the Si regions. Effectively, a self-etching process is created since the carriers cannot surmount the potential barrier.

Regardless of which mechanism is applied to explain pore formation, the chemistry describing the dissolution of Si is very well accepted. Combining several reactions and neglecting intermediate steps, the overall dissolution of Si in HF can be written as:



$$Si + 4HF + 2F^{-} + 2h^{+} \rightarrow SiF_6^{2-} + H_2 + 2H^{+}$$ [37].

The reaction emphasizes how the negatively charged fluorine ions (F^{-}) react with Si to dissolve the Si away while aided by holes diffusing into the substrate.

2.1.2 Applications of PSi

The main advantages that PSi offers are its large surface-to-volume ratio and high tunability of pore features: pore width and depth. With the ability to fabricate pores on the order of a few to several tens of nanometers in diameter and with millions of such pores contained in a few cm of porous material, the surface area is enhanced by orders of magnitude compared to a plain Si wafer. The diameter, depth and density of the pores can be controlled through adjustment of the etching current density used, duration of electrochemical etching, HF concentration, and doping of the silicon substrate [35].

Owing to the high controllability of pore characteristics, PSi has been used for a wide range of applications spanning optoelectronics [38, 39], biosensing [40-42], drug delivery [43, 44], solar cells [45], and supercapacitors [46, 47]. Typically, the size of the pore and associated porosity of the material is tuned for each respective application. The classification of pores by size is as follows: macroporous (diameter $>$ 50nm), mesoporous Si (diameter between 10-50nm) and microporous Si (diameter $<$ 10nm) [48].

For the purposes of creating a nanocomposite device that exhibits memristance, the pores can be filled with a metal oxide resulting in a nanostructure where each pore can act as a nanoscale memristor. In conjunction with the neighboring pores, a massive nano-network of memristors can thus be created to demonstrate pronounced variable resistivity effects at macroscale levels.

2.2 Titanium Dioxide (TiO_2)

As discussed above in relation to RRAM devices, metal oxides have attracted attention as the preferred insulating materials that exhibit variable resistance. Several transition metal oxides have demonstrated variable resistance resembling memristance such as nickel oxide (NiO) [16], strontium titanate ($SrTiO_3$) [49] and even amorphous tantalum oxide (a-Ta_2O_5) [50]. However, the most studied in relation to variable resistance is TiO_2 [5-8, 29] . TiO_2 has also been used for storage in lithium ion batteries [51], for decomposing environmental contaminants by photocatalysis [52] and for dye-sensitized solar cells [53, 54]

TiO_2 exists primarily in one of two phases: anatase and rutile; brookite is a third much less prevalent phase [55]. The bandgap of anatase is typically 3.21 eV while that of rutile is 3.00 eV [55]. In both of these forms of TiO_2, two major types of native defects are present: titanium interstitials and oxygen vacancies [56]. While the former is responsible for n-type conductivity in TiO_2 at atmospheric pressure and room temperature, oxygen vacancies can act as electron trapping/hopping cites around 0.1 to 0.2eV below the conduction band [57].

The presence of oxygen vacancies is an important consideration since the mechanism believed to be responsible for the observance of variable conductivity in TiO_2 memristive devices is related to the migration of oxygen vacancies. The role this mechanism plays, however, is not yet fully understood. It is believed to be attributable to either (1) the formation of conductive filaments

that establish a low resistance path between the electrodes or (2) the accumulation of defects at the electrodes, which presents a dynamic energy barrier at the interface varying the observed electrical conductivity. These particular mechanisms are dependent on device materials and structure.

The formation of conductive filaments is the most widely reported mechanism where ionic species migrate to form conducting pathways for current to flow from one electrode to the other. In a TiO_2 device, these defects are oxygen vacancies [5, 8]. The mechanism of filaments involves both an electroforming step where a conducting filament must be formed as well as a dismantling/rupture step where a pre-existing filament is removed so that it no longer conducts current. The rupturing step can be achieved either by applying a signal of the opposite polarity used to establish the filament, known as bipolar behavior, or by continued application of a signal of the same polarity which causes Joule heating to rupture the filament, known as unipolar behavior.

The second possible mechanism behind variable conductivity in TiO_2, the accumulation of defects at the metal-oxide/electrode interface [5], is generally characterized by bipolar behavior where the low and high resistance states are alternated by changing the polarity of the applied voltage. It is believed that in this mechanism, the buildup of ionic species, believed to be oxygen vacancies in the case of TiO_2, at the interface either increases or decreases the resistance of the device depending on the conductivity type of the metal oxide [12].

Chapter 3: Fabrication

TiO_2-PSi nanocomposites were fabricated by infiltrating a PSi film with a TiO_2 sol-gel precursor and subsequently annealing the sample to evaporate out the solvents and promote the formation of TiO_2 from the sol-gel constituents. Afterwards, conventional photolithography and metal deposition steps were performed resulting in two-terminal electronic components. When a voltage bias is applied across the metal electrodes, current is expected to flow through the porous region containing TiO_2 to produce variable conductivity characteristics.

TiO_2 was chosen because it is known to exhibit ionic conductivity, in the form of mobile oxygen vacancies, which result in the variable resistance behavior. Since TiO_2 is known to be an n-type material, p-type Si wafers were chosen to create nanoscale p-n junctions at each metal oxide-pore interface and enhance barrier height offset. The next sections provide details on the porous silicon formation and the subsequent infiltration and crystallization of TiO_2 inside the pores.

3.1 PSi Electrochemical Etching

Porous silicon was formed by electrochemically etching planar single crystal silicon (p^+ type, <100> orientation, 0.01 Ω cm). The etching set-up consisted of a Teflon etch cell with a hole of 2 cm^2 area in the bottom, a platinum wire, an O-ring with an area of a 2 cm^2 and a silver plate as illustrated in Figs. 3.1-3.4. To etch PSi, the planar sample is placed on the silver plate and then the etch cell is positioned such that the hole is over the Si with the O-ring in between serving as a seal. The etch cell is then partially filled with hydrofluoric acid-based electrolyte consisting of 87.5% ethanol, 6.25% hydrofluoric acid and 6.25% H_2O. The platinum wire is submerged in the solution ~1 cm above the Si. When current is applied, the platinum wire serves as the cathode and the Si as the anode.

Figure 3.1 - Teflon etch cell. The etch cell contained a hole of 2 cm^2 area in the bottom which demarcates the area to be etched in the Si substrate place below

Figure 3.2 - Platinum wire. The platinum serves as the cathode when electrical current is passed during etching.

Figure 3.3 - O-ring. 2 cm^2 in area, the O-ring serves as a seal and is placed between the Si substrate below and the etch cell above.

Figure 3.4 - Silver plate. The silver plate serves as a conduction path for the current to flow through to the Si which serves as the anode during the electrochemical etch.

The pore depth and diameter are controlled via the etch current density and duration of etching. The PSi films produced in this work were etched for 2000 s at 20 mA/cm^2 of etch current density to produce a film with a depth of 30 µm. For initial devices fabricated, the pore depth was maintained at ~4 µm. However, electrical characterization for these initial devices did not yield expected results as the memristance effects observed were not pronounced enough due in part to a surface layer of TiO_2 that was present on the devices and was thought to obscure the measurement results. Therefore, the pore depth was increased to 30 µm to increase the amount of nanocrystalline TiO_2 in the pores and the resulting memristance effects of the nanocomposites.

3.2 TiO_2 Deposition

3.2.1 TiO_2 Sol-Gel Development

Deposition of TiO_2 was carried out by precipitating a TiO_2 sol-gel precursor into the PSi film layer. This particular deposition process was chosen because it provides a relatively simple and inexpensive means of producing TiO_2 over other deposition processes such as atomic layer deposition and sputtering, and it was hypothesized to be the method with the highest likelihood of effectively infiltrating into the nanoscale pores. TiO_2 sol-gel precursors are reported to have been developed from various compounds such as titanium (IV) butoxide [58] and titanium isopropoxide [59]. For this experiment, titanium ethoxide or $Ti_4(OCH_2CH_3)_{16}$ was chosen to create the sol-gel precursor [60]. The sol-gel was developed by dissolving 1g of titanium ethoxide into a solution of 10 mL of isopropyl alcohol and 0.1 mL of hydrochloric acid. The mixture was stirred for 30 minutes at 500 RPM on a hot-plate set to 60°C to allow the titanium ethoxide to be completely dissolved.

3.2.2 TiO_2 Sol-Gel Deposition and Annealing

The sol-gel precursor was deposited by completely submerging the PSi film into the sol-gel for 30 minutes. The sample was then removed from the sol-gel and rinsed with ethanol both to remove any large precipitates on the surface which might inhibit further infiltration of the pores by the sol-gel as well as to maintain a smooth surface for subsequent metal-contact deposition. The sample was then heated on a hot-plate at 100° C for 1 min to evaporate solvents present within the pores and to allow increased infiltration. The sample was then completely submerged into the sol-gel for another half-hour and all of the previous steps were repeated a second time. This two-step deposition process was performed because prolonged, uninterrupted deposition

times were unsuitable as the sol-gel accumulates on the PSi surface and prevents further filling of the pores.

After deposition, the sample was annealed at 500 °C in air for 1 hour at a ramp rate of 10 °C/min to promote formation of TiO_2 from the sol-gel precursor. At low annealing temperatures such as 500 °C, anatase phase of TiO_2 is expected to be present [61, 62]. Anatase is known to be oxygen deficient and the number of vacancies can be controlled via adjustment of the TiO_2-film thickness and annealing conditions [63]. These vacancies are postulated to be responsible for changing the film conductivity when they move under an applied electric field.

3.3 Photolithography and Metal Deposition

Following TiO_2 deposition, metal contacts were patterned on the TiO_2-PSi surface by conventional photolithography and thermal evaporation of metals. During photolithography, Shipley 1813 was spun onto the samples at 5000 RPM for 45 s using a CEE spin-bake system. The samples were then exposed using a Karl Suss MA-6 mask aligner and developed in tetramethylammonium hydroxide (TMAH) developer for 30 s. Prior to metal deposition, an O_2-plasma reactive ion etching step was carried out using an Oxford Instruments PlasmaPro 100 Cobra to remove residual photoresist that was not removed by the TMAH developer after photolithography. This RIE step is necessary to ensure proper metal contact adhesion to the surface.

The electrical contacts were formed by thermal evaporation in an Angstrom Amod deposition tool and consisted of a Cr/Au layer. The Cr layer was deposited between the sample surface and the Au layer to promote adhesion of the Au contacts. Therefore the Cr layer was only a fraction of the thickness of the Au layer (Au ~ 120 nm, Cr ~ 20 nm). The spacing between the patterned

contacts ranged from 5-50 μm. After the metal deposition, an acetone soak was required to remove the excess metal deposited on top of the photoresist while preserving the patterned metal contacts. Finally, the devices were subjected to a 5 min 500 °C anneal step to promote adhesion of the metal to the device surface. Better adhesion minimizes the potential for resistive losses at the electrode/nanocomposite interface.

Chapter 4: Results

Both material and electrical characterization of the TiO_2-PSi devices were performed. Material characterization confirmed both infiltration of TiO_2 in the pores as well as the crystallinity of the metal oxide. Imaging of the devices by scanning electron microscopy (SEM) on a Raith eLine tool and transmission electron microscopy (TEM) on an FEI Technai Osiris was used to confirm the forming of metal electrodes on the TiO_2-PSi substrate and verify the crystalline nature of the material in the pores. Energy dispersive x-ray (EDX) spectroscopy was performed using a Bruker tool on the cross section of a sample to to provide an elemental mapping throughout the PSi layer. Raman spectroscopy, performed using a confocal Thermo Scientific DXR Raman microscope, was used to identify the specific crystalline phase of TiO_2 in the pores. X-ray diffraction (XRD) measurements, performed using an PANalytical Powder Diffractometer (X'Pert Pro) with CuK_α source (λ=1.54059 Å), were taken on a sample of TiO_2 annealed on a planar Si substrate to confirm the phase of TiO_2 present on the substrate. Electrical characterization was carried out using a Keithley 2400 voltage/current source-meter in conjunction with custom Labview routines to measure I/V pinched hysteresis loops and state-retention properties.

4.1 Material Characterization

An SEM image of a fabricated device is shown in Fig. 4.1. which shows the top view of a device after completion of metal deposition. The particular device shown had a spacing of 50 µm between the interdigitated contacts.

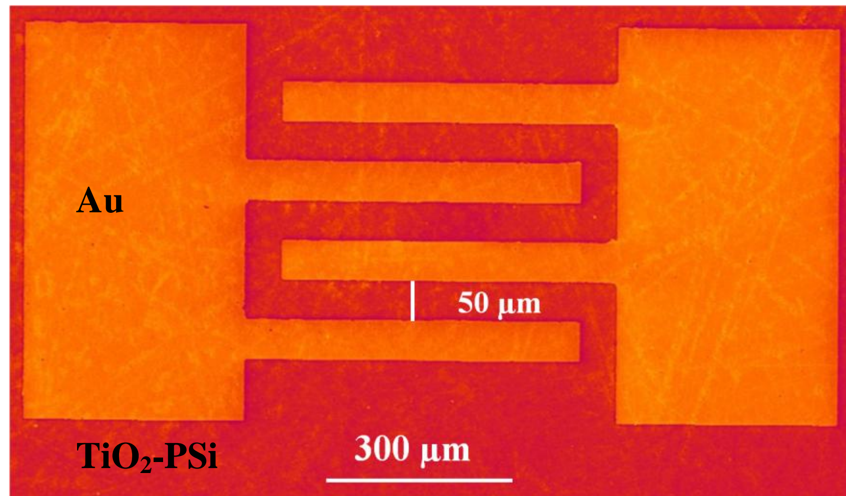


Figure 4.1 – Top view SEM of a 50 µm device. A two terminal device (the two rectangular areas at the ends) with interdigitated contacts separated by 50 µm is shown.

The elemental mapping shown in Fig. 4.2 confirms that Ti is uniformly present throughout the length of the 30 µm deep pores. This suggests that the ratio of TiO_2:PSi is consistent enough throughout the device that negligible variation in the electronic properties of the device as a function of PSi film depth is expected. Silicon and oxygen are also present in the elemental maps. The presence of oxygen is due to both the TiO_2 and SiO_2 in the nanocomposite.

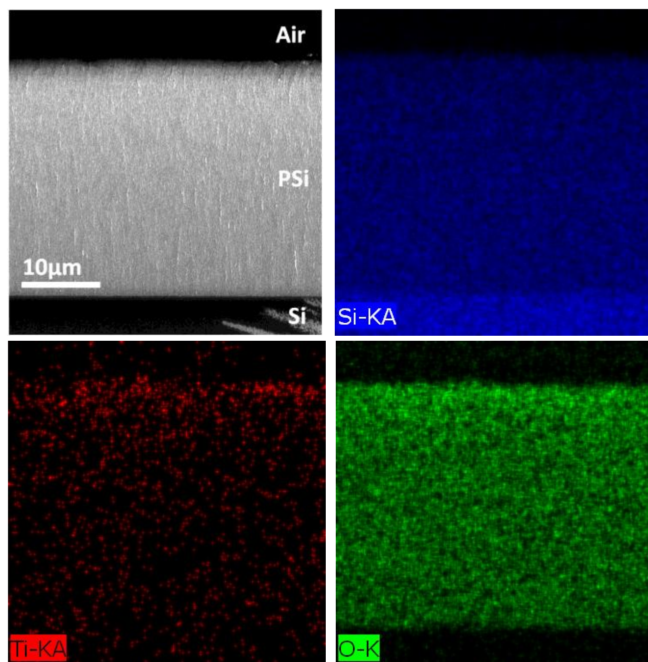


Figure 4.2 - Elemental mapping of device with 30 µm deep pores. The mapping reveals near uniform distribution of Ti and O throughout the length of the pores. Note that some O present may be due to SiO_2 that forms during the annealing process.

Given the annealing temperature of 500 °C used for the fabrication of the devices, the anatase phase of TiO_2 was expected to be the dominant phase present within the devices [61, 62]. From the XRD spectra in Fig. 4.3, the crystal structure of TiO_2 on a planar silicon substrate after annealing at 500°C was determined to be anatase based on the strong anatase peak shown at 25.3° - 2θ. As the annealing temperature is increased above 900 °C, the peak shifts to ~27.5° - 2θ, which is the characteristic peak for rutile. Note that the XRD data was obtained from TiO_2 deposited on planar Si by spin coating because there were no detectable peaks attributable to TiO_2 when taken from the PSi film due to the limited amount of TiO_2 available for reflection compared to the Si, given the nanoscale dimensions of the pores.

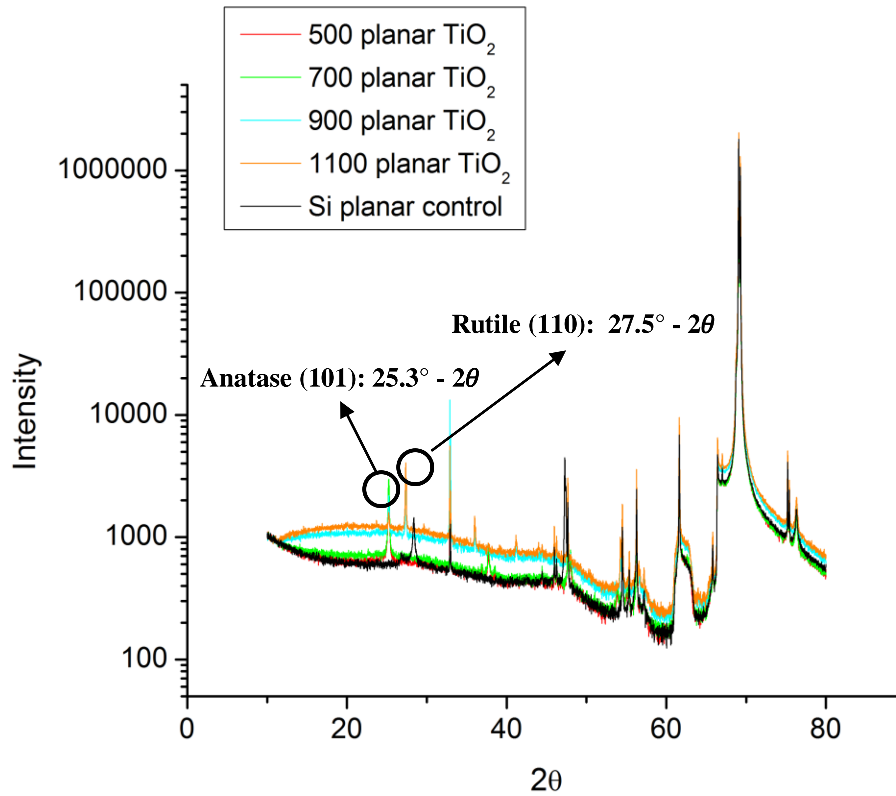


Figure 4.3 - XRD spectra of TiO_2 on planar Si. At annealing temperatures less than 900°C, anatase exhibits a strong peak whereas at 900°C and higher temperatures, a strong peak for rutile is observed.

The anatase structure of TiO_2 in PSi was confirmed by the Raman spectrum shown in Fig. 4.4. The Raman shifts seen in the spectrum at approximately 151 cm^{-1} and at 639 cm^{-1} are close to the primary characteristic shifts associated with the anatase phase of TiO_2 [64-66]. In addition, the characteristic PSi Raman shift is at 520 cm^{-1} or lower in wavenumber depending on the etching current and etching time used for the fabrication of PSi from planar Si [64]. A peak at 940 cm^{-1} indicates second order Raman scattering by Si [67].

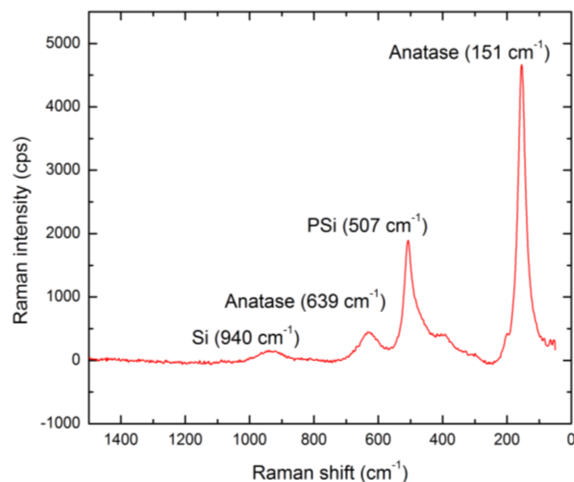


Figure 4.4 - Raman spectrum of TiO_2 in PSi. The spectrum indicates that anatase phase of TiO_2 is present (with peaks at 151 cm^{-1} and at 639 cm^{-1}) along with the PSi (~ 507 cm^{-1}) and Si (940 cm^{-1}) substrates.

Additional imaging by TEM on TiO_2 nanoparticles fabricated by annealing the sol-gel precursor on a planar Si substrate, shown in Fig. 4.5, provides visual confirmation of the crystal structure.

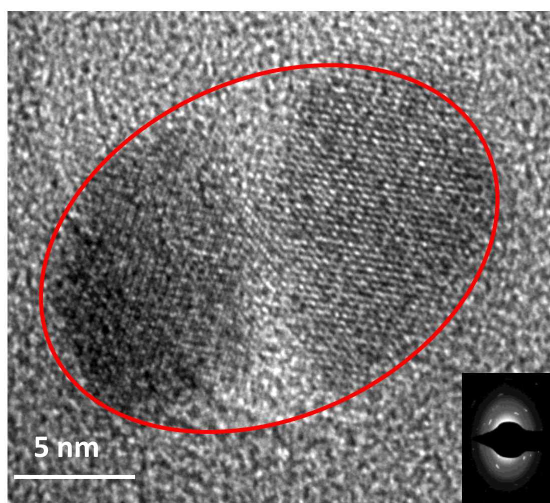


Figure 4.5 - TEM image of TiO_2 nanoparticles. The crystalline nature of the fabricated TiO_2 nanoparticles is evident in the TEM image. The nanoparticle is enclosed within the red boundary outlined in the image. **Inset - Electron diffraction pattern of TiO_2.**

4.2 Electrical Characterization

Electrical characterization of the TiO_2-PSi nanocomposite was performed using a Keithley 2400 source meter along with custom written Labview routines to measure the *I/V* pinched hysteresis characteristics and state-retention properties. *I/V* hysteresis loops were measured by applying sinusoidal voltage sweeps to the devices whereas state retention of the TiO_2-PSi hybrid films was determined by applying sequential voltage pulses with varying duty cycle and a time delay between each pulse.

4.2.1 I/V Hysteresis Loops

Fig. 4.6 shows the *I/V* curves of a 50 μm device obtained by applying multiple iterations of a sinusoidal voltage signal of 1 Hz with increasing magnitude from 140 V to 210 V (28 kV/cm - 42 kV/cm) and measuring the resulting current. The pinched hysteresis loops obtained are a characteristic feature of memristive devices serving to confirm that the devices do possess variable resistance properties [15, 28, 31]. The *I-V* hysteresis loops demonstrate that the resistivity of the device was lower at higher voltages as is expected of such systems exhibiting variable conductivity. Another distinguishing feature of these hysteresis curves is their non-crossing behavior at the origin. This is a strong indicator of the prominent mechanism contributing to the variable resistance phenomenon that is attributed to the accumulation of ionic defects at the metal-oxide/PSi interfaces, as will be discussed in section 4.2.3.1

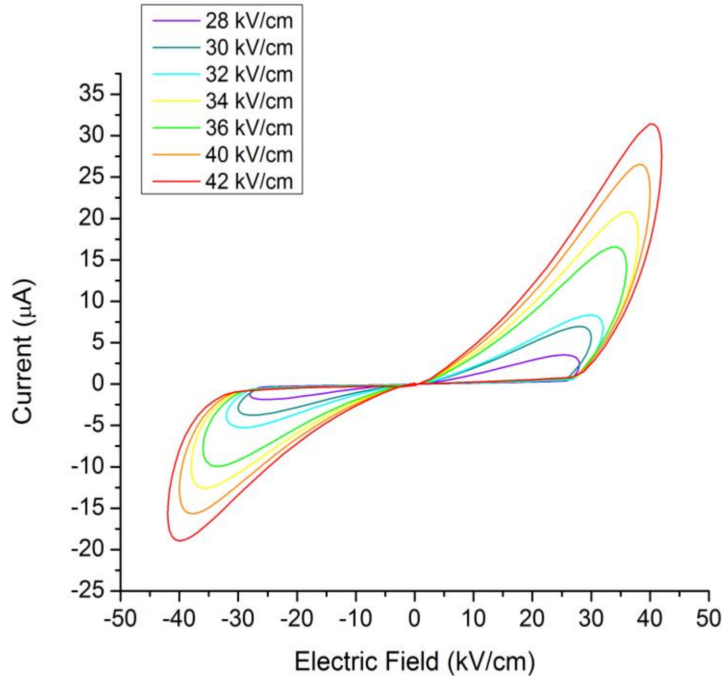


Figure 4.6 - Pinched hysteresis loops. The *I/V* hysteresis loops of the TiO_2-PSi devices were well-behaved with loops at lower voltages fully enclosed within those at higher voltages.

The hysteresis loops shown in Fig. 4.6 demonstrate well-behaved *I/V* characteristics with high values of resistance generally observed for the device. At 210 V (42 kV/cm), the highest resistance measured due to positive applied voltages is 6.5 MΩ along with a maximum current of 31.4 μA. Similarly, when -210 V (-42 kV/cm) is applied, the maximum resistance and current measured is 10.8 MΩ and 18.9 μA, respectively. Regarding the voltage at which the resistance begins transitioning from a high to a low value to allow greater magnitudes of current to flow through the device, the transition point for positive voltages is at ~133 V (26.6 kV/cm) where the instantaneous resistance of the device is 163.8 MΩ. The negative transition voltage is ~-153 V (30.6 kV/cm) and the instantaneous resistance measured at this applied voltage is 156.8 MΩ. The

mechanism behind the switching of resistance states at these transition points is discussed in section 4.2.3.1.

4.2.2 State Retention

In the case of a linear resistor, a plot of constant voltage pulses and measured current would show a train of equal current pulses ordered in time as the resistance is independent of current or voltage. However, the TiO_2-PSi devices are expected to have a dynamic range of resistance values which are dependent on the current and previous biasing conditions, thereby implying that the current obtained from a series of constant voltage pulses would result in variations in current that depend on the magnitude, polarity, and pulse time. Fig. 4.7 shows such a plot created from data from a device with a 15 μm device spacing. The data was acquired by applying 50 sequential 100 V (66.7 kV/cm) pulses with a pulse duration of 2 s and 1000 s delay time between the start of each pulse.

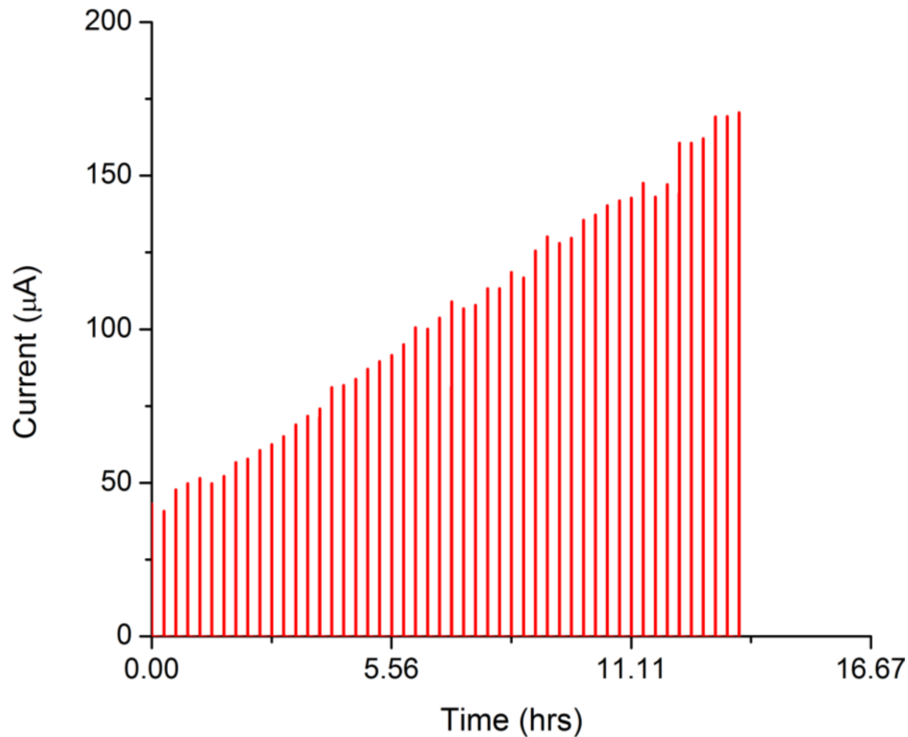


Figure 4.7 - State retention of 15 μm TiO_2-PSi device with 100 V (66.7 kV/cm) input pulses. The current response to each voltage pulse begins at the termination of the previous current measured. There was a 1000 s delay time between each pulse and each pulse had a duration of 2 s. The measured increase in conductivity is uniform and the device thus holds multiple resistance states over the course of the experiment.

The state persistence graph shown in Fig. 4.7 matched expectations for a memristive device as each current measured due to a voltage pulse applied originated at the point of termination of the previous current. Each current value was measured at the end of the input pulse's duration. In addition, the conductivity of the device is observed to increase with increasing application of voltage. Increasing the delay between each voltage pulse to 2000 s while reducing the voltage to

45 V (45 kV/cm) for 32 cycles resulted in a similar retention of the resistance state as shown in Fig 4.8. The device used for this state persistence test had a 10 μm spacing interdigitated contact.

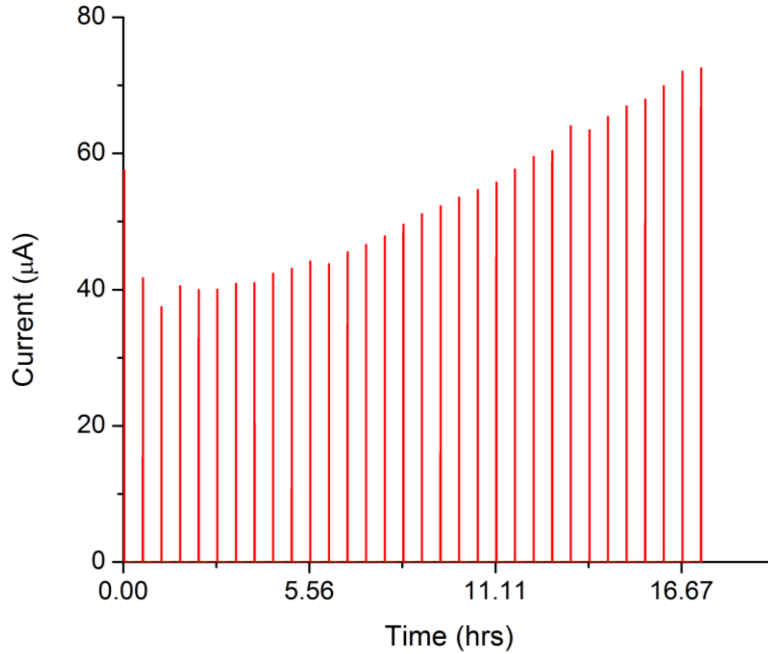


Figure 4.8 - State retention of 10 μm TiO_2-PSi device with 45 V (45 kV/cm) input pulses. Similar to Fig 4.7, the resistance state is retained by the device at zero bias as each current pulse starts at the point of termination of the previous one. There was a 2000 s delay between each pulse and each pulse had a duration of 2 s. The first current response can be deemed an anomaly, possibly occurring as a result of parasitic capacitance of the device.

For the state retention graph in Fig 4.7, the resistance of the device was observed to decrease from an initial 2.5 MΩ to 586.3 kΩ, a decrease of nearly 4 times by the end of the constant application of the 100 V pulses. As for the graph in Fig 4.8, the resistance range was seen to vary from 1.2 MΩ to 620.4 kΩ under the bias of 45 V sequential pulses. As the delay between voltage pulses was increased beyond 2000 s, the devices began losing their ability to retain their resistance states. The reasons for why such a loss of memory occurs and the dynamic range of

resistances observed for these devices, which can have important applications in analog memory circuits as well as for multi-bit storages, are discussed in section 4.2.3.2.

4.2.3 Discussion

4.2.3.1 *I/V* Hysteresis Loops

As noted above, the hysteresis loops obtained from the nanocomposite devices were observed to be non-crossing at the origin as is evident in Fig 4.9 which is a close-up around the origin of the hysteresis curve at 42 kV/cm from Fig 4.6.

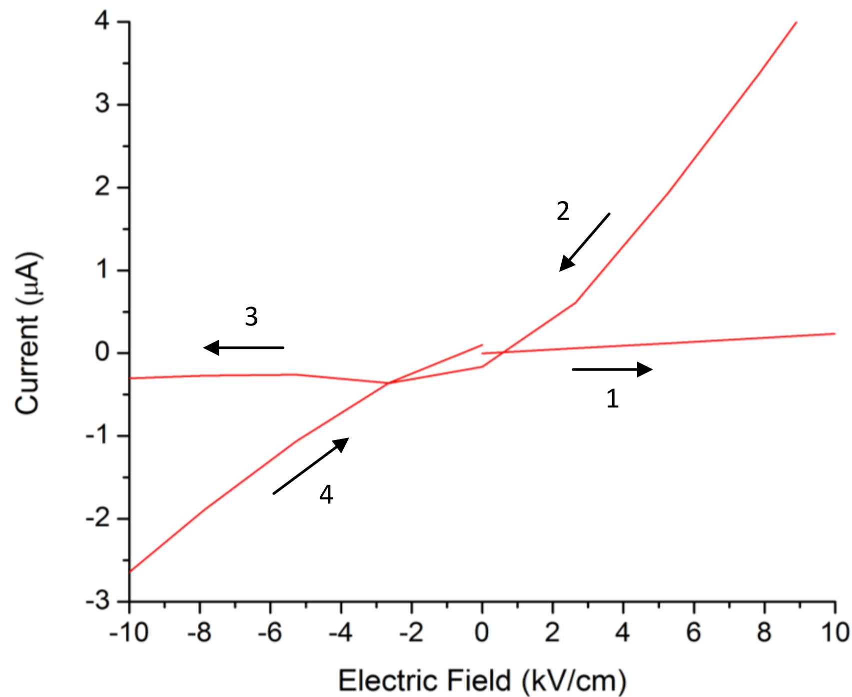


Figure 4.9 - Non-crossing hysteresis behavior. A closeup of the hysteresis loop at 42 kV/cm from Fig. 4.6. Following the numbered arrows, which indicate how current changes as voltage is changed, indicates that the hysteresis is non-crossing at the origin. Were the hysteresis to be crossing, arrows numbered 3 and 4 would switch locations.

The numbered arrows in the figure indicate the direction of current as the voltage is changed in magnitude and polarity. It can be inferred from the figure that the type of hysteresis obtained is non-crossing since the slope of the *I/V* curve abruptly changes as negative voltages are applied. Had the device exhibited crossing hysteresis, the same slope in the region of arrow 2 would have been maintained for the next region containing arrow 3. In other words, arrows 3 and 4 would have switched locations for a crossing hysteresis. This is exactly what is shown in Fig 4.10, a simulated graph of a crossing hysteresis akin to a perfect figure-8. The arrows indicate how the *I/V* curves are expected to intersect at the origin for a crossing, passive memristor device. The significance of whether the hysteresis loops cross or not lies in the insight it provides on the particular mechanism contributing to the variable resistance behavior of a device.

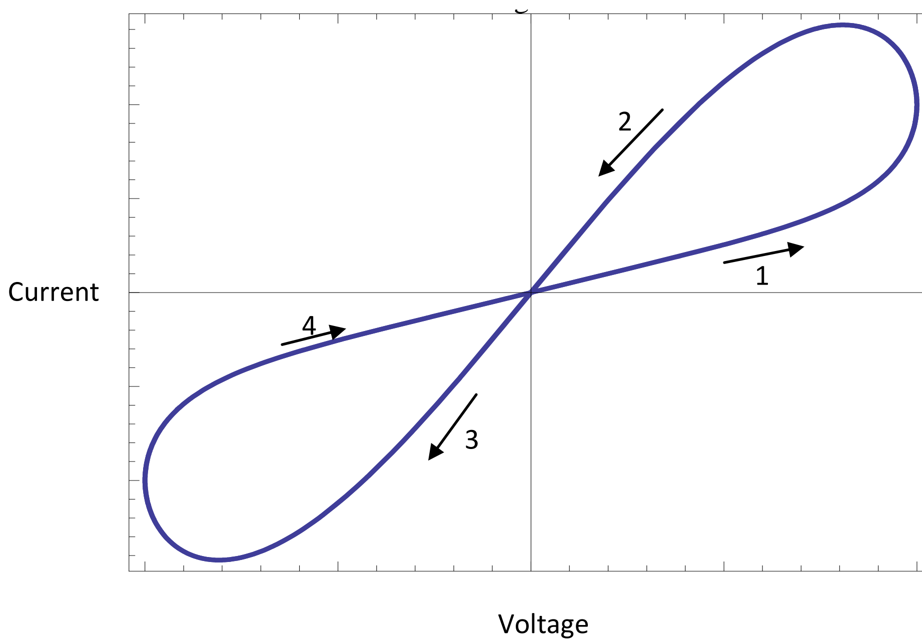


Figure 4.10 - Simulated graph of a crossing hysteresis *I/V* curve. In contrast to the graph in Fig 4.9, the current changes force the *I/V* curve to intersect at the origin producing a crossing hysteresis curve.

TiO_2-PSi devices fabricated in this experiment are believed to rely on the migration of point defects in the form of oxygen vacancies in the metal oxide for the variable conductivity

measured in the material system. Ionic defect accumulation at the pore wall/metal-oxide interface is proposed as the primary mechanism for variable conductivity in the TiO_2/PSi devices and also explains the particular nature of the non-crossing hysteresis loop. This mechanism is similar to the model proposed by Mares *et al.* [16] which uses a nickel oxide-PSi composite materials system. In the case of anatase TiO_2 used for the experiment, the native defects are believed to be primarily composed of oxygen vacancies instead of titanium interstitials since the metal oxide was annealed for a prolonged time [56]. The n-type conductivity in TiO_2, however, can most probably be attributed to titanium interstitials.

Infiltration of the p-type PSi with this n-type TiO_2 essentially creates p-n junctions at the numerous TiO_2-PSi interfaces. Ionic species, in the form of oxygen vacancies for TiO_2, migrate to a particular side in each of these TiO_2-PSi interfaces on application of an electric field. The accumulation of these vacancies creates an energy barrier height at that particular pore wall-Si junction that must be overcome by charge carriers.

The following considerations are given to the measured hysteresis curves. At 0V, the oxygen vacancies are assumed to be evenly distributed throughout the pores. As the voltage (electric field) begins to increase, the charge carriers begin to flow through the device, but at low currents due to the energy barriers encountered at the pore wall/metal-oxide interfaces. However, along with the electronic charge conduction, the oxygen vacancies also begin to slowly migrate towards one side of the pores under the applied electric field. As the field continues to increase, ionic defects accumulate at one side of the pores to cause additional energy states to exist near the junctions. The new energy states allow electrons to easily hop to these conduction states thereby increasing conductivity. This mechanism effectively reduces the energy barrier height at one side while the defect depleted side becomes more and more forward biased such that current

flow is effectively limited only to ohmic losses. This transition point appears to occur at approximately at 26.6 kV/cm in the hysteresis curves presented in Fig 4.6 earlier.

As the voltage continues to push past this transition point, the current rises rapidly and seems to only be limited by the maximum voltage applied in each cycle. This initial positive increase in the electric field exhibits strong diode-like behavior; however, once the voltage begins to decrease, the current follows a distinctly different path which shows a much more linear, ohmic-like behavior until the voltage returns to zero. As the voltage crosses the zero point, the current changes direction and now the opposite side of the pore is depleted of oxygen vacancies causing the junction to possess a Schottky-like barrier and the resistance state of the device is now high. Increasing the magnitude of the voltage in the negative direction causes the defects to drift towards the opposite interface, and the transition from an HRS to an LRS is observed at around 30.6 kV/cm. Finally, when the voltage is switched from negative to positive, the device exhibits a HRS again. This process explains the origin of the non-crossing behavior of the hysteresis curves: the abrupt jump from low-resistance to high-resistance after crossing the origin.

The behavior of these TiO_2/PSi devices are in contrast to the typical crossing loops governed by the predominant controlling mechanism reported by most other variable resistance type devices, namely the formation of conductive filaments [5, 68]. However, the assumed mechanism responsible for the TiO_2-PSi device behavior here and the theory of conducting filaments have in common their dependence on the migration of ionic species [3-5]. The role filaments play in other variable resistance devices is to establish low-resistance conducting channels between the two electrodes after an electric field has been supplied across the contacts for a sufficient time. Prior to this, the device is in a HRS. In observing *I/V* hysteresis in these other devices, once the conducting filament has been established it can only be dismantled when a sufficient electric

field is applied with the opposite polarity. Thus the device will stay in the LRS through the origin producing a crossing *I/V* hysteresis curve. This type of behavior is known as bipolar operation: positive polarity is needed to set the device in the LRS and negative polarity is needed to RESET the device in the HRS [5, 69].

Alternatively, some conducting filament devices also exhibit unipolar switching where the device is SET and RESET by applying the same polarity. In unipolar devices, once the conductive filament is formed, a large current can flow over time but increasing the voltage can rupture the filament due to Joule heating effectively RESETTING the device in the HRS. Hysteresis curves obtained from a device based on this mechanism would be crossing at the origin. While the formation of conductive filaments in the TiO_2-PSi devices cannot be entirely ruled out, the hysteresis behavior would be expected to be crossing at the origin if this were the controlling mechanism, providing strong evidence that the dominant mechanism for these composites is the accumulation of ionic defects at the numerous metal oxide-Si junctions with applied electric field, which sets up a dynamic barrier height.

4.2.3.2 State Retention

While hysteresis curves provide evidence of a variable resistance device as well as provide insight to the underlying working mechanisms, in order to be useful as a non-volatile electronic memory component, the device must be capable of retaining the resistance-state for prolonged periods without bias. The plot in Fig. 4.7 shows that for consecutive 2 s 100 V (66.7 kV/cm) pulses, the current increases linearly without reaching a saturation point, meaning that a limiting number of oxygen vacancies at the pore wall interface has not been reached. Were this limit to be reached, the conductivity would not increase as linearly and would be expected to remain

constant. The increase in conductivity with each pulse also strongly matches the prediction of the defect migration model which suggests that conductivity increases as a greater number of defects in the form of oxygen vacancies drift towards the TiO_2-PSi pore wall interface.

Furthermore, a close up of a single pulse in Fig. 4.11 shows that for each individual input pulse, there appears to be a logarithmic increase in the current response over the duration of the pulse, with the resistance value at the end of the previous pulse approximately equal to the beginning resistance of the next pulse.

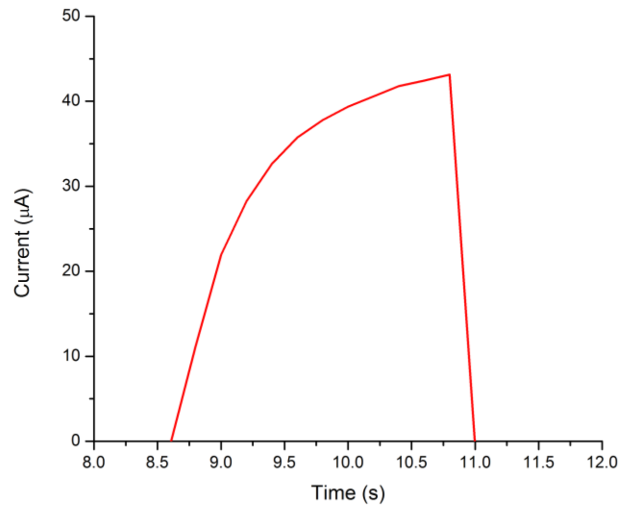


Figure 4.11 - Close up of the current response of a TiO_2-PSi device to a single voltage pulse. The increase in current can be explained by the model of electromigration of oxygen vacancies to a TiO_2-Si interface. The accumulation of these vacancies at the interface increases conductivity.

This data provides strong evidence for the state-retention ability of these devices since the nanocomposites retain the previous resistance-state throughout the duration of zero bias. The retention of the resistance state suggests that after migration of the defects under an applied

electric field, the oxygen vacancies are thermodynamically locked-in to their spatial position up to at least 1000 s. However, even assuming some finite relaxation time for the defects to migrate back and cause the device to fall out-of-state, as long as the next voltage signal is applied before this relaxation occurs, the state can be preserved.

It is important to note that the devices tested in this experiment yield a continuum of resistance states which can be utilized in analog memory technology. These devices could be used as binary, ON-OFF, resistive switches [70, 71] by arbitrarily choosing two discrete resistance states. State-retention times for binary switching in metal oxide-based memory devices have been reported in literature to be greater than 10 years [12]. These switches are binary memristive devices that exhibit two discrete resistance states of ON and OFF. The existence of two states results in better stability and greater retention times in contrast to memristive devices with multiple resistance states. In such continuous state memristors, gradual change in resistance states might increase the difficulty of retaining specific states. Nevertheless, relaxation times greater than 1000 s were measured for a 15 μm TiO_2-PSi device, which is almost 10^9 times greater than the update time necessary for conventional DRAM - about once every few microseconds. State retention testing on a 10 μm TiO_2-PSi device with 45 V (45 kV/cm) pulses showed that a relaxation time in excess of 2000 s is also possible (Fig. 4.8). The retention times observed for these devices exceeds typical times observed for other continuous state nanoscale memristive devices by a few orders of magnitude [72]. Owing to their multiple conduction states, TiO_2-PSi devices are a promising candidate for multi-bit storage applications where any discrete number of bits can be used as long as the resistance states are sufficiently distinguishable in value.

Chapter 5: Conclusion and Future Work

A nanocomposite device consisting of TiO_2 and PSi was fabricated and shown to exhibit memristance characteristics. The fabrication of the material system involved infiltration of TiO_2 into PSi using a sol-gel deposition method and subsequent annealing process to yield anatase TiO_2 in the pores. The presence and specific phase of TiO_2 was confirmed via XRD, EDX and Raman spectroscopy measurements. The resulting composite nanostructure was effectively a combination of nanoscale memristors that enabled variable resistance to be realized at the macroscale level. Thus, the spacings between the metal electrodes for the devices varied in the micron range as opposed to in the nanometer range.

The memristive nature of the nanocomposite TiO_2-PSi material system was verified through *I/V* and state retention measurements. The *I/V* measurements showed a pinched hysteresis loop, a characteristic fingerprint of a memristor. Analysis of the non-crossing nature of the loops at the origin supported the model that ionic migration of defect species, resulting in a dynamic barrier height at the interfaces of TiO_2 and PSi, is responsible for the variable resistance phenomenon observed in the devices. In the case of TiO_2, the defect species migrating are believed to be oxygen vacancies. State retention tests also supported the proposed mechanism of migration of oxygen vacancies as the conductivity of the devices was observed to increase over the application period of the input voltage pulses, a phenomenon that can be attributed to the accumulation of defects at the TiO_2-PSi interfaces.

Well-behaved hysteresis curves and state retention times on the order of approximately 2000 s make the TiO_2-PSi devices produced in this work a viable candidate for several nonvolatile memory applications. Although memristive and resistive memory devices are often studied for

possible use in digital memory, the TiO_2-PSi composites created here can be more effectively applied as analog memory elements or in high power applications due to the large electric fields involved in observing resistance switching in these devices. The variability in device sizes and the inherent tunability of PSi, however, mean that the material system can be easily adapted for use as digital memory or even for yet unexplored fields of neuromorphic computing owing to the similarity between the memristive network and the neural network. As device sizes decrease, the electric fields required to observe pronounced variable resistance also decrease.

Further work can be performed on this project to increase the stability of the TiO_2-PSi nanocomposites. It has been observed that with repeated electric characterization tests, over time, a change in the electrical properties of the devices are observed. Specifically, the openness of the *I/V* hysteresis curves appears to decrease after repeated cycles of sinusoidal voltages applied to the devices. A possible reason for this degradation in devices can be attributed to the probes used for electrical measurements and the resistive losses introduced by them. The additional resistive losses would create increased Joule heating due to high electric fields applied and therefore lead to damaged contacts on the devices. A proposed way to prevent the degradation of the devices is to wire bond the metal contacts on the nanocomposites. This method of forming contacts can help reduce resistive losses associated with the electrical probes being used.

Once stable devices have been obtained, irradiation can also be performed on the devices to ascertain any change in electrical properties during the process. Two main types of irradiation can be performed to observe the effects on the devices - x-ray and proton irradiation. The electrical properties of the devices, specifically *I/V* hysteresis, would be measured in-situ and compared to tests before the device to verify whether there is any loss in the memristance properties of the devices due to irradiation.

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