LAYOUT-AWARE MODELING AND ANALYSIS METHODOLOGIES FOR TRANSIENT RADIATION EFFECTS ON INTEGRATED CIRCUIT ELECTRONICS

By

Jeffrey S. Kauppila

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Approved:

Lloyd W. Massengill, Ph.D.

Ronald D. Schrimpf, Ph.D.

W. Timothy Holman, Ph.D.

Bharat L. Bhuva, Ph.D.

Mark N. Ellingham, Ph.D.

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DEDICATION

This dissertation is dedicated to my wife, Amy, and daughters, Audrey and Abigail. Their prayers, support, and patience over the course of this research are greatly appreciated.

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“Now to him who is able to do far more abundantly than all that we ask or think, according to the power at work within us, to him be glory in the church and in Christ Jesus throughout all generations, forever and ever. Amen.” Ephesians 3:20-21 (ESV)

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CHAPTER I

INTRODUCTION

The interaction of ionizing radiation with semiconductor materials results in the creation of electron-hole pairs. In the presence of an electric field across a semiconductor device junction, these carriers are separated by the electric field, resulting in the generation of a transient current at the device terminals. The utilization of integrated circuits in space and defense applications that will be exposed to transient radiation environments must account for the impact of the environment on the operation of the circuit. With the increasingly simulation analysis driven design of integrated circuits, and the increased cost to fabricate designs in advanced technologies, designers must consider radiation effects during the design phase to limit the number of fabrication and test cycles required to obtain a radiation hardened part.

For years, there have been circuit simulation models for transient radiation effects, however with the advancement of technology, new modeling methods must be developed to account for the complex geometries, circuit response speeds, and bias-dependent effects on the radiation induced transient currents. This work advances the historical modeling approaches and utilizes device physics models to develop bias-dependent and device layout-aware methods for modeling the response of dose rate and single-event effects in advanced integrated circuit technologies. The models account for geometry scaling, bias-dependence, and circuit feedback response on the generation and collection of radiation induced transient currents. Behavioral modeling languages are utilized to integrate the calculation of geometrical scaling

and bias-dependence with the transient current generation sources, eliminating the use of independent current sources and lumped SPICE element models.

A novel modeling and simulation method, accounting for circuit layout dependence and device spacing has been developed and demonstrated for bulk CMOS technologies. The layout-aware modeling methods and analysis address multiple device charge collection effects in bulk technologies, which have led to a strong layout dependence on the response of integrated circuits to radiation stimuli. The layout-aware analysis capability is demonstrated in the analysis of multiple flip-flop designs and in the analysis of a single-event hardened operational amplifier.

The methods developed in this work are being utilized in radiation-effects research activities at universities, aerospace and defense organizations, and commercial integrated circuit design and manufacturers. Layout-aware radiation-enabled models using the methodologies developed in this work have been integrated with process design kits and deployed to the radiation-hardened by design community.

As integrated circuit technologies continue to scale to the sub-20nm regime and disruptive technologies, e.g. FinFETs, the radiation response of devices and circuits will be increasingly dependent on the layout of the device and circuit, as well as the location of the electron-hole pair creation with respect to the device. The reduced feature size and increased device density will result in an increased susceptibility to low energy transient radiation induced faults. The modeling and analysis methodologies developed in this research are scalable to sub-20nm and non-planar technologies and will enable designers to assess the susceptibility of integrated circuit components to transient radiation effects during the development and design phase, resulting in increased first or early pass success in the design and function of integrated circuits

intended for use in applications that include transient radiation environments.

Dissertation Organization

This dissertation begins with an overview of transient radiation effects and existing modeling methods found in the literature for the dose rate and single-event radiation environments. TCAD simulations in recent literature highlight the observation of a transient current plateau effect that results from the circuit response impacting the charge collection mechanisms. Chapter III develops methods to capture the bias-dependence of radiation-induced transient currents in behavioral models appropriate for use in circuit simulation and analysis. Modern integrated circuit technologies have complex 3-D structures and a wide variety of possible geometries used in design. Chapter IV details the advancement of the historical 1-D, limited geometry dose rate models to include scalability with layout geometries and real-time bias dependence, as well as lifetime and conductivity modulation as a function of carrier generation rate. Layout-aware, bias-dependent single-event modeling methods to capture charge sharing and parasitic bipolar junction transistor effects are developed in Chapter V. A novel automated layout-aware circuit analysis method utilizing standard integrated circuit design tools, single-event enabled models, and the circuit layout to assess vulnerability to single-event upset or transients is detailed in Chapter VI. Chapter VII discusses the impact of this work in the design of radiation-hardened circuits and the potential application of the developed methods to sub-32nm technologies, including disruptive, non-planar technologies.

There are three appendices included after the references. Appendix A describes methods for designing test structures used in the calibration and validation of the

compact models detailed in this work. Appendix B provides examples of freely available SPICE models of bulk CMOS, silicon-on-insulator CMOS, and bipolar junction transistors. The models can be utilized in simulation with the bias-dependent single-event model that is also included in Appendix B. Integration of transient radiation models with the baseline electrical SPICE models, from Appendix B, as well as a netlist demonstrating the layout-aware analysis parameterization of the single-event models are described in Appendix C.

CHAPTER II

TRANSIENT RADIATION EFFECTS ON ELECTRONICS

A fundamental mechanism in semiconductors is the generation of excess carriers as a result of energy absorption in the material. A photon with energy, or and ion depositing energy, in excess of the bandgap energy of the semiconductor can create an electron-hole pair by raising an electron from the valence band to the conduction band. The bandgap of silicon is 1.1eV, therefore deposited energy in excess of 1.1eV has the potential to generate excess carriers. However, much of the energy absorbed is thermalized in the lattice, therefore, an average of 3.6eV is required to produce an electron-hole pair in silicon [1], [2], [3], [4], [5]. In the presence of an electric field across a semiconductor device junction, the excess carriers generated near the junction may be separated by the electric field and traverse the junction, resulting in the generation of a transient current at the device terminals. High intensity transient radiation events can generate enough excess carriers in the presence of a junction to result in transient currents greater than the normal signal levels in many circuit applications [1].

Dose Rate Effects

When semiconductor devices are exposed to high intensity transient penetrating radiation pulses, often referred to a dose rate, prompt gamma, or gamma dot pulse, such as those obtained from pulsed reactors, flash X-ray machines, or linear accelerators, the carrier generation is essentially uniform through-out the device.

Wirth and Rogers developed closed form solutions of the transient photocurrents for idealized device geometries and junction profiles [1]. Using the average energy of 3.6eV for electron-hole pair production in silicon, it has been shown that a dose rate of one rad per second produces a generation rate of 4.3×10^{13} e-h pairs/cm^3-s [1], [2], [6].

The response of the P-N diode to a high intensity transient radiation pulse has been well characterized and the understanding scales to P-N junctions within integrated circuit semiconductor devices [1], [2], [7], [8], [6], [9], [10], and [11]. The uniform generation of excess carriers near a reverse biased P-N junction results in a transient photocurrent. The carriers generated within the depletion region of the junction will be swept across the junction by the built-in electric field, and are collected almost instantly. The holes are swept into the p-type region and the electrons into the n-type region, resulting in a current flow from the n-type to p-type region. This immediate collection of carriers is referred to as the prompt component of the junction photocurrent [1].

Carriers generated outside of the depletion region create a transient increase in minority carrier densities in the n-type and p-type regions. The carriers in the vicinity of the junction diffuse toward the junction. The carriers generated within one diffusion length of the edge of the depletion region, on average, will diffuse to the junction and be collected. Carriers generated outside of one diffusion length from the edge of the depletion region will likely recombine before reaching the junction, and therefore do not significantly contribute to the photocurrent. Carrier diffusion processes require a finite time to occur, therefore the diffusion component of the photocurrent is often referred to as the delayed component. As with the prompt current component, the

delayed current flows from n-type to p-type.

Existing models for the magnitude and duration of the prompt and delayed components of the transient photocurrent resulting from a dose rate pulse have been developed and will be discussed in the next section.

Dose-Rate-Enabled Modeling Landscape

In 1964, Wirth and Rogers published the landmark paper on modeling the drift and diffusion components of the primary and secondary prompt gamma generated photocurrent in silicon semiconductor devices [1]. The work done by Wirth and Rogers has been the foundation of dose rate modeling for decades. In 1983, Long et al., published a model for carrier lifetimes and diffusion through like doping high-low junctions, applied to epitaxial layers [7]. The carrier diffusion lengths and lifetime are modified as a result of carriers needing to move from a highly doped to low doped region of the device. Long et al. showed that the carrier movement is not simply satisfied by superposition of carrier lifetimes in each of the regions. Massengill implemented the Wirth and Rogers equations, as well as the diffusion length and lifetime modifications by Long, et al., in a time and voltage dependent current source in SPICE2 [8].

The Wirth and Rogers model is comprised of two components: (1) a prompt component produced by electron-hole pairs generated within the depletion region and (2) a component resulting from the diffusion of carriers generated near the depletion region. For a pulse of magnitude G and duration T, the Wirth and Rogers model is

evaluated as the system of equations

$$I_{PC}(t) = \begin{cases} 0 & ; t < 0 \\ qAG\left[X_D + L_{Dn} erf\left(\sqrt{\frac{t}{\tau_n}}\right) + L_{Dp} erf\left(\sqrt{\frac{t}{\tau_p}}\right)\right] & ; 0 \le t \le T \\ qAG\left\{L_{Dn}\left[erf\left(\sqrt{\frac{t}{\tau_n}}\right) - erf\left(\sqrt{\frac{t-T}{\tau_n}}\right)\right]\right. & \\ \qquad \left. + L_{Dp}\left[erf\left(\sqrt{\frac{t}{\tau_p}}\right) - erf\left(\sqrt{\frac{t-T}{\tau_p}}\right)\right]\right\} & ; t > T \end{cases} \tag{1}$$

where I_{PC} is the photocurrent at time t, q is the electron charge of 1.602×10^{-19} Coulombs, G is $4.3 \times 10^{13} \frac{e-hpairs}{cm^3 rad(Si)}$ times the dose rate in rad(Si)/s, A is the area of the junction, X_D is the depletion width of the junction, L_{Dn} and L_{Dp} are the minority carrier diffusion lengths for n-type and p-type silicon, and τ_n and τ_p are the minority carrier lifetimes for n-type and p-type silicon [1]. The depletion width is calculated as

$$X_D = \sqrt{\left[\frac{2\epsilon_s}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)(\phi_i - V_a)\right]} \tag{2}$$

where ϵ_s is the permittivity of silicon, N_a is the acceptor doping concentration in the p-type silicon, N_d is the donor doping concentration is the n-type silicon, ϕ_i is the built in potential, and V_a is the bias across the junction [3]. The built in potential is

$$\phi_i = \frac{kT}{q} ln \frac{N_a N_d}{n_i^2} \tag{3}$$

where k is Boltzmann's constant, T is the temperature in Kelvin, and n_i is the intrinsic carrier concentration of silicon, which is $1.45 \times 10^{10} cm^{-3}$ [3]. The minority carrier diffusion length in (1) is calculated as

$$L_D = \sqrt{D\tau} \tag{4}$$

where D is the minority diffusion constant, which is calculated as

$$D = \left(\frac{kT}{q}\right)\mu \tag{5}$$

where μ is the minority carrier mobility. τ in (4) is the minority carrier lifetime [3].

Long et al. developed a model to calculate the diffusion length and carrier lifetime to account for the use of highly doped epitaxial layers in integrated circuit manufacturing. The epitaxial layer results in a junction of highly doped and low doped like-type silicon. When the collection volume encompasses a high/low junction, the diffusion length calculation is modified as

$$L_1 = L \cdot tanh\frac{W}{L} + \frac{L^+}{cosh\frac{W}{L}} \tag{6}$$

where L_1 is the modified diffusion length for the high/low junction, L is the low doped side diffusion length, L^+ is the high doped side diffusion length, and W is the undepleted epitaxial width [7]. The lifetime for the minority carriers in the high/low junction is modified as

$$\tau_1 = \frac{L_1^2}{2D} \tag{7}$$

where D is the diffusion constant for the low doped side and L_1 was calculated in (6). The modified diffusion length and lifetime parameters are substituted into (1), when the collection volume encompasses the high/low epitaxial junction.

Enlow and Alexander published a model for high injection minority carrier transport [9], which was updated in the model developed by Wunsch and Axness [10]. The Wunsch paper in 1992 provided the most comprehensive time domain solution to the dose rate induced photocurrent, building upon the work of Wirth and Rogers, Long et al., and Enlow and Alexander [10], however the full model derivation is not available in published work [2], [12]. Fjeldly has developed a combined expression model for minority carrier lifetime across low, high, and Auger carrier injection

regimes [11]. The unified minority carrier lifetime is calculated as

$$\tau = \left(\frac{1}{\tau_1} + \frac{1}{\tau_a}\right)^{-1} \tag{8}$$

where τ_1 is the dose rate dependent minority carrier lifetime in the Shockley-Read-Hall (SRH) regime, which covers low-injection to the saturation of SRH traps and τ_a is the minority carrier lifetime in the Auger regime. The dose rate dependent τ_1 is calculated as

$$\tau_1 = \frac{1}{2}\left(\tau_\infty - \frac{n_0}{G}\right) + \sqrt{\frac{n_0\tau_0}{G} + \frac{1}{4}\left(\tau_\infty - \frac{n_0}{G}\right)^2} \tag{9}$$

where τ_0 is the low-injection minority carrier lifetime, τ_∞ is the saturated SRH lifetime and can be approximated as twice the low-injection lifetime, n_0 is the majority carrier concentration at equilibrium, and G is the carrier generation rate. The Auger minority carrier lifetime is calculated as

$$\tau_a = \frac{1}{\sqrt[3]{G^2 r_{aug}}} \tag{10}$$

where r_{aug} is the Auger recombination coefficient [2], [11].

Dose rate photocurrents are modeled in circuit simulation as additional current sources placed across the device junctions, with current flowing from n-type to p-type. The Wunsch and Axness model, implemented as a piece-wise-linear current source, does not account for real-time changes in the device bias leading up to or during a transient radiation pulse. The Massengill SPICE2 implementation of the Wirth and Rogers equations, however, did calculate the bias-dependent depletion width at the start of the transient radiation pulse [8],[10]. Modern integrated circuit processes utilize lower bias conditions, therefore the use of independent current sources may force simulated voltages to non-physical values. Additionally with the myriad of

geometry options in modern processes, the number of models required for design coverage would be very time consuming to develop. This work develops modeling methodologies based upon the work of these authors with the addition of real-time bias calculation though the duration of the pulse and recovery and device geometry dependence, as well as the incorporation of dose rate induced conductivity modulation [6] and carrier lifetime modulation [2], [11]. The modeling methods developed in this work, and described in Chapter IV, have been shown to be portable across process and technology and demonstrate good agreement with test data.

Single-Event Effects

Unlike a dose rate pulse that generates excess carriers uniformly throughout the silicon of an integrated circuit, the interaction of a circuit and high energy ionizing particles is a random and localized occurrence, referred to as a single event. Single events lead to randomly appearing glitches in integrated circuits and electronic systems, ranging from transient current and voltage pulses to the corruption of data stored in memory elements. Wallmark and Marcus postulated the production of electrical errors as a result of ionizing particles in 1962 [13]. Errors in flip-flops due to ionizing particles interacting with circuits on communication satellites were discovered and reported by Binder in 1975 [14]. Errors in terrestrial systems due to naturally occurring alpha particles were observed by May and Woods in 1978 [15]. Many additional single-event related problems have been observed in the integrated circuit electronics of space and terrestrial systems, resulting in a growing field to study and to model the mechanisms and to mitigate the negative effects [5].

When an energetic ionizing particle penetrates a semiconducting material, it loses

energy though interactions with the semiconductor lattice structure, resulting in the production of free electron-hole pairs as the energy transferred when the interaction exceeds 3.6eV, the average energy required to generate an electron-hole pair. The rate of energy loss to electron-hole pair generation, referred to as linear energy transfer (LET), has units of energy per length, where the LET units are typically expressed as MeV-cm^2/mg. As the particle penetrates the material, it slows and the rate of energy deposition per unit length changes. The incremental length charge creation by the ion is calculated as

$$dQ\,[pC] = L(x)\left[\frac{pC}{\mu m}\right] * dX\,[\mu m] = \frac{LET(x)\left[\frac{MeV-cm^2}{mg}\right] * \rho\left[\frac{mg}{cm^3}\right] * 1.6 \times 10^{-5}}{G\,[eV]} \tag{11}$$

where the units of the variable is given in the brackets and dQ is the differential charge deposited in the incremental length, $L(x)$ is the linear charge deposition, dX is the incremental length, LET is the linear energy transfer of the particle at the incremental point in the path, ρ is the density of the target material, and G is the electron-hole pair generation energy (3.6eV for Si) [5]. Assuming a constant LET, the conversion from LET to deposited charge in silicon is calculated by

$$Q\left[\frac{pC}{\mu m}\right] = 1.035 \times 10^{-2} * LET\left[\frac{MeV - cm^2}{mg}\right] \tag{12}$$

The excess carriers, if generated near a reverse-biased P-N junction, can result in a transient current flowing from n-type to p-type silicon. Similar to dose rate transient currents, carriers generated in the depletion region of a reverse-biased junction are immediately separated and swept across the junction, the prompt current component. Carriers generated near the junction diffuse to the edge of the depletion region, resulting in a delayed diffusion current component, or they recombine and do not contribute to the transient current. In some cases, multiple devices in close proximity

to the track of the single event can collect the diffusing carriers. Charge sharing, also called multi-node charge collection, takes place when multiple reverse biased P-N junctions collect excess carriers generated by a single event [16]. Additionally, a single event occurring in an n-well, within a p-type substrate, can result in large transient currents that debias the n-well, which is typically tied to VDD in digital circuits. This well de-biasing may turn on lateral parasitic bipolar junction transistors (BJTs) in MOSFET devices and can influence the width of voltage transients in logic or information corruption in memory elements [17], [18], [19].

The transient currents resulting from a single event generate unwanted voltage transients capable of propagating though the circuit and competing with legitimate signals or perturb a memory element to change the state of the stored bit [5]. Models of single-event currents are injected in circuit simulation to assess the vulnerability of a candidate circuit to single-event effects. Existing models are discussed in the next section.

Single-Event-Enabled Modeling Landscape

Modeling single-event effects in circuit simulation has traditionally utilized the independent double exponential current source. Messenger developed an analytical expression, a difference of two exponentials, relating the temporal current waveform as a result of an ionized particle depositing charge in a reverse biased p-n junction [4]. Massengill detailed the single-event modeling methods of circuits in SPICE utilizing the double exponential current source in his 1993 NSREC Short Course [5]. Massengill provided the details of the time-current profile of the double exponential current source, as well as an equation for calculating the peak current given the characteristic

source time constants and the charge to be deposited by the pulse. The double exponential time-current profile follows the set of equations,

$$I(t) = \begin{cases} 0 & ; t < 0 \\ I_P \left(1 - e^{\frac{-t}{\tau_R}}\right) & ; t < t_D \\ I_P \left(1 - e^{\frac{-t_D}{\tau_R}}\right) e^{\frac{-(t-t_D)}{\tau_F}} & ; t > t_D \end{cases} \tag{13}$$

where I_P is the peak current at time t_D and τ_R and τ_F are the rising and falling characteristic time constants, respectively. The double exponential current source in most circuit simulators also allows the user to input a starting current, assumed to be 0 in (13), and a delay time before the pulse starts, also assumed to be 0 in (13). When modeling a single-event in a circuit, the user often knows the desired amount of charge to deposit and some of the characteristic time constants based on technology performance. Given that this information is known, the peak current required to achieve the desired charge deposition can be calculated with the equation,

$$I_P = \frac{Q_{Dep}}{\left[t_D + \tau_F - \tau_R - (\tau_F - \tau_R)\, e^{\frac{-t_D}{\tau_R}}\right]} \tag{14}$$

where Q_{Dep} is the desired deposited charge from the single-event strike and the other parameters follow those utilized in (13). Typical single-event models for bulk technologies have characteristic time constants of <10 ps and 100 ps for τ_R and τ_F, respectively. For advanced SOI technologies, those characteristic time constants are on the order of 1 ps and 10 to 20 ps for τ_R and τ_F, respectively. Massengill also provided a means of easily converting between an ions linear energy transfer (LET) and charge deposition per unit of path length through the device, as given in (12)

and repeated here as,

$$Q_{Dep}\left[\frac{pC}{\mu m}\right] = 1.035 \times 10^{-2} * LET\left[\frac{MeV - cm^2}{mg}\right] \tag{15}$$

where LET is the linear energy transfer for a heavy ion and Q_{Dep} is the charge deposited per unit of path length through the device [5].

Fulkerson has developed additional expressions for the temporal current waveform based on calculations of ambipolar diffusion, high or low injection conditions, and carrier current densities [20], [21]. The current profile of the source is still based on a double exponential function, similar to the form presented in [4]. The Fulkerson model is implemented with an independent double-exponential current source, additionally it also includes a reverse biased diode in parallel with the independent current source that will become forward biased when the junction voltage collapses [20], [21].

Single-event modeling in silicon-on-insulator (SOI) MOSFETs must also account for amplification of the deposited charge by the parasitic lateral BJT [22], [23]. Kerns and Massengill presented a single-event model for SOI MOSFETs, which contained an independent double-exponential current source and a BJT SPICE instance in parallel with the MOSFET, where the drain and collector, source and emitter, and body and base were connected. The model also contained a body-to-source resistance to model the source tie portion of the device and a resistor from drain to source to model MOSFET leakage. A schematic representation of the model is shown in Fig. 1, and a representation of an SOI MOSFET with a body-tied-to-source contact is shown in Fig. 2.

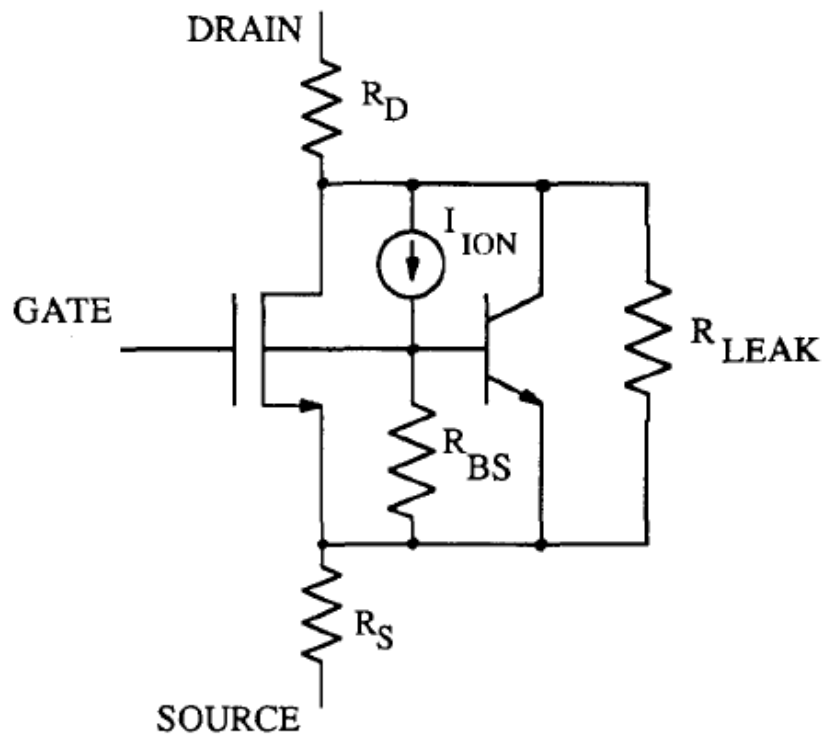

Figure 1: Schematic representation of the SOI single-event model presented by Kerns in [22].

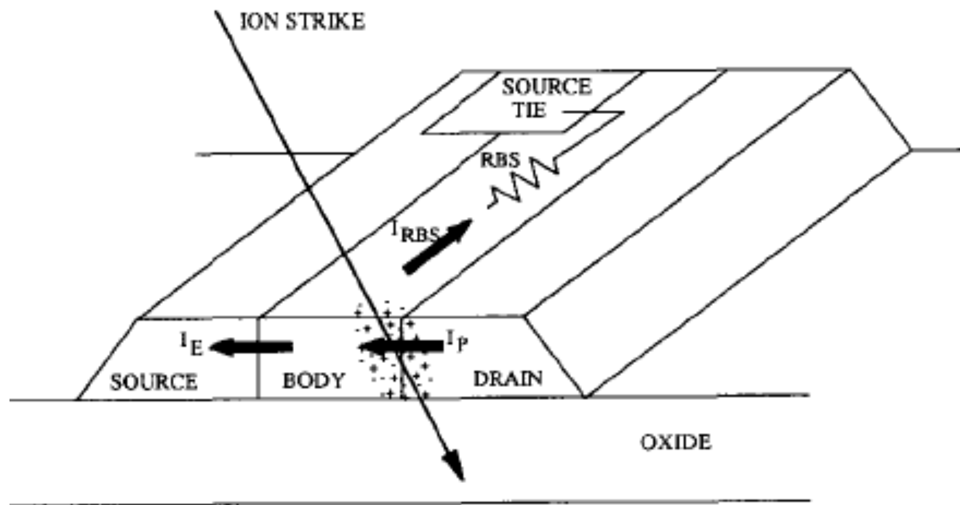

Figure 2: SOI NMOSFET with a body-tied-to-source contact and the RBS body resistance shown [23].

Massengill showed the relationship between the body resistance and the amplification of the deposited charge by simulating the critical charge required to upset an SRAM cell with respect to the distance between the strike and the body-tied-to-source region. With increased distance, thus increased RBS, the deposited charge required for upset was reduced, as the parasitic BJT amplified the deposited charge to a level equal to or exceeding the critical charge required to upset the SRAM cell [23]. The single-event model for SOI MOSFETs with parasitic BJT presented by Kerns and Massengill utilized full SPICE components for the BJT and resistors, wrapped together in a SPICE subcircuit. The model presented in [22] and [23] has largely been the basis for single-event modeling of SOI MOSFETs for two decades. Recent research has focused on the current generation source, a more physical representation of current deposition and collection, yet remaining an independent current source.

In [24] and [25], Fulkerson utilized 1-D carrier transport models to develop a single-event current generation method based on the physical models for carrier transport, specifically focused on diffusion. The model also incorporated some sensitivity to the location of the strike with respect to the center of the body and the drain edge. Schematically, Fulkerson's SEE model followed the Kerns and Massengill model in [22]. Alvarado, in [26], applied the Fulkerson current generation model [25], and the Kauppila bias-dependent model [27] to inject current into the base of a parasitic BJT in SPICE, and it is assumed that the Kerns and Massengill model topologies in [22] and [23] were followed. Kobayashi, in [28] and [29], observed a current plateau effect in the single-event current and modeled the width of the plateau as being proportional the to the charge storage time as the parasitic BJT comes out of saturation.

The models presented in [26] and [28] utilize individual SPICE components,

especially a SPICE BJT model, to represent the single-event current and amplification mechanism. The use of a SPICE BJT component increases the simulation overhead, when all MOSFET instances are pointing to a single-event model subcircuit, even if the current source of all but one MOSFET subcircuit are disabled. Additionally, the SPICE BJT model must be parameterized for each technology and device size, this is possible through the use of equations, but none of the papers detailed a parameterization methodology for the parasitic BJT. Additionally, the inclusion of a SPICE BJT model eliminates the drain/source symmetry of the SOI MOSFET models.

Observation of Bias Dependence in TCAD Simulations

Three-dimensional device simulations of deep sub-micron MOSFET technologies, utilizing mixed SPICE and TCAD, have been used to study the details of single-event effects in devices and small circuits [16], [17], [30], [31]. These simulations have revealed the importance of capturing the bias-dependent characteristics of the transient radiation-induced currents in order to accurately predict circuit upsets and errors. These simulations have also shown that the single-event currents in deep sub-micron technologies are not accurately modeled in circuit simulations using independent current sources, when the struck device is connected in a circuit [17], [30], [32].

However, when single-event effects are simulated for single devices in TCAD, with hard biased device terminals, the double exponential waveform is still a close approximation of the device response. Fig. 3 shows a comparison of the NMOSFET drain current from a single-device TCAD simulation and a double exponential

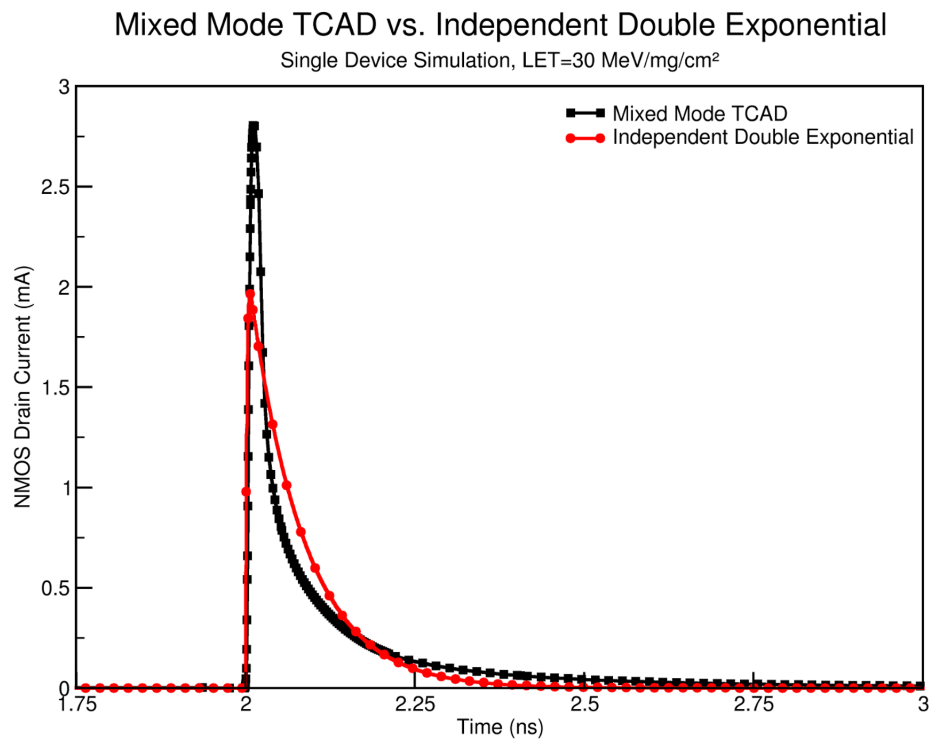

Figure 3: The double exponential current waveform is still a close approximation for the single-event current generated by TCAD with the terminals of the MOSFET connected directly to voltage sources in the simulation [27].

waveform that has approximately the same time constants, peak current, and total accumulated charge. Because the single-device response is still closely approximated by a double exponential waveform, it has been used as a base function in other modeling approaches [33], [27].

In SPICE circuit simulations, the independent double exponential current source does not accurately reproduce the results seen in mixed mode TCAD simulations. Fig. 4 shows a comparison of the NMOSFET drain current from an inverter simulated

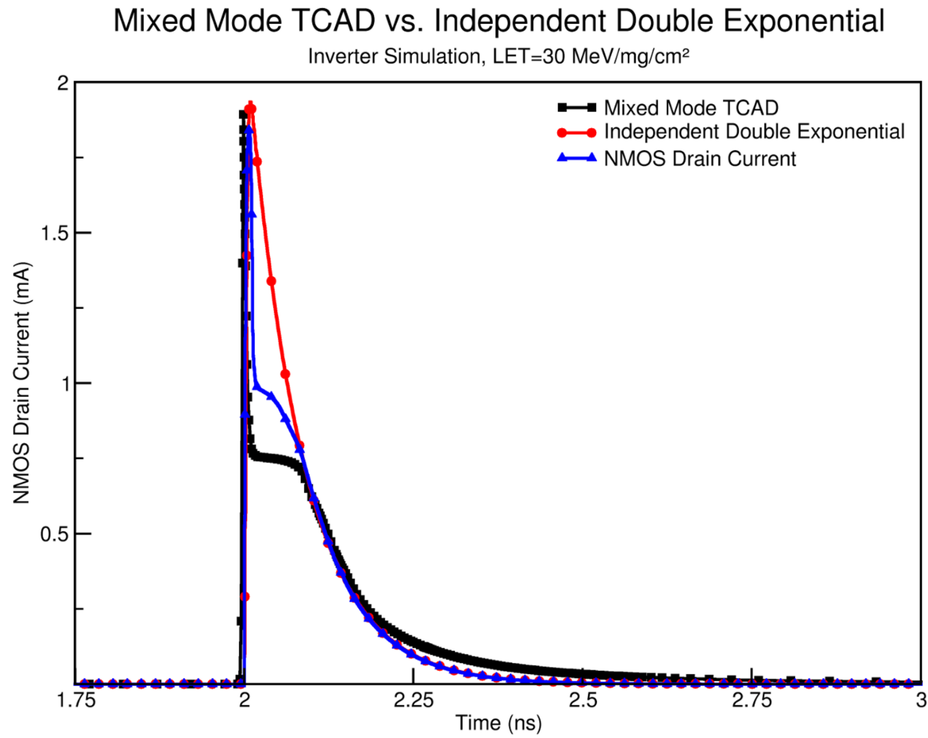

Figure 4: Comparison of NMOSFET drain current in TCAD mixed-mode and SPICE simulation of an inverter, where the SPICE simulation used an independent current source to model the single-event pulse. The double exponential parameters from Fig. 3 were used in this simulation, as shown by the Independent Double Exponential plot. It can be observed that the integrated charge is different between the TCAD simulation and the NMOSFET drain current resulting from the use of an independent double exponential source [27].

in TCAD mixed mode and SPICE, where an independent double exponential current source was used to model the single-event current in SPICE. The double-exponential

current source was connected to the NMOSFET drain node and to the NMOSFET body node. These connections are external to the intrinsic SPICE MOSFET drain and body resistances. Additionally, the NMOSFET body is often tied directly to ground or a fixed VSS voltage in SPICE simulations, thus the current source is pushing current into an infinite current sink. The NMOSFET drain voltage is a function of the Ohms Law relationship of the PMOSFET load impedance and the current being pulled through that impedance by the independent current source. As a result, the independent current source will force the NMOSFET drain below ground or the VSS voltage rail until the NMOSFET body-drain diode turns on and the resulting diode current compensates the independent current source. Mixed mode TCAD simulations do not demonstrate this behavior because the single event current is a result of charge that is generated within the TCAD device and intrinsic impedances. Fig. 5 shows the inverter output voltage (NMOSFET drain voltage) comparison for TCAD and SPICE simulations utilizing ideal independent double exponential current sources.

Conclusions

This work advances the historical modeling methods and incorporates effects based on bias dependencies, scalability of device layout, and model parameterization liked to physical processes. Recent TCAD simulation results have demonstrated that the transient shape of the bias-dependent radiation-induced current pulse is critical to accurate circuit simulation based vulnerability predictions. The development of bias-dependent transient radiation induced current modeling methods are discussed in Chapter III. Chapter IV details the development and implementation of layout-aware, bias-dependent, dose-rate models for dielectrically isolated bipolar junction transistor

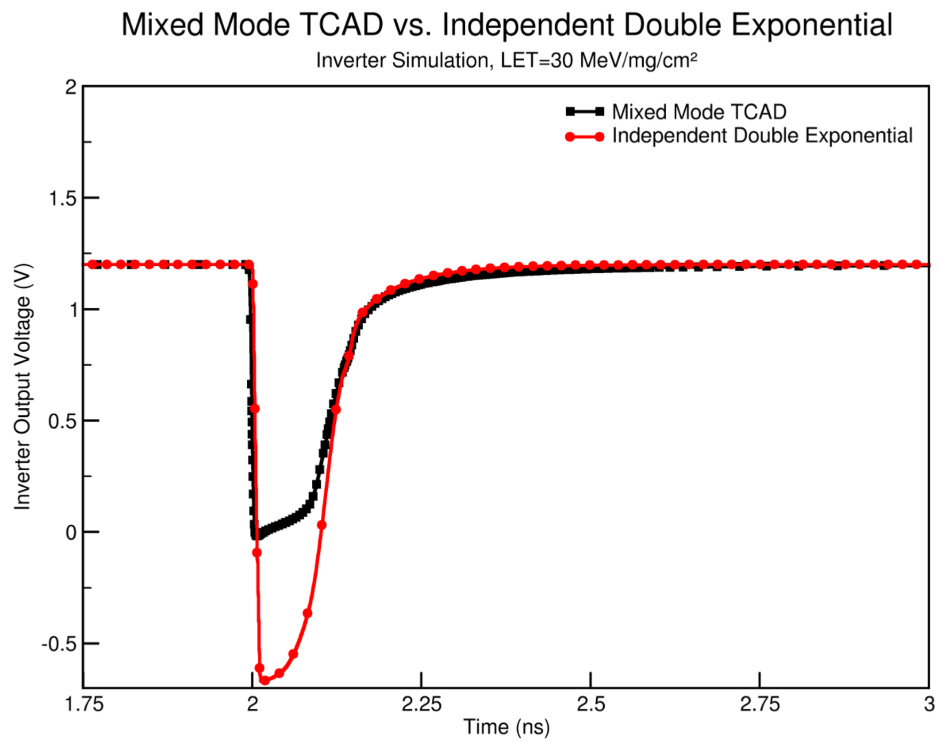

Figure 5: Comparison of TCAD and SPICE simulated inverter output voltages (NMOSFET drain voltages) shows the SPICE output voltage is forced well below the negative rail, but the TCAD simulated output voltage does not demonstrate this behavior [27].

(BJT) and silicon-on-insulator (SOI) complimentary metal oxide semiconductor (CMOS) technologies. Layout-aware, bias-dependent single-event modeling methods are discussed for bulk CMOS, bulk silicon germanium (SiGe) heterojunction bipolar transistor (HBT), and SOI CMOS technologies in Chapter V. The modeling methods to account for device layout in dose rate and single-event models has led to the development of novel layout-aware analysis capabilities, discussed in Chapter VI, which utilize layout information and circuit simulation to perform and automated characterization of the radiation response of a design. As technologies continue to scale to smaller dimensions, increased density, and lower supply voltages, circuits are anticipated to become increasingly sensitive to transient radiation-induced faults. Technology scaling leads to higher chip development and manufacturing costs, increasing pressure for first or early pass success in circuit functionality and reliability in a radiation environment. The methods developed in this work will provide integrated circuit designers with capabilities to assess circuit vulnerabilities and susceptibility to transient radiation-induced effects.

CHAPTER III

BIAS DEPENDENCE OF RADIATION-INDUCED CURRENTS

As discussed in Chapter II, TCAD simulations of transient radiation effects on deep sub-micron technologies showed an elongated current plateau [17], [30], [16], [31]. The plateau effect has been observed in mixed-mode TCAD simulations of single-event transients in inverter chains, where the PMOSFET drive current limits of the plateau amplitude [17], [30], [16], [31], [32]. DasGupta showed that the width of the plateau is directly proportional to the width of the propagating SET voltage pulse [32]. This plateau is a bias-dependent effect that depends on the surrounding circuitry's ability to source or sink the radiation induced current in the reverse biased junctions of the device. The compact modeling methodology to account for this bias-dependent current plateau has been developed and incorporated into the layout-aware compact modeling methods presented in Chapters IV and V.

Historically, the independent current sources have been parameterized to match the characteristics of simulated or measured transient pulses, as implemented using the equations presented by Wirth for dose rate in [1] or utilizing a double-exponential current for single-event modeling as in [4] and [5]. However, in advanced integrated circuit technologies, the independent sources could not be parameterized to match the plateau effect, as a function of arbitrary junction bias and surrounding circuit drive. Fig. 4, shown again here as Fig. 6, and Fig. 7 demonstrate the plateau effect observed in TCAD based single-event simulations of a sub-100nm CMOS inverter [27]. Fig. 7 shows the NMOSFET drain currents from a mixed mode TCAD simulation

for multiple linear energy transfer (LET) values [31], [34]. For small LET values, the drain current is still well approximated by a double exponential waveform. However, with increasing LET, the drain current is clamped at the PMOSFET drive current. The current plateau is set by the drive strength of the pull-up device; in the case of this inverter simulation, the pull-up current is set by the PMOSFET device drive current.

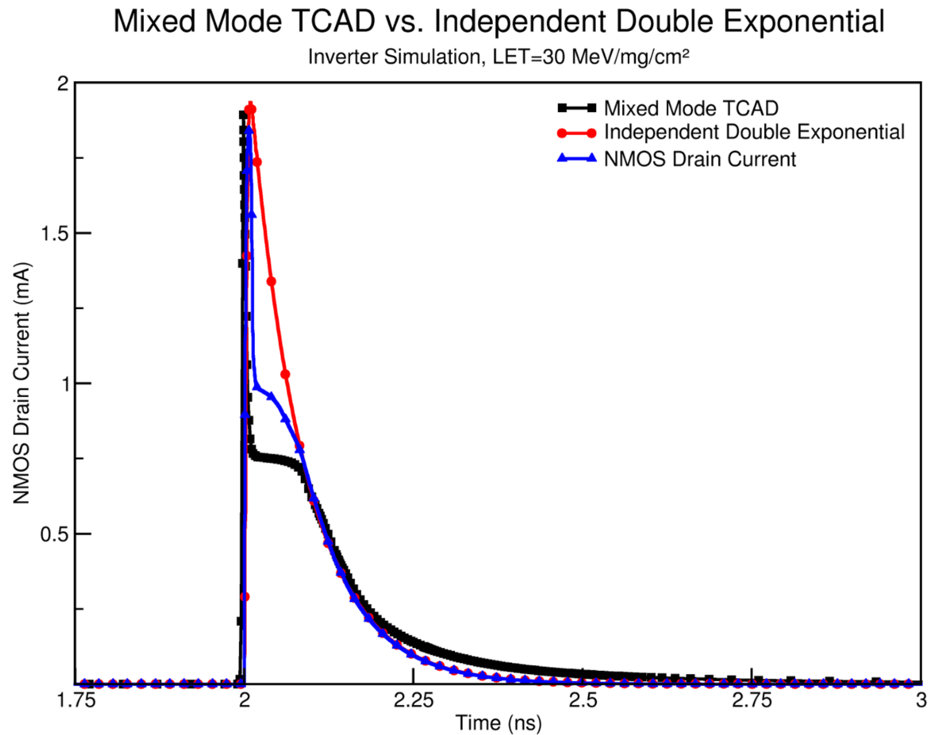

Figure 6: Comparison of 3-D TCAD observed current plateau and the resulting NMOSFET single-event current when an independent double exponential source is used as the model [27].

There have been attempts to model the ”plateau” effect for SPICE circuit simulation, ranging from piece-wise linear current sources to models that utilize many additional SPICE components to calculate the appropriate current response [35], [36], [33]. Piece-wise linear (PWL) based models have been derived from mixed mode TCAD simulations or from measured test data [35], [36]. While the PWL model

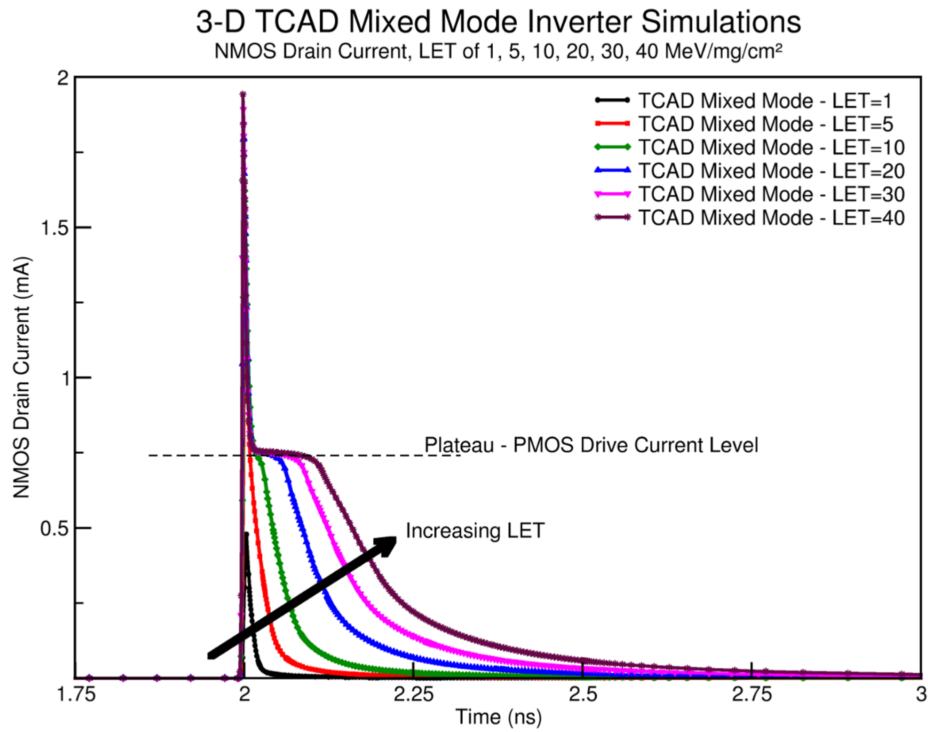

Figure 7: 3-D TCAD mixed mode simulations results showing single-event induced NMOSFET drain current for various LET values. Low LET currents can be approximated by a double exponential waveform. As LET increases, the single-event induced drain current is clamped at a level equal to the PMOSFET drive current [27].

accurately captures the characteristics of the single event current, it is inherently not scalable to other bias conditions, LET values, or device sizes. This implies that TCAD simulation or test data would need to be obtained for each desired SPICE simulation case. Additionally, as Turowski and Mavis have both observed, SPICE independent current sources can force unrealistic voltages at circuit nodes and the currents do not change with bias, as mixed-mode TCAD simulations have shown [30], [33].

Mavis has presented a bias-dependent model, the equivalent circuit model (ECM) that captures the plateau effect [33]. The ECM is implemented using a series of dependent current and voltage sources. These dependent sources are used to calculate the response of the single event current to the change in device bias. Because this model uses standard SPICE components, it has the potential to be portable across SPICE simulators. The ECM, however, uses many dependent SPICE components that must each be characterized, programmed, and calibrated for each technology and main current source function, referred to as a kernel function in [33]. Additionally, the presented implementation of the ECM is a subcircuit attached to a circuit node rather than integrated with a MOSFET model and internal to the intrinsic drain/source and body resistors.

Bias-Dependent Modeling Methodology

The bias-dependent modeling methodologies developed in this work still utilize independent current sources to generate the primary charge deposition and current waveform shape, however the charge from the independent current source is deposited onto a holding capacitor. For the purpose of visualizing and explaining the function of

each part of the model, Fig. 8 shows a schematic representation of the bias dependent methodology using standard SPICE components.

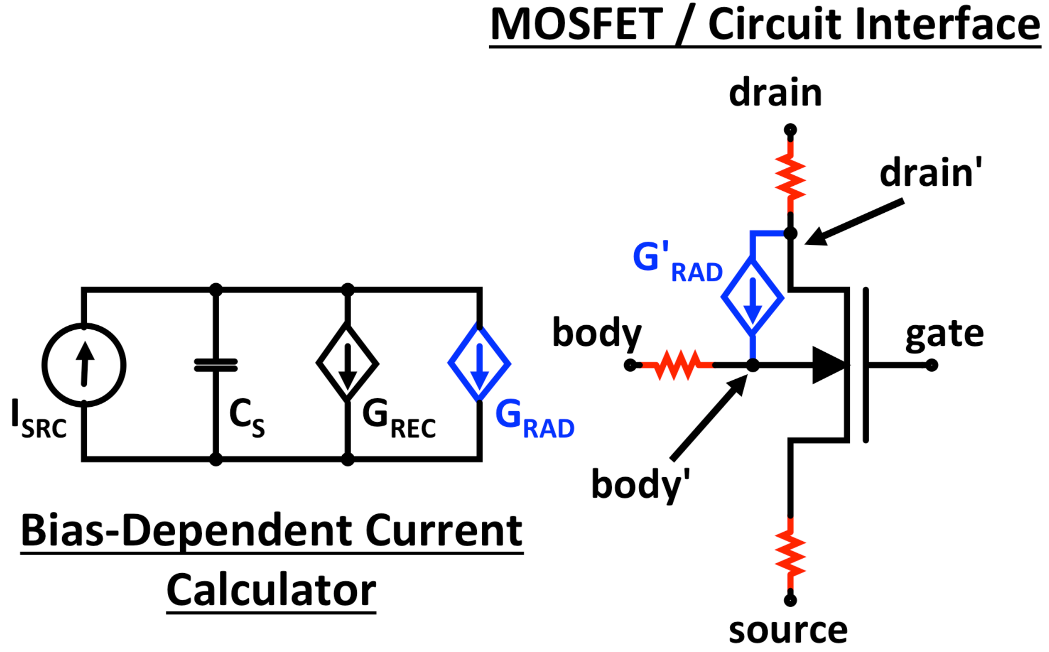

Figure 8: The schematic representation of the bias-dependent transient radiation induced current model across a P-N junction, represented here as the body-drain junction of an NMOSFET.

The calculation portion of the model consists of four branches, and the current applied to the transistor is a mirror of one of the branches. The model, presented in schematic form in Fig. 8, has been implemented using the Verilog-AMS behavioral modeling language as a system of equations:

$$I_{SRC}(t) + \frac{C_S dV(C_S)}{dt} = G_{REC}(t) + G_{RAD}(t) \tag{16}$$

$$G_{REC}(t) = f\left(V(C_S), C_S, RecombParameter\right) \tag{17}$$

$$G_{RAD}(t) = f\left(V(C_S), C_S\right) \times Fermi\left(V(P, N)\right) \tag{18}$$

$$G'_{RAD}(t) = G_{RAD}(t) \times \textbf{Gain} \tag{19}$$

that solve the differential equation for the four branches in the calculation portion and multiply the G_{RAD} output value by a gain factor if applicable, the gain is 1.0 in this work. In (18), $V(P, N)$ is the voltage between the internal junction nodes from p-type to n-type and are equivalent to the $body'$ and $drain'$ nodes in Fig. 8. The Fermi-style function in (18) clamps the current through G_{RAD} when the reverse bias across the junction collapses. The Fermi function is calculated as

$$\frac{1}{1 + e^{\frac{V(P,N)}{F}}} \tag{20}$$

where $V(P, N)$ is the bias across the junction from p-type to n-type and F is the parameter that determines the slope and range of the current reduction. The F parameter determines the junction bias range, +/-FV around 0V, over which the G_{RAD} current in (18) drops from approximately 75% to 25% of the non-current limited calculated value. As shown in Table 16, the F parameter is often set in the range of 0.01 to 0.1.

The independent current source, I_{SRC}, represents the basic time-current profile of the transient radiation-induced current. The functions directing the behavior of the radiation-induced current source are developed in Chapters IV and V, however an independent double-exponential current source will be utilized as the I_{SRC} in the discussion of the bias-dependent modeling methods. The as a double-exponential current source is easily implemented and has good convergence in SPICE simulations, while still representing the basic single-event current waveform for single MOSFET devices, as shown in Fig. 3. The capacitor, C_S, is used to ensure charge conservation.

Its value is not critical (outside of numerical considerations) and does not represent a physical capacitance. The voltage across the capacitor is proportional to the charge that has not been dissipated by the two dependent source branches.

The G_{RAD} and G'_{RAD} dependent current sources represent the radiation-induced current at the semiconductor junction and are internal to the intrinsic impedances of the junction, e.g., diffusion resistances or contact resistances. The current through G_{RAD} is a calculated value that is proportional to the voltage across C_S and is a function of the voltage across the internal transistor junction. In the P-N junction represented by an NMOSFET in Fig. 8, the internal drain side of the junction is denoted as $drain'$, and the internal body is likewise denoted as $body'$. If the $drain'$-$body'$ junction is reverse biased, the calculated G_{RAD} current will follow the current generated by I_{SRC}. As the $drain'$-$body'$ junction voltage collapses and approaches 0V, due to the current limiting of a load device, the current through G_{RAD} is also reduced and will plateau at the limited supply current level, as determined by the surrounding circuitry. G'_{RAD} is a mirror of G_{RAD} and flows directly into the transistor. G_{RAD} is not directly connected to the transistor to isolate the calculation portion of the model from any undesired external influences, such as those that may charge C_S and cause errant charge collection.

The G_{REC} dependent current source accounts for recombination currents in the device. The magnitude of the G_{REC} current is typically small for cases where there is little bias change. However, when the bias collapses and the G_{RAD} current is limited by the circuit, the G_{REC} current allows the voltage across C_S to decrease, shortening the length of the plateau due to recombination of excess charge in the semiconductor. The magnitude of G_{REC} is dependent on the lifetime of the excess

carriers in the device. The model parameter utilized to set the strength of the G_{REC} source is the $RecombParameter$ shown in (17). Fig. 9 demonstrates the functionality of the $RecombParameter$ in the G_{REC} source and shows its impact on the overall pulse shape.

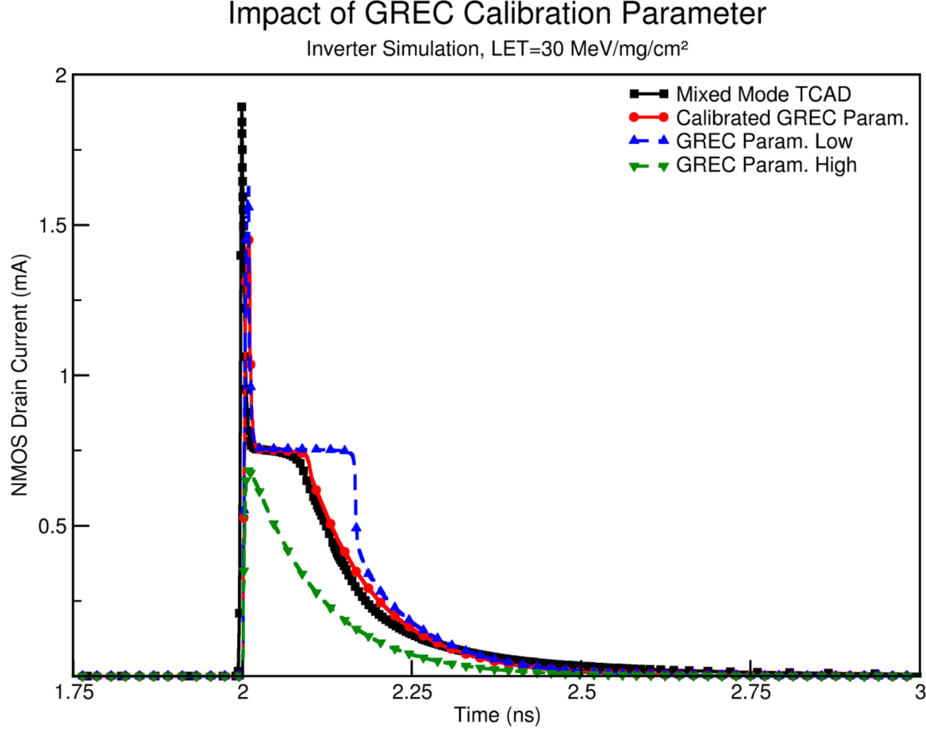

Figure 9: The $RecombParameter$ in the G_{REC} component controls the width of the plateau for a technology. As the parameter value is decreased, the plateau widens. If the parameter is too large, the ability to reproduce the plateau will be eliminated. Calibration of the G_{REC} component can be achieved using TCAD or test data that shows a plateau response, however the $RecombParameter$ is approximately the reciprocal of the minority carrier lifetime during the event.[27]

The $RecombParameter$ is approximately the reciprocal of the minority carrier lifetime during the event, which accounts for the excess carriers generated in the event and is the combined Shockley-Reed-Hall (SRH) and Auger lifetimes calculated as

$$RecombParameter \approx \frac{1}{\tau_T} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_A} \tag{21}$$

where τ_T is the combined SRH and Auger lifetime, and τ_{SRH} and τ_A are the SRH and Auger lifetimes, respectively [3], [11]. The Fjeldly model in (8)-(10) can be used to calculate the total minority carrier lifetime for dose rate events. In the case of single-event minority carrier lifetime for the event will be dominated by the shortest lifetime, which will be in the region of the strike, because lifetimes combine as the reciprocal of the sum of the reciprocals. If the magnitude, time, and volume of the charge deposition can be calculated or assumed, a generation rate can be calculated in terms of $\frac{e-hpairs}{cm^3-s}$, and the Fjeldly model can be easily utilized. Additionally, the combined lifetime can be calculated from the concentration of excess e-h pairs generated in the ion track region, which can be approximated as

$$n' = p' = \frac{Q_{Dep}[pC/\mu m] * L_{Col}[\mu m] * 1 \times 10^{-12}[C/pC]}{q * Vol_{Dep}[cm^3]} \tag{22}$$

where n' and p' are the generated excess electron and hole concentrations in cm^{-3} as a result of the single event, Q_{Dep} is the deposited charge calculated in (15), L_{Col} is the length of the collection volume, q is the electron charge, and Vol_{Dep} is the volume of the charge deposition, units are given in square brackets. In a p-type doped silicon $n_0 = n_i^2/N_a$ with $p_0 = N_a$ and $p_0 = n_i^2/N_d$ with $n_0 = N_d$ for n-type doped silicon [3]. The total electron and hole concentrations are $n = n_0 + n'$ and $p = p_0 + p'$, respectively. The expressions for SRH and Auger recombination are

$$U_{SRH} = \frac{(pn - n_i^2)}{\left[p + n + 2n_i cosh\left(\frac{E_t - E_i}{kT}\right)\right]\tau_0} \tag{23}$$

$$U_A = \Gamma_n n\left(pn - n_i^2\right) + \Gamma_p p\left(pn - n_i^2\right) \tag{24}$$

where n and p are the total electron and hole concentrations, respectively, n_i is the intrinsic carrier concentration of Si, and Γ_n and Γ_p are the Auger recombination

coefficients, typically $1-2\times10^{-31}cm^6s^{-1}$, for electrons and holes, respectively. U_{SRH} is maximized when E_t=E_i, meaning recombination centers are near the middle of the gap, and therefore the third term in the denominator will be much less than the sum of the total electron and hole densities [3]. τ_0 in (23) is calculated as a function of the average doping in the region using the SRH Concentration Dependent Lifetime Model [37]. The SRH and Auger lifetimes for minority electrons then are calculated as

$$\tau_{SRH} = \frac{n'}{U_{SRH}} \tag{25}$$

$$\tau_A = \frac{n'}{U_A} \tag{26}$$

where τ_{SRH} is the SRH lifetime, τ_A is the Auger lifetime, and n' is the excess electron concentration calculated in (22). The calculation of the hole minority lifetime in n-type silicon would substitute p' for n' in (25) and (26).

Example Application of Bias-Dependent Methods

The bias-dependent transient radiation-induced current modeling methods are demonstrated here as a single-event model integrated with the BSIM4 transistor model [38]. A bias-dependent single-event source was connected to the internal drain and body nodes of an NMOSFET, following the MOSFET schematic in Fig. 8. The integrated BSIM4 and bias-dependent model has been compared to 3-D mixed-mode TCAD simulations of an inverter in a bulk 90nm CMOS process [31], [34]. This inverter has a PMOSFET to NMOSFET width ratio of 2.5/1. The bias-dependent model shows excellent agreement with the mixed-mode TCAD results. Additionally, the bias-dependent model does not force the output voltage of the inverter below the

rail as the independent current source was shown to do in Fig. 5. Figs. 10 and 11 show the NMOSFET drain current and inverter output voltage resulting from 3-D mixed mode TCAD and simulations using the bias dependent single-event model for various amounts of deposited charge.

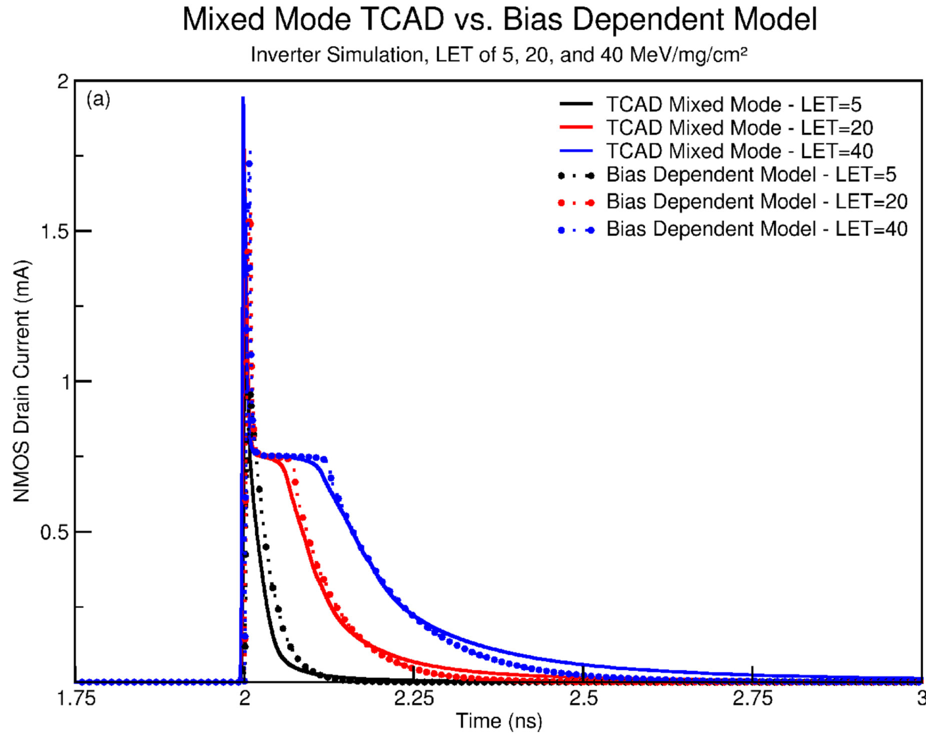

Figure 10: The drain current of the struck NMOSFET device, TCAD in solid line and bias-dependent single-event model in the dotted line, over multiple LETs. The plateau effect is observed in the TCAD simulation and reproduced in the model.

Conclusions

Bias-dependent transient radiation-induced current modeling methodologies have been developed that are capable of capturing the bias-dependent effects observed in recently published 3-D mixed-mode TCAD and test data. Specifically, the methodology is capable of reproducing the current limited plateau effect and includes additional capability to factor in effects such as recombination and if needed, a

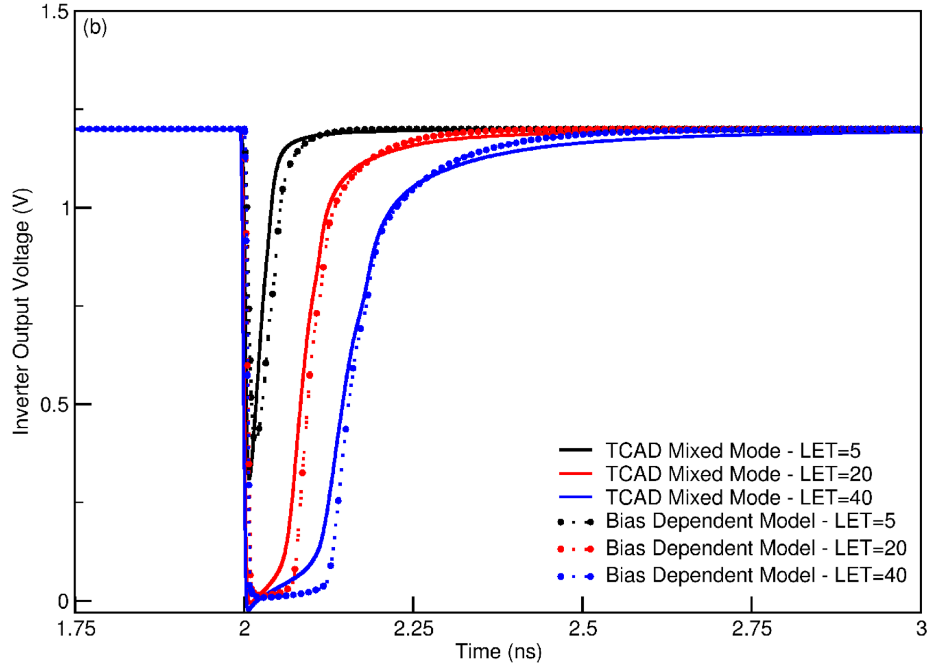

Figure 11: The inverter output voltage as a result of a simulated strike to the off NMOSFET device, TCAD in the solid line and the bias-dependent model in the dotted line. The output pulse widths of the two simulations agree well over LET.

constant gain between the current calculation unit and the current source connected to the device terminals. The modeling methodology has been implemented in a simple, efficient, and portable manner with a limited number of calibration parameters. The methodology was demonstrated using a bias-dependent single-event model implementation integrated with a 90nm bulk NMOSFET model using the BSIM4 MOSFET model. Simulations using the integrated BSIM4 transistor and bias-dependent single-event model have shown good agreement with 3-D mixed-mode TCAD simulations. Simulating the bias dependencies in the transient radiation response of devices are critical as technologies continue to scale.

CHAPTER IV

LAYOUT-AWARE DOSE RATE COMPACT MODELING

Previous work has been performed to develop detailed mathematical models of the generation of electron-hole pairs and the resulting transient currents. The historically developed dose rate photocurrent models are primarily 1-D and limited multi-dimensional focused on large devices, discrete components or early bipolar junction transistor integrated circuit technologies [1], [7], [2], [11]. Current integrated circuit technologies require models that can account for complex 3-D implementation with scalability over device geometry, bias voltage, and dose rate.

Dose rate compact modeling methodologies have been developed based on physical models for electron-hole pair generation, dose rate dependent carrier lifetimes, carrier diffusion, and conductivity modulation, as discussed in Chapter II [1], [7], [8], [11], [6]. This work extends the previous work and develops the methodologies to model the complex 3-dimensional integrated circuit features with scalability over device bias condition, device layout geometries, and environment level. The dose rate photocurrents are modeled for each junction in the integrated circuit device, with each junction model reflecting the layout based geometry features and scaling of the device junction. The photocurrent sources are attached to the electrical SPICE model within a sub-circuit wrapper, which enables seamless integration with manufacturer process design kits (PDK) and commercial integrated circuit design and analysis tools. The intrinsic series resistances at the electrical model terminals are externalized in the sub-circuit wrapper and are implemented following the SPICE equations for the

type of device being modeled [39]. The photocurrent source terminals are connected to the electrical model internal to the series resistances, with current flowing from the n-type silicon in a device toward the p-type silicon.

The dose rate enabled models have been compared to test data for circuits, ranging from basic parallel device arrays to more complex analog/mixed signal circuit implementations, in bipolar junction transistor (BJT) and silicon-on-insulator (SOI) complementary metal-oxide semiconductor (CMOS) technologies. A high level of agreement between the models and test data has been achieved when comparing the peak photocurrent, transient pulse shape, and circuit behavior as a result of the dose rate pulse. The fundamental properties and implementation of the photocurrent model and comparisons of the model performance to test data are presented in this chapter. A discussion of the device arrays and operational amplifiers used in calibration and validation of model behavior is included in Appendix A.

The dose rate enabled models are calibrated to test data obtained from arrays of parallel devices irradiated in a linear accelerator. The calibration process primarily involves the tuning of two internal model variables to match the pulse height and shape from the test data. The model functionality and accuracy over bias conditions and geometry is demonstrated by comparing circuit simulations to circuit test data. The model user does not need to adjust internal parameters of the model for any bias or geometrical scaling, but only needs to adjust the pulse parameters of dose rate level, pulse width, and pulse start time. The use of calibrated dose rate models during the circuit design phase gives the designer the ability to observe the dose rate response of a circuit prior to release for fabrication. This capability provides a means of catching dose rate induced upsets in the circuit design phase and correcting the circuit issues

that lead to upset. Additionally the models are a forensic analysis tool for diagnosing anomalies observed in testing, post fabrication. Designers can also use the models to identify circuit paths of high dose rate current and use the information as a tool to guide the selection of metal widths and power bus sizes to prevent rail-span collapse during layout [6].

Modeled Technologies

The dose rate photocurrent generation models, implemented in Verilog-AMS, have been integrated with process design kits for dielectrically isolated BJT and SOI CMOS integrated circuit technologies [40]. The fundamental structure and mathematical calculations within the model are portable across technologies. The carrier collection volume calculations and model integration, however, are technology specific.

The BJT technology devices considered here are constructed in individual dielectrically isolated tubs, isolating the devices from each other and the substrate. The tubs form the collector of the BJT, with the base and emitter within the tub, creating a vertical BJT device. The minimum drawn dimension in the BJT processes is on the order of 2-3μm. The BJT technology is rated to support collector-base voltages up to 30 V.

The SOI CMOS process is partially depleted technology that utilizes body-tied devices. The body can be independently contacted or tied to the source of the MOSFET. The devices are constructed on a mesa structure with isolation from other devices and the substrate via silicon dioxide. The SOI CMOS technology supports gate-to-source and drain-to-source voltages up to 5 V.

Dose Rate Enabled Compact Model

The dose rate modeling methodologies developed in this work are based on physical models for electron-hole pair generation, dose rate dependent carrier lifetimes, carrier diffusion, and conductivity modulation as presented in [1], [7], [11], [6]. The Verilog-AMS behavioral modeling language provides the capability to implement the physically based models in 3-dimensions and calculate the bias-dependent volumes of the carrier collection [40]. The photocurrents and collection volumes are solved in a closed loop system at each time step of the simulation, incorporating multiple dose rate, doping level, and bias-dependent effects as well as 3-dimensional boundary conditions.

In the BJT technologies, the collector, base, and emitter resistances, which can be tens to hundreds of ohms, were pulled out of the SPICE electrical model and placed in the sub-circuit wrapper. The Mextram BJT model was utilized in this work, and the constant RCC, RBC, and RE resistances were externalized, while the RCV and RBV resistances were contained within the SPICE model [41], [42], [43]. Fig. 12 shows a schematic representation of the Mextram BJT model, where the RCC, RBC, and RE resistances are noted and RCV and RBV are noted as $I_{C1}I_{C2}$ and $I_{B1}I_{B2}$, respectively. The constant resistances were implemented to maintain temperature dependence and dependence on other parameters in the Mextram model [39], [43]. In other types of BJT models, intrinsic resistance models are not static values, but vary with bias and current, and the externalized resistors in these model types must be implemented using the SPICE equations for resistance value calculations [39]. The photocurrent sources in the BJT models were placed inside of the resistances for a more physical placement of the photocurrent sources in the SPICE model.

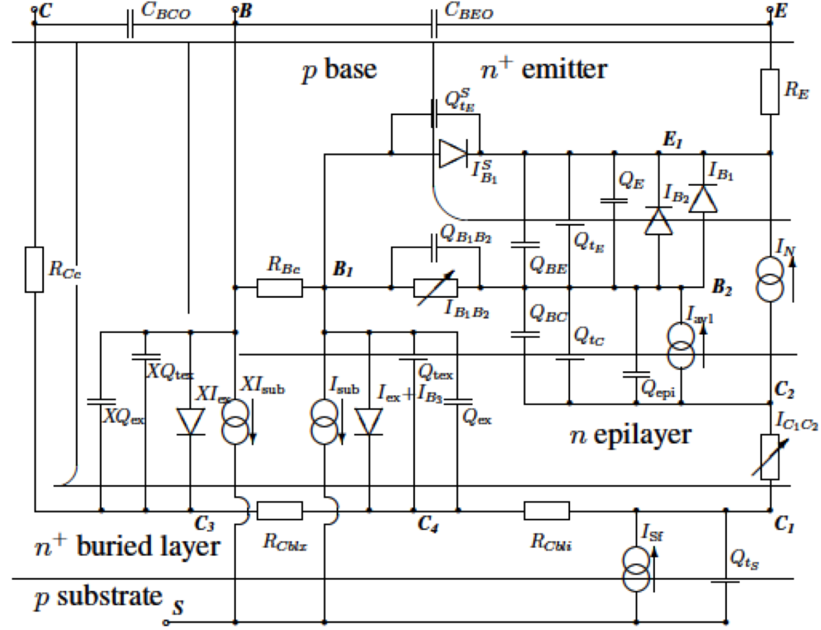

Figure 12: Schematic representation of the Mextram compact model with RCC, RBC, and RE noted by name in the schematic. RCV and RBV are noted as $I_{C1}I_{C2}$ and $I_{B1}I_{B2}$, respectively [41], [42], [43].

To account for conductivity modulation in the collector and base resistances, the emitter doping is sufficiently high that modulation can be ignored in RE, a Verilog-AMS variable resistor implementation is placed in parallel with the externalized resistance. During the time before the pulse occurs, the parallel resistance is very large, e.g. $1 \times 10^{12}\Omega$, and during the pulse the parallel resistor is reduced to provide the correct reduction in resistance for the calculated level of conductivity modulation. Massengill included conductivity modulation in [6], however the implementation was based on SRH lifetime only, as the Fjeldly model was introduced over a decade later [11]. As a result, Massengill's model required separate calculations for low and high injection conditions, with the potential for a discontinuous modulation function over dose rate [6]. This work incorporates the Fjeldly lifetime model into the calculation of the conductivity modulation, resulting in continuity of the modulation function over

dose rate. The implementation of the conductivity modulation within the compact model is presented in the next section.

A schematic representation of the BJT model with the collector, base, and emitter resistances external to the SPICE model, the collector and base modulation resistances in parallel with RC and RB, and the photocurrent sources inside of the resistance models is shown in Fig. 13. Likewise, the photocurrent sources in the

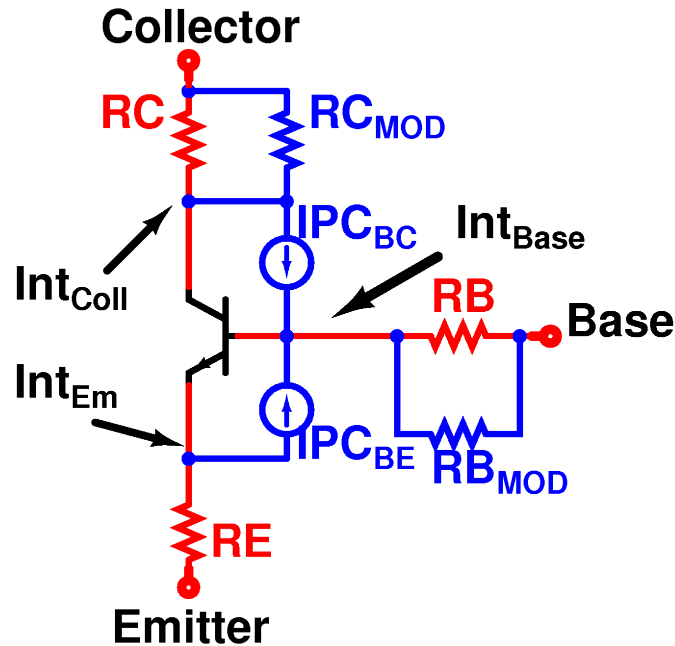

Figure 13: Schematic representation of the NPN BJT model with the intrinsic collector, base, and emitter resistances removed from the model and implemented separately as RC, RB, and RE. Conductivity modulation of RB and RC is implemented by placing the RB_{MOD} and RC_{MOD} resistors in parallel with the RB and RC resistors. Photocurrent sources are then placed across the internal junction nodes.

partially depleted SOI CMOS technology, with body contacts, were also placed inside the intrinsic resistance models, with the drain and source resistances pulled out of the electrical model and placed in a sub-circuit wrapper. The photocurrent source was placed inside the intrinsic body resistance by using the internal body terminal in the BSIMSOI SPICE model [44].

The use of dielectrically isolated technologies in this work allowed for simplified assumptions within model. The dielectric isolation provides the boundary condition for the photocurrent collection, in the case of long diffusion lengths, where the Wirth assumption of a limiting boundary of one diffusion length is used, when the diffusion length is less than the distance to the dielectric isolation boundary. Additionally, this boundary condition meant that there was no need to determine how volumes between two adjacent devices, within the region of generated electron-hole pair collection, would split the collected carriers between the two devices. The concepts developed in this modeling method extend to bulk technologies, where the boundary condition will be set by diffusion length and device proximity. When two bulk devices are separated by less than two diffusion lengths, it can be assumed that they will evenly split the collection volume between them [1].

While, the modeled technologies contained a single device per active tub, for the BJT technologies, in the SOI CMOS technology, multiple finger devices, or multiple connected gates over a single active area with alternating drain and source between the gates, were accounted for within the photocurrent modeling because the models were scalable with geometric possibilities and unique layout patterns according to the process design kit (PDK). The dose rate model for the multiple fingered devices mapped a current generation source to each of the junctions in the fingered device. For example, a two-fingered device may have two source regions, a single drain region, and two body regions. The model generates photocurrents for the two source/body junctions and the two drain/body junctions, with the capacity to account for the collection volume represented by each of the sources.

Model Implementation

The dose rate model utilizes some basic information about the fabricated devices in the technologies including the drawn layout regions, vertical (cross-sectional) geometrical information and average doping levels in the various device regions. During circuit operation and transient radiation pulse, the depletion width varies with the bias across the junction, where the photocurrents flowing through the device perturb that bias. To account for this effect, the model calculates the depletion width at each junction in the device at every simulation time step during the dose rate pulse; thus when the depletion region collapses current generation at that junction is limited by the surrounding circuitry attempting to restore the bias. In the Verilog-AMS model, the depletion region width is calculated for each side of the junction using the function in Table 1, where $DepW$ is the calculated depletion width, $NThis$ is the carrier concentration on the side of the junction being calculated, $NOther$ is the carrier concentration on the other side of the junction, VPN is the boas across the junction referenced from p-type to n-type, VBI is the calculated built in potential, Eps is the permittivity of silicon, $ni2$ is the approximate intrinsic concentration of silicon squared at 300K, and q is the electron charge [3].

Utilizing the doping level information, the dose rate dependent carrier lifetimes and diffusion lengths for carriers in a specific region are calculated [3], [11]. The nominal carrier lifetime in a device region, and thus nominal diffusion length, is calculated as a function of the average doping in the region using the SRH Concentration Dependent Lifetime Model [37]. The carrier lifetimes are modulated as a function of the dose rate level following the methods outlined in [2] and [11]. Additionally, the carrier lifetimes are calculated to account for carrier motion through

Table 1: Verilog-AMS function to calculate the depletion width on one side of the junction

```
analog function real DepW;
  input NThis, NOther, VPN;
  real NThis, NOther, VPN;
  real VBI, Eps, ni2, q, VJ, y;
  begin
    ni2=2.1E20; //Approx intrinsic concentration squared at 300K
    q=1.602E-19;
    Eps=11.7*8.854E-14;
    VBI=$vt*ln((NThis*NOther)/ni2);
    VJ=VBI-VPN;
    if(VJ>0) y=sqrt(2*Eps*VJ/(q*NThis));
    else y=0.0;
    DepW=y;
  end
endfunction
```

a high doping to low doping region of like type silicon [7]. Table 2 shows the Verilog-AMS calculation of nominal carrier lifetime and diffusion length, as well as the modified lifetimes according to Long et al. and Fjeldly [7], [11], where $DRtauSRH$ and $DRtauAUG$ are the Fjeldly lifetime equations; tn and $tinf$ are τ_0 and τ_∞ from (9), respectively; $p0$ is the doping concentration; Gn is the dose rate carrier generation rate; $raug$ is the Auger recombination coefficient; $t0$, ta, and tBL are the initial and doping concentration dependent lifetimes; tau and $tauBL$ are the dose rate dependent lifetimes for the region and highly doped buried layer of like doping; *Diff* and *DiffBL* are the diffusion coefficients; $\$vt$ is the Verilog-AMS temperature dependent kT/q; LD and $LDBL$ are the diffusion lengths for the low doped region and highly doped buried layer; $Depth - DepW$ is the W parameter from (6), and LDV and $tauV$ are the high/low junction diffusion length and lifetime according the Long, et al. model [7]. It is assumed that the generated carriers diffuse and are collected at the depletion region of a junction, and therefore creates a photocurrent at the terminal

Table 2: Verilog-AMS calculation of lifetimes and diffusion lengths

```
//Functions to calculate DR lifetimes according to Fjeldly 2001 paper
analog function real DRtauSRH;
   input tn, tinf, p0, Gn;
   real tn, tinf, p0, Gn;
   DRtauSRH=1/(0.5*(tinf-(p0/Gn))
                 +sqrt((p0*tn)/Gn+0.25*pow((tinf-(p0/Gn)),2)));
endfunction

analog function real DRtauAUG;
   input Gn, raug;
   real Gn, raug;
   DRtauAUG=pow((Gn*Gn*raug),0.3333);
endfunction

//Within main code block...
//Calculation of lifetime and diffusion length values
      //Initial lifetime, before SRH Concentration Dependence
t0=4E-8;
      //Calc liftime based on SRH Model in Atlas Man
      //Region and high doped buried layer (BL)
ta=t0/(1+N/5.0E16);
tBL=t0/(1+NBL/5.0E16);

      //Calculate DR dependent lifetimes with Fjeldly Model
tau=1/(DRtauSRH(ta,2*ta,N,Gn)+DRtauAUG(Gn,raug));
tauBL=1/(DRtauSRH(tBL,2*tBL,NBL,Gn)+DRtauAUG(Gn,raug));

      //Diffusion coef of layer and buried layer (BL)
Diff=$vt*ua;
DiffBL=$vt*uBL;

      //Diffusion lengths for layer and buried layer (BL)
LD=sqrt(Diff*tau);
LDBL=sqrt(DiffBL*tauBL);

//Calculate High/Low diffusion parameters from Long 1983 paper
LDV=LD*tanh((Depth-DepW)/LD)+LDBL/cosh((Depth-DepW)/LD);
tauV=pow(LDV,2)/(2*Diff);
```

of the device, only from within one diffusion length from the edge of the depletion region [1]. Therefore, the maximum collection volume for each junction is the volume of the depletion region and the volume of the region within one diffusion length of the depletion edge, or the edge of the dielectric isolation if the distance is shorter.

As discussed in Chapter II the electron-hole pairs generated in the depletion region are assumed to be collected immediately [1]. The carriers generated outside of the depletion region diffuse to the junction in a temporal profile following the form of

$$erf\left(\sqrt{\frac{t}{\tau}}\right) \tag{27}$$

where erf is the error function, t is the time after the start of the pulse, and τ is the calculated carrier lifetime, including lifetime modulation as a result of the dose rate induced carriers [1], [11]. Table 3 shows the implementation of the error function in Verilog-AMS after the numerical approximation from Abramowitz and Stegun, where x is the $\sqrt{t/\tau}$ from (27) and p and $a1$-$a5$ are the coefficients [45]. At a given time t, the distance from the edge of the depletion region over which the generated carriers are collected is the calculated diffusion length multiplied by (27). The photocurrent observed at the device terminals, for one side of the junction follows the equations

$$I_{PC} = G * DR * q * \sum Vol_J\left(X_D, L_D erf\left(\sqrt{\frac{t-T_0}{\tau}}\right)\right) \tag{28}$$

and

$$I_{PC} = G * DR * q * \sum Vol_J\left(0, L_D\left(erf\left(\sqrt{\tfrac{t-T_0}{\tau}}\right) - erf\left(\sqrt{\tfrac{t-T_{STOP}}{\tau}}\right)\right)\right) \tag{29}$$

where G, the generation rate, is $4.3 \times 10^{13} \frac{e-hpairs}{cm^3 rad(Si)}$, DR is the dose rate in rad(Si)/s, and Vol_J is the volume within which the generated carriers are collected. This

Table 3: Verilog-AMS implementation of the error function using the approximation from Abramowitz and Stegun [45]

```
analog function real erf;
  input x;
  real x,p,a1,a2,a3,a4,a5,t;
  begin
    p = 0.3275911;
    a1 = 0.254829592;
    a2 = -0.284496736;
    a3 = 1.421413741;
    a4 = -1.453152027;
    a5 = 1.061405429;

    t = 1.0 / (1.0 + p*x);
    erf =1.0- ( (a1 + (a2 + (a3 + (a4 + a5*t)*t)*t)*t)*t ) * exp(-x*x);

  end
endfunction
```

collection volume is a function of the depletion width X_D, the diffusion length L_D, and the start and stop times for the pulse T_0 and T_{STOP}, respectively. Equation (28) applies from the start of the dose rate pulse to the end of the pulse and (29) is applicable for the time after the end of pulse. The calculation of the volume is highly dependent on the carrier lifetime and the depletion width. As a result, these are the main variables used to calibrate the model to test data. The tuning of these variables is performed through modification of the initial material lifetimes and the average doping in the different regions of the device. These variables have direct relationships to dose rate modulated carrier lifetime, diffusion length, and depletion width. These are also variables with the highest degree of uncertainty in the technology information utilized in the parameterization of the model.

Conductivity modulation is calculated as a function of the number of excess carriers created in the device region and the ratio of the carrier mobilities as given

for n-type silicon by

$$\sigma_n^{-1} = \sigma_{n0}^{-1} \left[\frac{1}{1 + \frac{\delta n}{n_0} \frac{1+b}{b}} \right] \tag{30}$$

where σ_n is the conductivity during the transient radiation pulse in $(ohms - cm)^{-1}$, σ_{n0} is the normal conductivity of the n-type material in $(ohms - cm)^{-1}$, n_0 is the normal electron carrier concentration in cm^{-3}, $b = \mu_n/\mu_p$ (where μ_n and μ_p are the carrier mobilities of electrons and holes, respectively, in the n-type material), and δn is the excess carrier concentration in cm^{-3} [6]. Massengill calculated the excess carrier concentration for low and high injection cases, however, with the Fjeldly dose-rate dependent lifetime model over low to Auger regions, a single excess carrier concentration calculation is utilized

$$\delta n = G * DR * \tau \tag{31}$$

where G, the generation rate, is $4.3 \times 10^{13} \frac{e-hpairs}{cm^3 rad(Si)}$, DR is the dose rate in rad(Si)/s, and τ is the lifetime calculated using the Fjeldly model [11], [6]. The material doping concentration and mobilities are technology parameters also utilized in the calculations in Table 2, where the dose-rate dependent lifetime τ is also calculated. The implementation of conductivity modulation places variable resistors in parallel with the electrical model resistances that have been pulled external to the SPICE model, as shown in Fig. 13. During times before and after the transient radiation pulse, the parallel resistors have very large values, resulting in a total parallel resistance equal to the electrical model resistance. For a dose rate pulse of duration

T the parallel resistance is calculated as

$$R_{MOD}(t) = \begin{cases} 1 \times 10^{12} & ; t < 0 \\ \frac{1}{erf(\sqrt{\frac{t}{0.5\tau}})} \frac{C_m R_0}{(1-C_m)} & ; 0 \le t \le T \\ \frac{1}{erf(\sqrt{\frac{t}{0.5\tau}}) - erf(\sqrt{\frac{t-T}{\tau}})} \frac{C_m R_0}{(1-C_m)} & ; t > T \end{cases} \tag{32}$$

where R_{MOD} is the value of the parallel modulation resistor, R_0 is the value of the externalized resistor from the SPICE model, t is time, τ is the dose rate dependent lifetime calculated following (8) as implemented in Table 2, and C_m is the conductivity modulation factor, which is the multiplier of σ_{n0}^{-1} calculated in (30). The 1/erf is utilized to smooth the change in resistance value in an effort to avoid temporal discontinuities and improve simulation convergence. The parallel resistor implementation includes the following assumptions and conditions:

Assume: $C_m < 1$

if $C_m \ge 1$, then $R_{MOD} = 1 \times 10^{12}$

Assume: $erf(\sqrt{\frac{t}{0.5\tau}}) \ne erf(\sqrt{\frac{t-T}{\tau}})$

if($erf(\sqrt{\frac{t}{0.5\tau}}) = erf(\sqrt{\frac{t-T}{\tau}})$), then $R_{MOD} = 1 \times 10^{12}$

if($t > T$ **and** $R_{MOD} > 1000R_0$), then $R_{MOD} = 1 \times 10^{12}$

Equations (28) and (29) are calculated for both sides of every junction in the device. The 3-D extension of the model is contained in the calculations of the volumes Vol_J, which are dependent on the depletion width and the error function scaled diffusion length. The total collection volume for a junction is the summation of the Vol_J sub-volumes. Each sub-volume represents a rectangular parallelepiped region in 3-D space around the junction with each edge of the volume determined by the depletion region width and scaled diffusion length in the direction of the edge, with

a limit established at the dielectric isolation edge or in the event of a collision with another volume. The volume calculations for a single Vol_J on the outside edge of a junction during the dose rate pulse follow the pseudo-coded methods shown here:

```
XD = calcDepWidth(NA, ND, Bias)
DiffL = LD*erf(sqrt((t-T0)/TauDR))
EX = XD+DiffL
If(EX > dist(junc, IsoX)), then EX = dist(junc, IsoX)
EY = widthJuncY + 2 * (XD + DiffL)
If(EY > dist(junc, IsoY)), then EY = widthJuncY+2*dist(junc, IsoY)
EZ = depthJuncZ+XD+DiffL
If(EZ > dist(junc, IsoZ)), then EZ = depthJuncZ+dist(junc, IsoZ)
Vol = EX*EY*EZ
```

In the pseudo-code above, XD is the calculated depletion width, DiffL is the dose-rate dependent carrier diffusion length, as calculated in (2) and (4) as implemented in the Verilog-AMS code provided in Tables 1 and 2, E[X,Y,Z] are the edges of the rectangular parallelepiped region in 3-dimensions, dist(junc, Iso[X,Y,Z]) is the distance from the junction to the isolation in that direction. It is assumed that the X edge extends from the junction into the region for which the depletion width is being calculated. The width and depth of the junction are measured in the Y and Z edges, respectively. The sub-region volume, Vol, is the volume of the parallelepiped defined by the edges EX, EY, and EZ. The calculation for the inside edge of the junction uses the edges of other volumes as boundary conditions. During the time after the pulse, the distance contributed by the width of the depletion region is eliminated from the

volume calculation. The sum of each of the VolJ sub-regions, on both sides of the junction, is the total collection volume for the junction. The volumes are calculated and updated at every time step in the simulation.

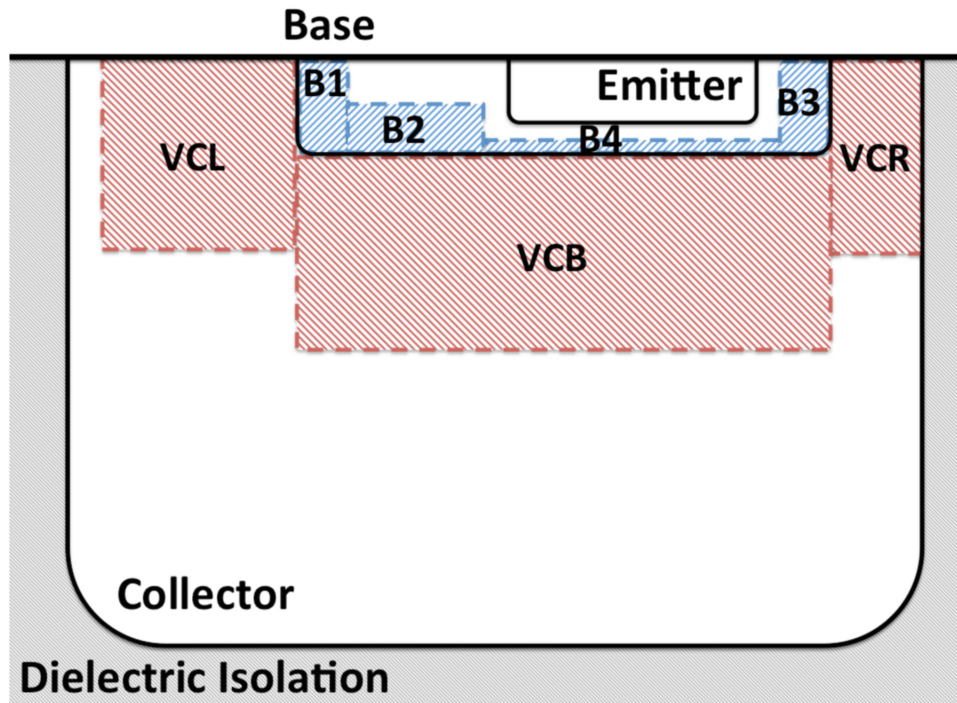

Figure 14: Example 2-D slice of an NPN BJT with the base/collector junction volumes shown. Each of the volumes has been divided into a sub-volume. The other junction volumes are not shown above, but volume B4 is adjusted to reflect the volume collision that would exist if the emitter volumes were shown.

The volume calculations capture the full volume around a junction and take into account the dielectric isolation boundaries, as well as boundary conditions where two volumes collide. In the event of a volume collision, there is a pseudo-boundary created and the carriers up to the boundary are collected. The pseudo-boundary moves spatially if the leading edges of the volumes move in the same direction. A representative 2-D example of the base-collector junction volumes for an example NPN BJT is shown in Fig. 14, where the region outside of the collector is dielectric isolation.

The volumes shown in Fig. 14 reflect the dielectric isolation boundary condition with the limiting of volume VCR and the volume $B4$ is limited due to the collision that would take place with the bottom sub-volume from the emitter/base junction (not shown). The volumes on the base side of the junction, $B1$ to $B4$, and the volumes on the collector side; VCL, VCB, and VCR, will all contribute to the photocurrent that flows from the N-type collector to the P-type base, using equations (28) and (29).

When the reverse bias across the junction collapses, as a result of the photocurrents in the device and current source and/or sink limitations in the surrounding circuitry, the amount of photocurrent must be reduced to match the source/sink limits and prevent forcing non-physical voltages. The bias-dependence of the photocurrent is implemented by multiplying the calculated photocurrent in (28) and (29) by a Fermi function

$$I_{PC-BD}(t) = I_{PC}(t)\frac{1}{1+e^{\frac{V_{p-n}}{F}}} \tag{33}$$

where I_{PC-BD} is the bias-dependent photocurrent, I_{PC} is the photocurrent calculated in (28) and (29), V_{p-n} is the junction bias from the p-type to n-type silicon, and F is the parameter that determines the slope and range of the current reduction. The F parameter determines the junction bias range, +/-FV around 0V, over which the photocurrent drops from approximately 75% to 25% of the calculated photocurrent value.

The dose rate enabled compact modeling methods developed in this work are much more complex than adding independent SPICE piece-wise-linear current sources with calibrated pulse widths and heights across the junctions of a device, following the traditional methods [1], [7], [10], [11]. The advantage of this model is the ability

to capture bias-dependent effects on the collection volume and carrier collection throughout the simulation. Additionally, independent current sources can force node voltages to non-physical values, not reflected in the bias-dependent response of the device, due to the requirement that the source supply a specific current regardless of the bias on the device. However, the complexity of the model results in increased simulation times compared to models that do not incorporate dose-rate effects. We have observed, for moderate to complex analog/mixed signal circuits, simulation time increases of 2-10X. Additionally, discontinuities in complex calculations are always a concern, because they can result in convergence errors. The Verilog-AMS language is well suited to guard against discontinuities by use of transition functions and great care has been taken in developing the model to avoid discontinuous functions [40]

Comparison to Test Data

. The dose rate enabled models have been compared to test data for circuits, ranging from basic parallel device arrays to more complex analog/mixed signal circuit implementations, in bipolar junction transistor (BJT) and silicon-on-insulator (SOI) complementary metal-oxide semiconductor (CMOS) technologies. The arrays and circuits measured in this research are detailed in Appendix A. The data were acquired using the Linear Accelerator (LINAC) facility at the Naval Surface Warfare Center in Crane, IN. The models showed excellent agreement with the peak currents over dose rate and bias, transient current pulse shape, and circuit response. The model performance is first compared to test data from arrays of parallel devices fabricated in each technology and then simulations of full analog/mixed signal circuits are compared to test data from those circuits in each technology.

The models presented in this work are parameterized by the user with three global simulation variables: the dose rate in rad(Si)/s, the pulse width, and the start time of the pulse. The model user does not need to modify any internal variables in the model once the calibration to the technology has been completed. Calibration of the model to test data is achieved primarily by tuning the initial lifetime values, as shown in Table 2, and average doping densities in the device regions. The calibration procedure was performed using the test data from arrays of parallel devices, and the model performance is verified through comparison of the calibrated models to circuit test data. The comparison of the calibrated models to circuit performance demonstrates the models' ability to have minimal user defined parameters and a single set of calibrated internal variables, while operating over many bias conditions and device geometries.

Dielectrically Isolated BJT Model Comparison to Test Data

Fig. 15 shows a comparison of the peak photocurrent of an array of parallel PNP devices and the corresponding dose rate model. The PNP device array consisted of twenty parallel devices, connected on chip with a common emitter, base, and collector terminal bonded to a 40-pin DIP package. There was a 20V reverse bias on the base-collector junction and the emitter was shorted to the base on the test board. Fig. 16 shows a comparison of peak photocurrent from an array of parallel BJT devices with the same bias condition, but a different geometry, than the BJT device data shown in Fig. 15, demonstrating the capability of the models to scale with layout geometry. Fig. 17 shows the response of a Vanderbilt designed operational amplifier test circuit for peak power supply photocurrent and Fig. 18 shows an example output voltage

perturbation response compared to simulation of the amplifier using the dose rate models. The operational amplifier is a complementary folded cascode design based on the amplifier design described in [46] and in Appendix A. The amplifier was connected as a unity gain follower with +/-5 V power supply rails and an input signal of 0 V. The output responses of the test data and the simulation data have good agreement for the first 50 ns after the pulse starts, with the dose rate pulse width being less than 30 ns long. However from 50 ns to 250 ns, there is disagreement in pulse magnitude, but the trend in pulse behavior agrees. The time scale of the disagreement is on the order of the bandwidth of the amplifier and may be attributable to differences in the amplifier feedback; specifically, the lack of parasitic layout and test board elements in the simulation, and non-ideal components in the test setup. The models show good agreement with the data for arrays of transistors and when comparing circuit simulation to experimentally measured circuit behavior.

Silicon-on-Insulator-CMOS Model Comparison to Test Data

Fig. 19 shows a comparison of the transient current pulse shape for an array of SOI PMOS devices compared to the corresponding dose rate model and a TCAD simulation of the device, where the currents from the test data were scaled by the number of devices in the array to reflect a single device response. The PMOS array of over 1000 parallel devices had a common gate, drain, source, and body terminals and was packaged in a 40-pin DIP. The array was biased with the gate, source, and body shorted on the test board to the 5 V VDD rail and the drain was biased at 0V. Fig. 20 shows the response of the dose rate model over bias and dose rate compared to test data. The bias conditions followed the setup utilized for Fig. 19, however

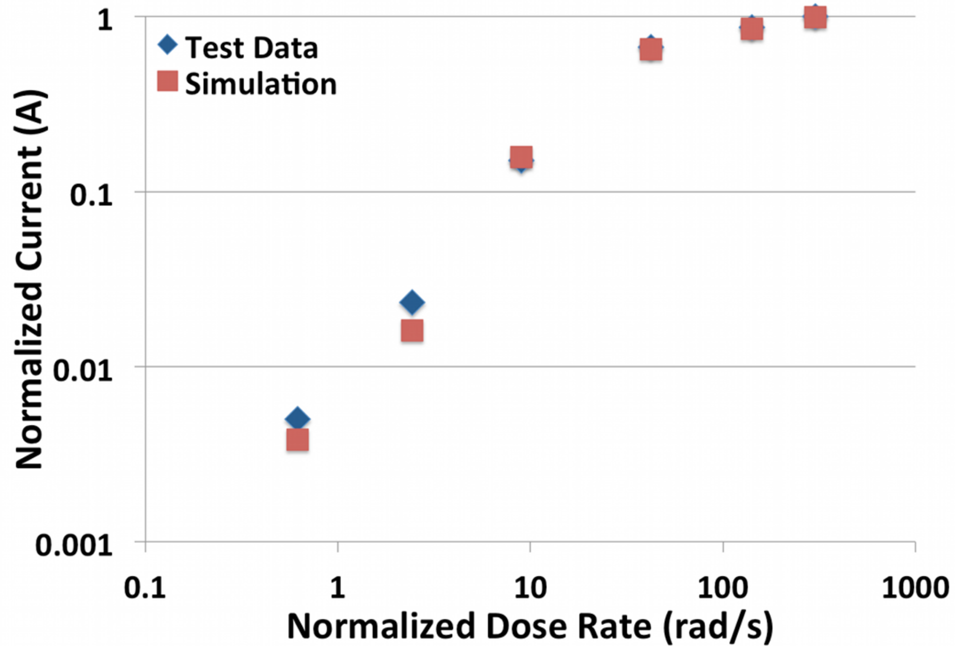

Figure 15: The peak photocurrent produced by a dose rate model in the BJT technology compared to test data results from a linear accelerator dose rate test. The data and model agree well over dose rate.

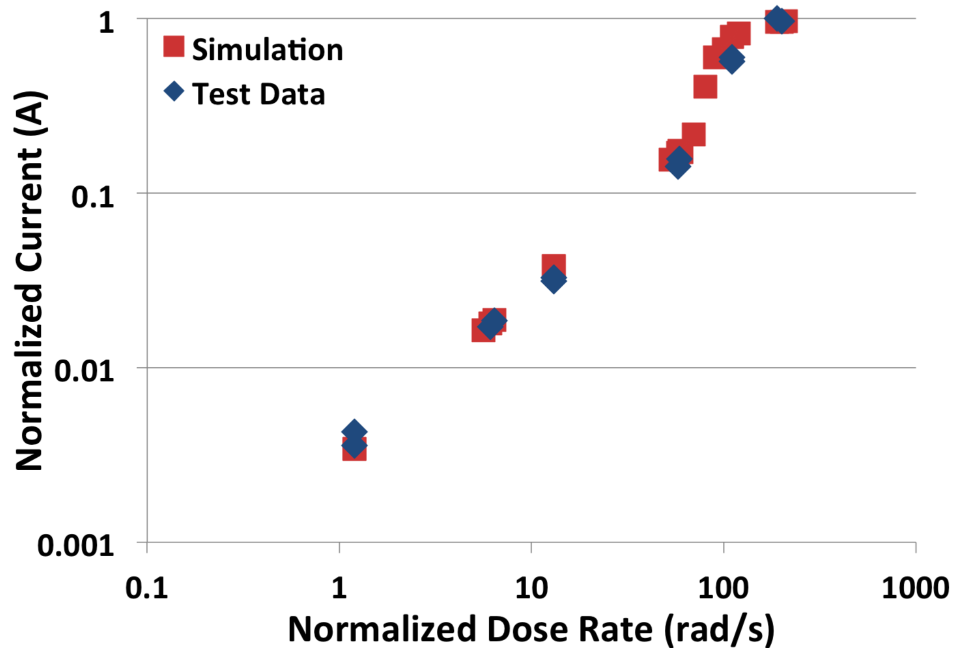

Figure 16: The peak photocurrent produced by a dose rate model in the BJT technology, for different geometry devices from those in Fig. 15, compared to test data results from a linear accelerator dose rate test. The data and model agree well over dose rate, demonstrating the geometrical scalability of the model.

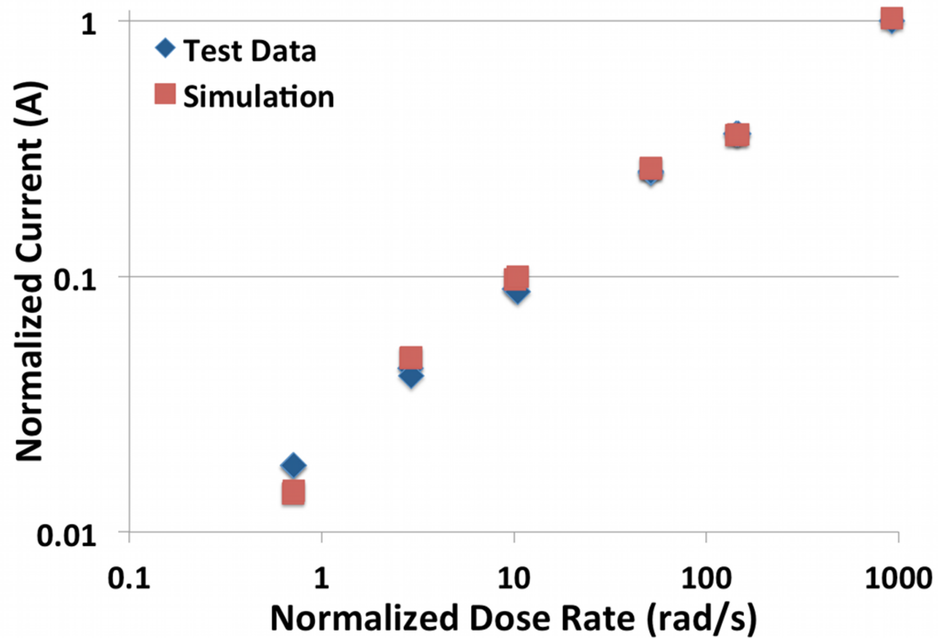

Figure 17: The positive rail photocurrent for an operational amplifier compared to the simulation data. The model data and the test data are in excellent agreement.

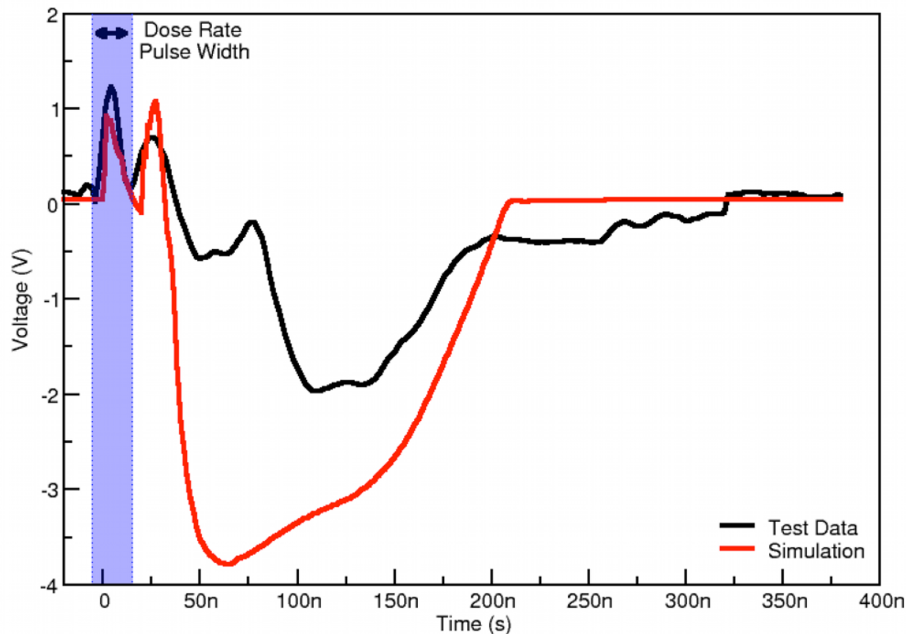

Figure 18: The output response of the operational amplifier for a less than 30 ns dose rate pulse shows good agreement below 50 ns between the simulation and test data. From 50 ns to 250 ns a large negative response is shown in simulation and test, however the magnitudes do not agree, probably due to missing some of the parasitic elements from the test board in the circuit simulations.

the VDD voltage was varied with a range of source-to-drain voltage of 1 V to 5 V and a one-volt step between the biases. The higher biased devices resulted in larger photocurrents. This behavior is expected as a result of the larger depletion regions, and the models reflect this behavior with good agreement to the test data.

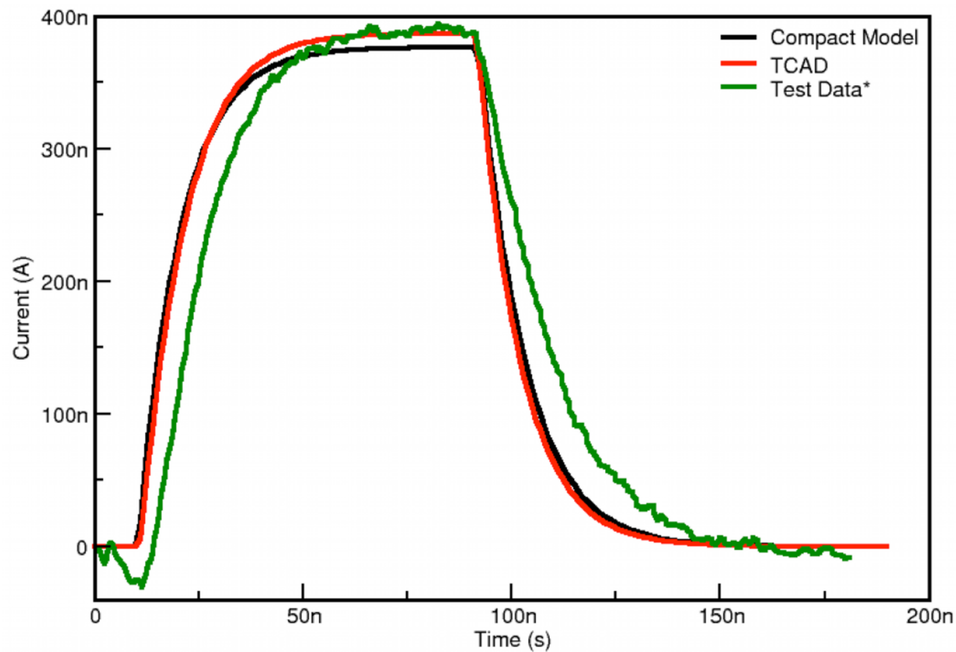

Figure 19: The test data and compact model response show similar transient behavior. The test data were scaled by the total number of devices in the array to reflect the single device simulations for the compact model and the TCAD simulation.

Conclusions

Layout-aware dose rate enabled compact modeling methodologies were developed for application to the modern integrated circuit processes with complex 3-D geometries, device layout configurations, and multiple bias conditions. The methodologies have been applied to multiple dielectrically isolated processes across technology types. The models and test data show good agreement in both the BJT and SOI CMOS technologies, with scalability across device geometry and bias conditions. The models

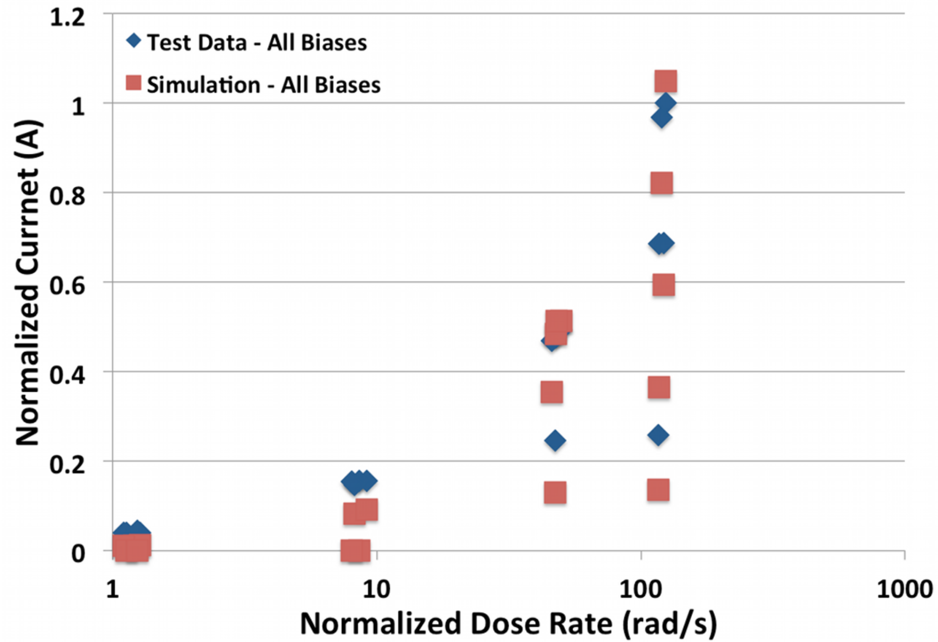

Figure 20: The test data and model simulations show good agreement for the SOI CMOS technology over dose rate and bias. The highest currents were generated by the devices with the largest bias conditions, as expected with increased depletion region volumes at higher bias.

have been calibrated to test data for device arrays and validated to circuit test data. The compact models developed in this work enable accurate simulation of the dose rate response of an integrated circuit. Circuit simulations utilizing these models have run times of approximately two times the nominal electrical simulation time, with very large circuits exhibiting simulation times up to 10X electrical simulation times. The models provide a tool that enables designers to make design decisions and to have greater confidence of successful circuit operation prior to release for fabrication.

CHAPTER V

LAYOUT-AWARE SINGLE-EVENT COMPACT MODELING

Circuit response times in modern integrated circuit technologies are comparable with the characteristic times for single-event charge deposition and collection, meaning that the charge collection process dynamically interacts with and is shaped by the circuit response. With transient pulse widths competing with legitimate signals in circuits operating in the GHz frequency range, the temporal width of the pulse has become a key metric of circuit response [47],[48]. In bulk technologies, charge sharing and well modulation have significant impact on the single-event response of devices and circuits [16], [17], [19], [18]. The single-event response of silicon-on-insulator devices is impacted by the parasitic lateral BJT formed by the drain, body, and source, which is a function of the device layout, technology geometry, and real-time bias perturbation. This work develops layout-aware single-event enabled models for devices in bulk and SOI technologies, the methodologies for capturing the relevant effects, and parameterizing the models.

Single-Event Models for Bulk Technologies

Technology scaling has brought decreasing feature sizes, increased device density, and lower bias conditions to integrated circuit designs, which means charge sharing is a vulnerability that must be accounted for in redundancy based hardened designs in bulk technologies [49]. Charge sharing in scaled technologies has also been exploited as a means of hardening differential circuits and D-flip-flops [50], [51], [52], [53].

Because a single event in scaled technologies may have an effect on multiple devices, even if no device is directly struck, the location of the strike with respect to the device needs to be accounted for in single-event modeling. Capturing transient shape of the pulse and the breadth of the charge collection in multiple devices within a simulation framework is critical to accurate circuit vulnerability predictions.

Bulk CMOS Modeling

The bias-dependent modeling methods described in Chapter III form the foundation of the single-event enabled models discussed here. Charge sharing and well modulation effects are incorporated into the single-event modeling methods developed for bulk CMOS technologies. In addition to placing the bias-dependent current generation within the drain and source resistances as shown in Fig. 8 in Chapter III, bulk CMOS models must also account for the resistance between the transistor body and well/substrate contact, as well as the reverse biased n-well/p-substrate junction in PMOSFET devices. Contacts to the n-well and p-substrate in commercial designs are often sparse and spaced far apart, up to 30μm between contacts to meet minimum design rules [19]. TCAD simulations and heavy-ion testing have shown the considerable impact of well/substrate contacting schemes on the single-event response, where increased contact spacing equates to increasing the resistance between the transistor body and well/substrate contact and larger magnitude single-event responses [17], [19], [18]. Fig. 21 shows the schematics for bulk NMSOFET and PMOSFET single-event models with bias-dependent sources across all P-N junctions, including the n-well/p-substrate, and resistances between the MOSFET body and well/substrate contacts. When multiple devices in close proximity within a well or

in the substrate are simulated, the body nodes of the devices are tied to a common well/substrate resistor, to model the impact of well potential modulation on all devices in the common well. Additionally, the PMOSFET models include a switch to disable the n-well to substrate single-event source, where the source is disabled if the instance is only modeling charge sharing rather than modeling the primary struck device. The process of modeling charge sharing is discussed later in this section.

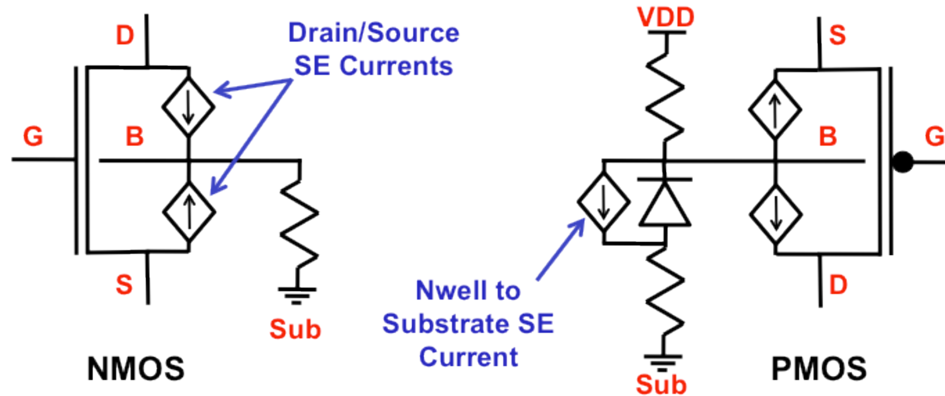

Figure 21: Single-event enabled NMOSFET and PMOSFET subcircuit schematics with bias-dependent sources across all P-N junctions. The NMOSFET has a resistance between the body and the substrate, and the PMOSFET has resistance between the body and VDD (typical n-well potential in digital circuits), as well as a reverse bias diode representing the n-well to p-substrate junction. The intrinsic drain and source resistances, as shown in Fig. 8 are not shown here.

The single-event current sources at each of the P-N junctions are parameterized to set the behavior of the primary I_{SRC}, as shown in Fig. 8 and used in (16), as well as the $RecombParameter$ in (17). Typically, the I_{SRC} is implemented as a double exponential function, as detailed in (13), where the parameters are the total deposited charge, which is used in setting the peak current as in (14), the peak delay time, and the rise and fall time constants. The resistances for the body-to-well contact can be estimated from sheet resistance or resistivity of the well or substrate material, the dimensions of the well, and the average distance to a contact. In sub-100nm

bulk CMOS technologies, the n-well resistance for a maximum contact distance of 30μm is on the order of 2kΩ-5kΩ and substrate resistance is typically 100Ω-500Ω. Single-event hardened circuits benefit from using more well/substrate contacts or even stripe contacts, which significantly reduces the resistance between the device and the well/substrate contact [17], [19], [18].

The parameterization of the model for a single event directly passing though a device will have a very fast rising time constant, on the order of a picosecond, and a falling time constant of tens to a hundred picoseconds [5]. The delay time is typically parameterized as 3-4 times the rising time constant. For charge sharing cases, where a neighboring device was struck or the ion passes near the device without intersecting a depletion region, the parameterization depends on the distance between the ion track and the modeled device collecting shared charge. In [16], Amusan's TCAD simulations of neighboring devices showed a reduction in charge collection with increasing distance between the devices. The results in [16] or similar TCAD studies can be utilized to develop look-up tables of distance vs. single-event charge used to parameterize the deposited charge in the single-event model. Additionally, the rising time constant and delay time will increase, where the ratio of delay time to rising time constant remains approximately 3-4. TCAD simulations have shown that rising time constant approaches three times the direct strike falling time constant, and the falling time constant approaches six times the direct falling strike time constant with increased distance to between the ion track and the device. Table 4 demonstrates an example look-up table for parameterizing the single-event model for different distances between the ion-track with LET of 30MeV-cm^2/s and the device [16] and [54]. Tables are needed for multiple LET values, as the charge and time constant parameter changes

over distance are also dependent on LET. Modeling the charge collected on a device based on the distance from the ion strike to the device provides a starting point for relating the layout of multiple devices in a circuit and their single-event response within that circuit.

Table 4: Example model parameters of direct strike and charge sharing for an LET of 30MeV-cm^2/s vs. distance [16], [54]

Distance (nm)	Charge (fC)	Rise Time (ps)	Fall Time (ps)
0	155	1.5	105
180	113	40	175
540	35	110	320
760	20	155	410
900	15	180	465
1200	5	240	585

Calibration to TCAD

Calibration of model parameters for a single event directly interacting with a device is performed can be performed with two simulation setups and multiple LET values. The simulations include a hard-biased case, where the device terminals are connected directly to voltage supplies and a current limited case, in the form of a mixed mode inverter or using a resistor for current limiting. In the case of a hard-biased NMOSFET device, the drain is connected to VDD and the gate, source, and body are grounded. The hard-biased case provides a means of calibrating the I_{SRC} parameters, and the current limited case is used to calibrate the $RecombParameter$.

As shown in Fig. 3, the hard-biased TCAD simulation case can be approximated with a double exponential waveform. From the hard-biased simulation case, the rise and fall time constants, delay, and collected charge can be extracted. The rising time constant is approximately the time from the start of the pulse to the time that

the pulse rises to 63.2% of the peak value. Similarly the falling time constant is the time from the peak value to the time at which the waveform drops to 36.8% of the peak value. The delay time is the time from the start of the pulse to the time that the waveform reaches the peak value. Because single-event models in Synopsys TCAD deposit charge spatially and temporally in Gaussian means, these temporal parameters are starting points for fitting the double-exponential waveform defined in (13), especially the rising time parameter [34]. The current limited TCAD simulation case, whether the limiting device is the on-condition MOSFET in a mixed mode inverter or a resistor, is used to calibrate the $RecombParameter$ that controls the width of the current plateau as observed in Figs. 7 and 9.

TCAD simulations of neighboring devices or reverse biased P-N junctions are used to calibrate the amount of charge collected by the P-N junctions and the time constants of the collection, at varying distances from the ion track [16], [54]. These TCAD simulations are used to populate LET dependent look-up tables to parameterize single-event models for devices not directly struck by the single event. Hard-bias simulation conditions can be utilized for the charge-sharing TCAD simulations, as the bias-dependence of each single-event source will be a function of the current limited response and the calibrated $RecombParameter$.

Circuit Simulation Results

The capabilities and performance of the bulk CMOS single-event model are demonstrated here with simulations of a hard-biased NMOFET device and a single-event strike in an inverter chain, a common test structure for measuring the distribution of single-event pulse widths. The compact models follow the topology

of Fig. 21 and were implemented using BSIM4 models from the Arizona State University Predictive Technology Models (ASU PTM), targeted to a 45nm bulk CMOS technology [55], [56], [57], [58], [59]. These ASU PTM models are included in Appendix B. The drain, source, and body resistors parameters were set to zero, and the resistors, with correct resistance values for the device sizing, were placed in a subcircuit between the SPICE model drain, source, and body nodes and those same nodes of the subcircuit. The bias-dependent single-event sources were placed across the P-N junctions, as shown in Fig. 21. Simulations were performed using a simulated LET of 30MeV-cm^2/mg, so that the charge sharing parameters shown in Table 4 could be utilized.

Fig. 22 shows the resulting NMOSFET drain current from a simulated single-event strike on an NMOSFET transistor with the drain connected to a 1V DC voltage and the source, body, and gate tied to ground. The resulting current waveform is a double-exponential shape, as observed in Fig. 3. The NMOSFET device was simulated with a width of 104nm and length of 45nm. The single-event model parameters utilized in the hard-bias NMOSFET simulation were applied to the simulation of an inverter chain, where the NMOSFET of the same size in the first inverter was struck.

The inverter chain is shown in Fig. 23, where the chain included six inverters connected serially and the input was tied to ground. The signals are measured at the output of the first, second, and fifth inverters, which are referred to as the Struck Inverter, Inverter +One, and Inverter +Four, respectively. The NMOSFET and PMOSFET devices in the inverters have width to length ratios of 104nm/45nm and 214nm/45nm, respectively. The initial simulation of a single-event strike to the NMOSFET of the Struck Inverter did not include charge sharing, to demonstrate

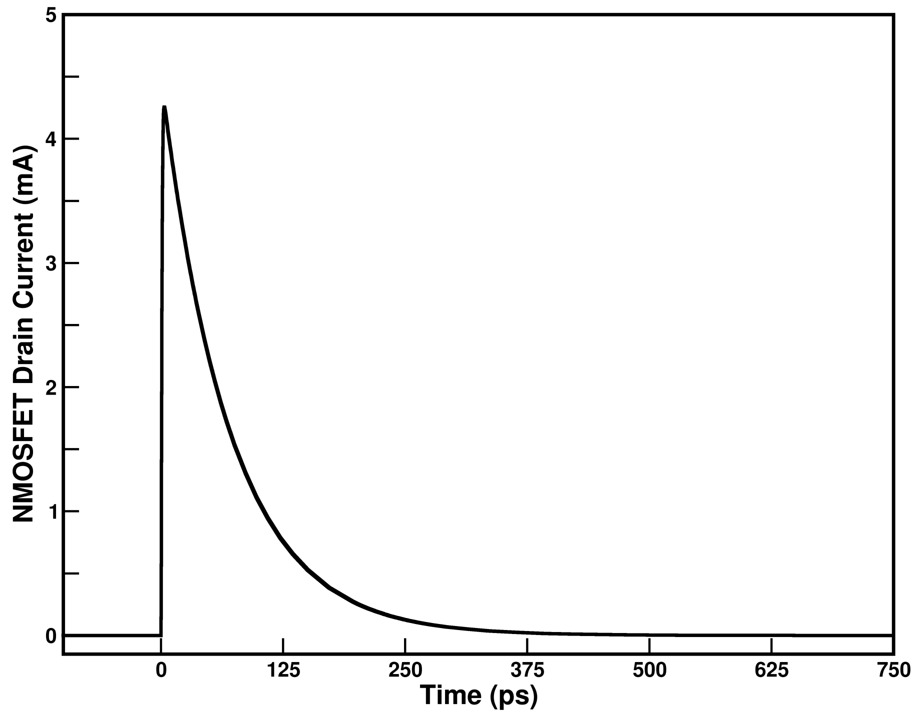

Figure 22: NMOSFET drain current resulting from a simulated single-event strike with an LET of 30MeV-cm^2/mg on a hard-biased NMOSFET device, with drain tied to 1V and source, body, and gate tied to ground.

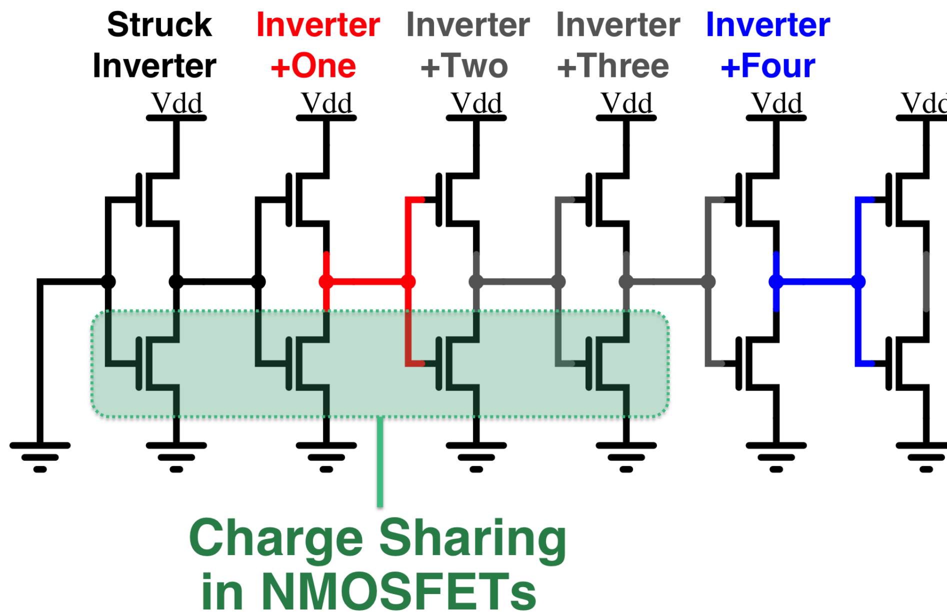

Figure 23: A chain of six serially connected inverters, with the input tied to ground. The outputs of the Struck Inverter, Inverter +One, and Inverter +Four are presented in subsequent figures.

the basic behavior of the single-event model. Figs. 24 and 25 show the single-event output voltage and current transients respectively. The output voltage transient is plotted for the output of the Struck Inverter, Inverter +One, and Inverter +Four. The transient at each plotted point is approximately 250ps in width. Fig. 24 also shows a rise in the local substrate potential, resulting from current flowing from the NMOSFET drain to the body/substrate. This rise in potential is due to the substrate resistance, shown in Fig. 21, where each of the NMOSFET bodies in the inverter chain are tied to the substrate resistor. Fig. 25 shows only the NMOSFET drain current

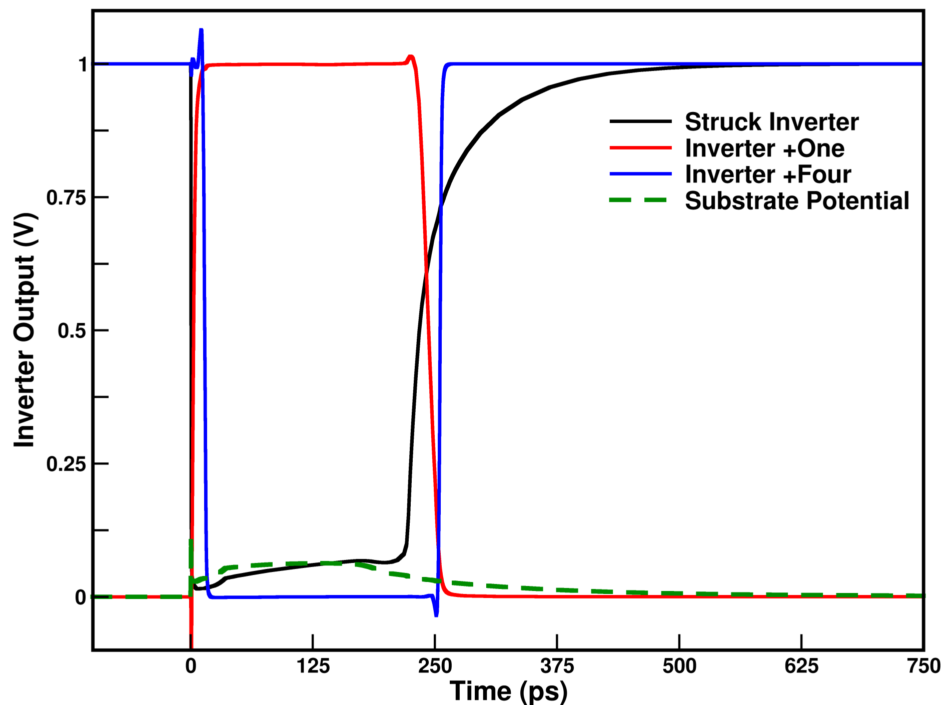

Figure 24: The 250ps long voltage transients resulting from a simulated single-event strike on the NMOSFET of the Struck Inverter, shown in Fig. 23. The transients at the output of the Struck Inverter, Inverter +One, and Inverter +Four are shown.

transient from the Struck Inverter, which demonstrates the current plateau at the level of the PMOSFET drive current discussed previously in Chapter III.

The inverter chain was also simulated with charge sharing among the NMOSFET

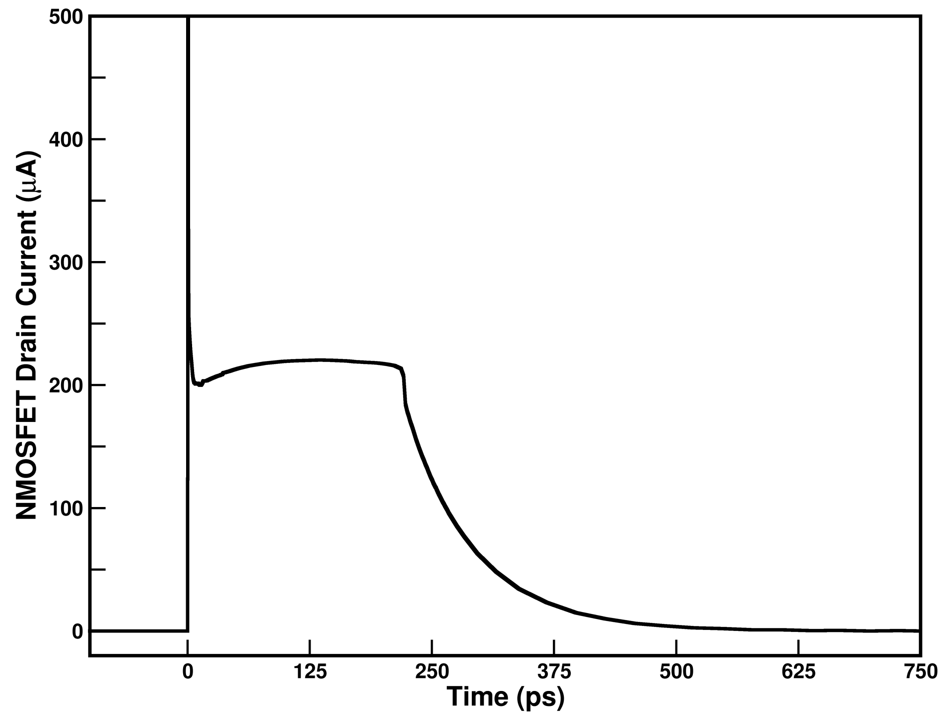

Figure 25: The NMOSFET drain current transient resulting from the simulated single-event strike in the Struck Inverter of the chain of six inverters is shown. The shape of the current waveform shows a plateau at the level of the PMOSFET drive strength.

devices, where the NMOSFET devices sharing charge are highlighted in Fig 23. The charge sharing parameters were extrapolated from Table 4 and assumed an inverter-to-inverter pitch of 180nm. Fig. 26 shows the voltage transients at the output of the Struck Inverter, Inverter +One, and Inverter +Four. As a result of the charge sharing, the transient pulsewidth is quenched, as observed by Ahlbin in TCAD simulations and heavy-ion testing [60]. It should also be noted that the voltage transient at the output of Inverter +One appears to be forming a double pulse, however the double pulse is not sufficient enough in magnitude to propagate [61]. Fig. 27 shows

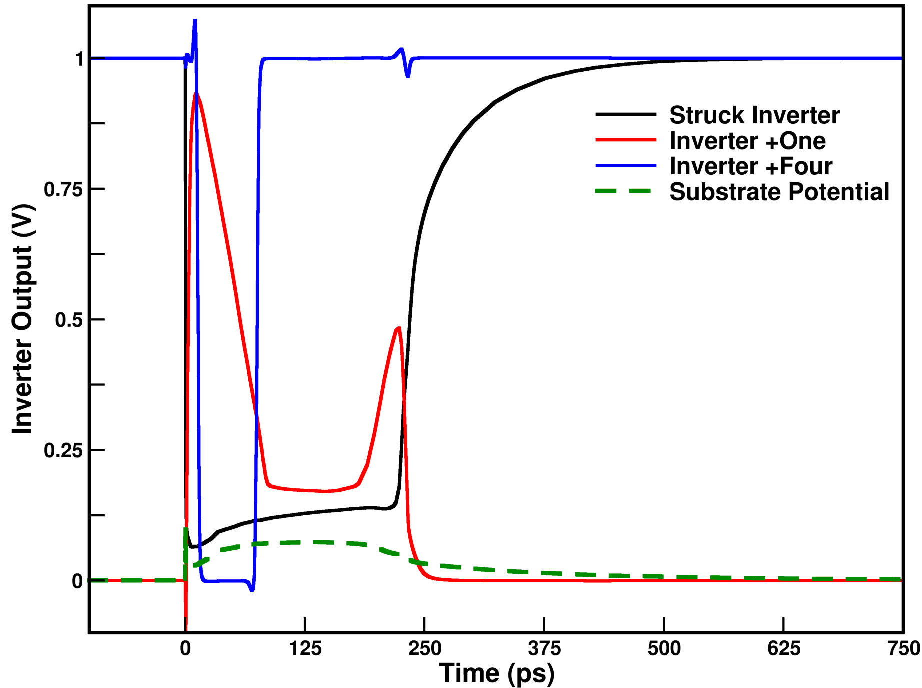

Figure 26: Pulse quenching of the voltage transient is observed when charge sharing is implemented for the strike to the first inverter in the inverter chain of Fig. 23 [60]. The output of Inverter +One also demonstrates a slight double pulse shape, however the double pulse does not propagate [61].

the current transients at the NMOSFET drains of the Struck Inverter and Inverters +One through +Three, which all implement the charge sharing single-event model parameterized with values extrapolated from the values in Table 4.

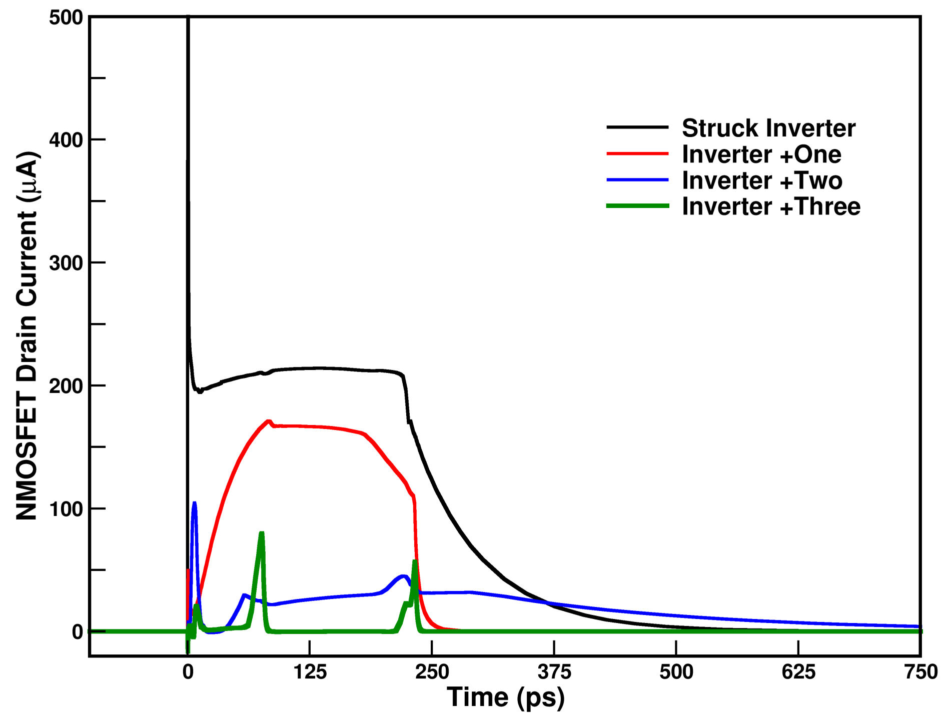

Figure 27: The single-event current transients at the NMOSFET drains of the Struck Inverter through Inverter +Three, the four inverters where the NMOSFETs implement charge sharing. The Struck Inverter current waveform resembles the transient in Fig. 25, and the transients of the subsequent inverters decrease in magnitude and have longer rise and fall times, which correspond to the parameters in Table 4.

Additional circuit simulation results validating the single-event models and methods for bulk CMOS technologies described in this section are presented in Chapter VI. The models are incorporated into a novel automated layout-aware circuit analysis tool that generates simulation netlists from the circuit layout information. The single-event enabled models included in the netlist are parameterized using functions that depend on the LET of the simulated single event and the distance of each device from the location of the ion-track.

Bulk SiGe Heterojunction Bipolar Transistor Modeling

Single-event compact models capable of capturing bias-dependent charge collection behavior, due to dynamic circuit response, and multiple transistor charge sharing in SiGe HBT circuits have been developed to demonstrate the applicability of the single-event modeling methods in a bulk bipolar transistor technology. The bias-dependent modeling techniques follow those presented in Chapter III and have been integrated with the Mextram bipolar junction transistor (BJT) compact model [41], [42], [43]. This model was created to improve simulation capabilities in the characterization of the single-event transient behavior of SiGe HBT circuits compared to traditional methods of inserting an independent double-exponential current source to generate the single-event current effect on the ion-struck device, as detailed in Chapter II. This model utilizes a simple, efficient, and portable implementation in Verilog-AMS and has been exercised using the Cadence Spectre circuit simulator and Mextram transistor models in a commercial process design kit [62]. Calibration of the bias-dependent model and charge sharing behavior were performed using 3-D TCAD simulations [63]. Comparisons of the simulated transient response of a SiGe

bandgap reference circuit, using the TCAD calibrated bias-dependent and layout-aware model, and the measured response from 36 MeV oxygen ion microbeam testing on that circuit, are presented.

36 MeV oxygen ion microbeam testing of a SiGe bandgap reference circuit, shown schematically in Fig. 28, resulted in single-event transients that were relatively small in magnitude but long in duration. At hundreds of nanoseconds, these circuit

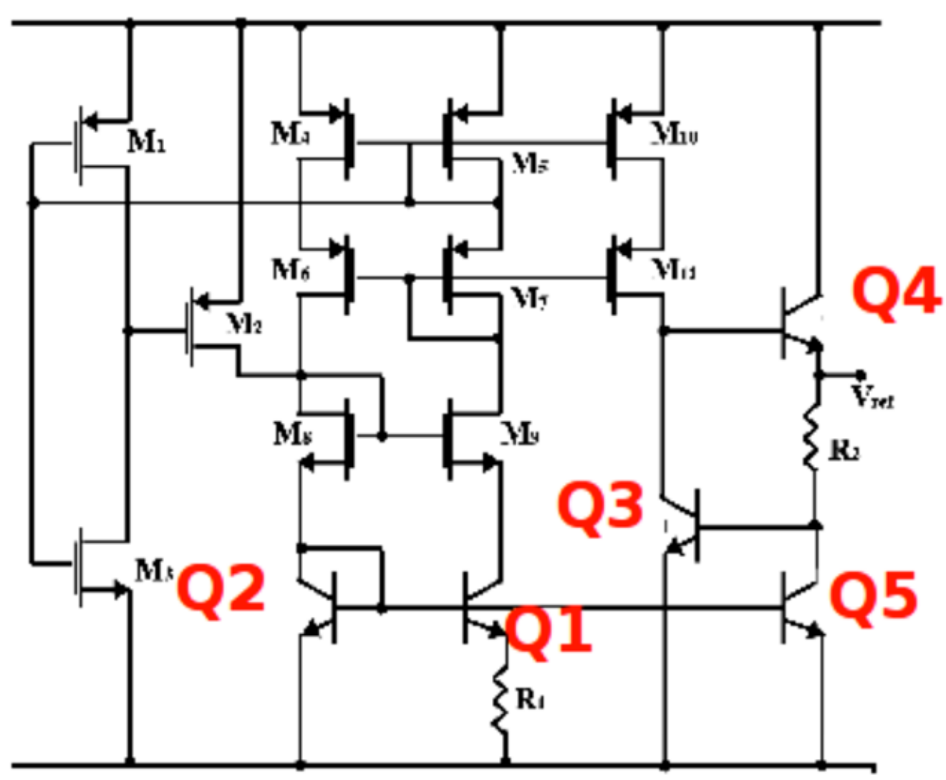

Figure 28: The schematic of the bandgap reference with the location and names of the SiGe HBT transistors highlighted. In test, device Q1 showed the greatest propensity for producing long transients. After [64]

transients were ten times longer than transients observed in single SiGe HBTs [64]. Because microbeam testing was used, the strike locations producing these long transients are known. Traditional double-exponential source modeling of the single-event transient on the device known to produce long transients did not reproduce

the magnitude or duration of the output voltage transient in the reference circuit, as shown in Fig. 29.

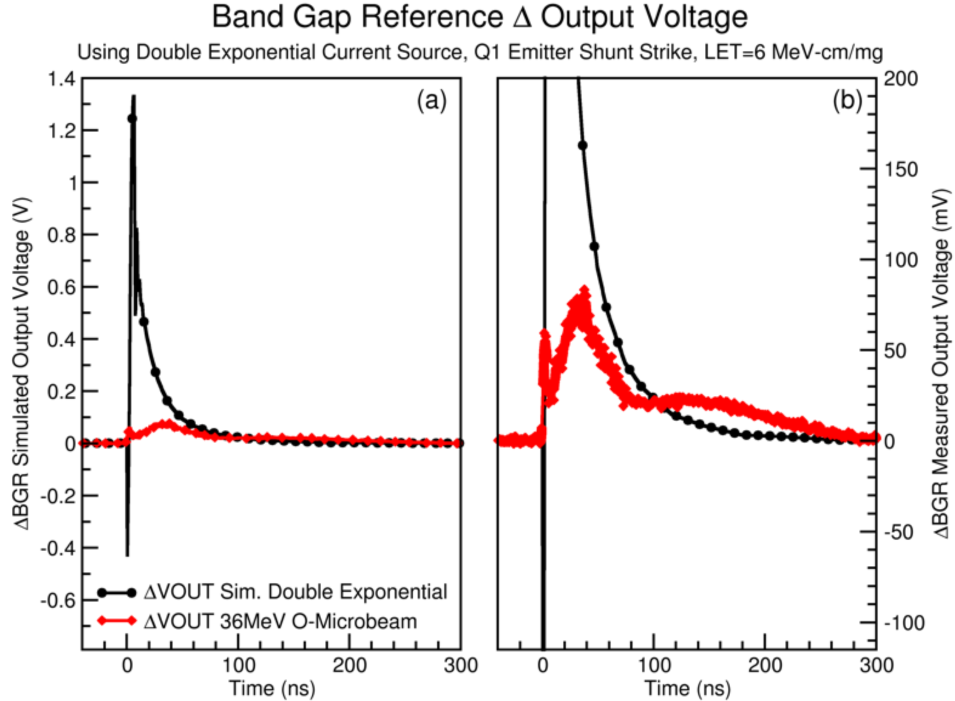

Figure 29: The simulated transient using independent, double-exponential current sources on Q1. The simulated transient is much larger in magnitude (a) and does not reproduce the recovery plateau/tail (b).

Modeling Bias Dependence and Charge Sharing

In Fig. 30, the TCAD data for the collector and substrate currents have a plateau-like shape, similar to the behavior observed and modeled in deep sub-micron CMOS devices and presented earlier in this chapter. Therefore a bias-dependent model, using methods similar to those implemented for bulk CMOS, was developed and integrated into the Mextram HBT model [27], [41]. The plateau behavior is not reproduced when the single event in the HBT is modeled with traditional independent double-exponential sources, as shown in Fig. 30. The current transient in Fig. 30 is less than

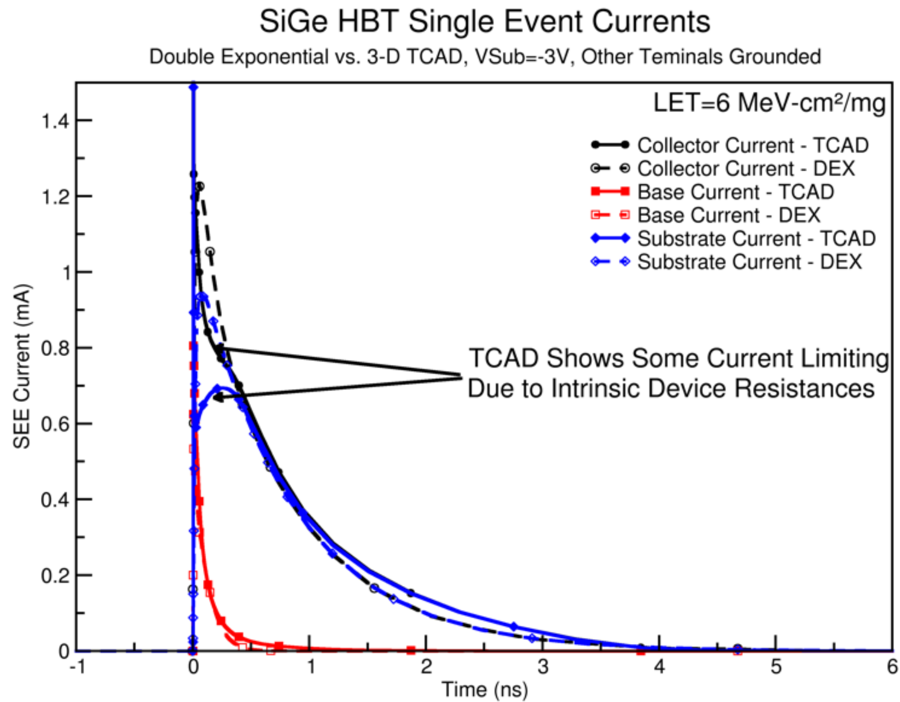

Figure 30: SiGe HBT single-event terminal currents from 3-D TCAD simulation compared to circuit simulation with an independent, double-exponential current source. Simulated ion in TCAD had an LET of 6 MeV-cm^2/mg, which approximates the 36 MeV oxygen ion and corresponds to about 1pC of deposited charge in the device. Note that some current limiting, or bias-dependent behavior can be observed in the TCAD response. This is similar to the bias dependence observed in [27].

10ns, which is consistent with observations from single device testing on HBTs [64].

In addition to the bias-dependence that is not captured with the double-exponential source, as seen in Fig. 30, the low magnitude and long duration tail in Fig. 29 indicates that some device-to-device charge sharing is occurring, which was initially thought to be improbable. Even with the deep isolation trenches around the HBT devices, 3-D TCAD simulations of two devices, space 16μm apart, did indicate the presence of multi-device charge collection. TCAD simulations were performed with strike locations occurring: 1) at the emitter of one device: 2) at a position 4μm outside of one device and between both devices: and 3) at the midpoint (8μm from each device). Fig. 31 shows the devices used in the 3-D TCAD simulations, specifically the third simulation case. The shared charge resulted in a small collector-substrate transient with a magnitude of 3-6μA and a width of 20-50 ns.

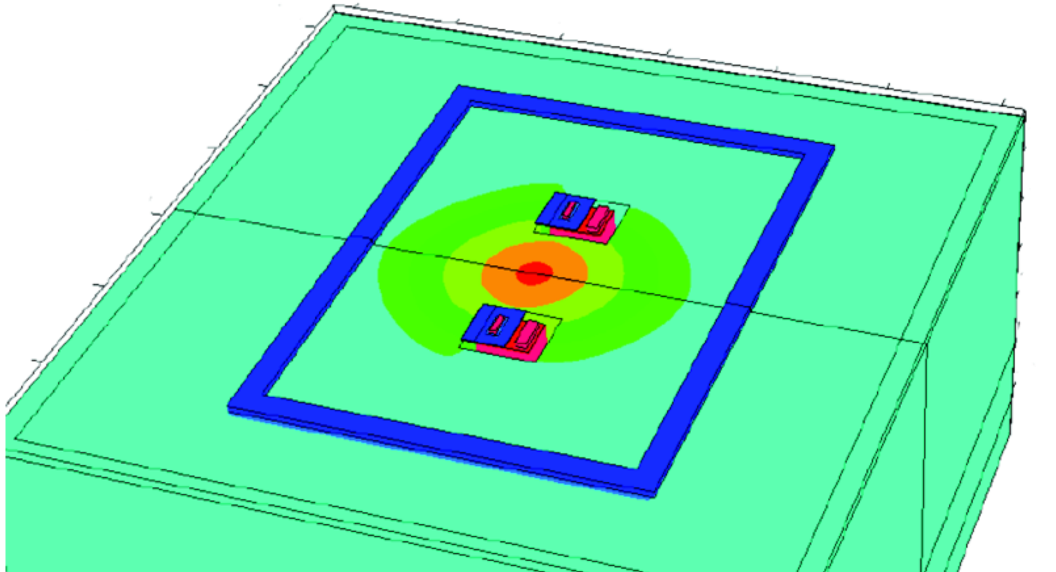

Figure 31: Two SiGe devices in 3-D TCAD with a single-event strike depositing charge at the midpoint between the two devices, simulation case 3. Each HBT device has deep-trench isolation, and the strike is occurring outside of that isolation. This structure was used to measure charge sharing for normal incidence strikes at various positions relative to the two devices.

The bias-dependent single-event model used in this work follows the methods used for bulk CMOS [27]. In the SiGe HBT model, there is a bias-dependent current source, as discussed in Chapter III, for each device junction in the SiGe HBT: emitter-base, base-collector, and collector-substrate. The bias-dependent sources were integrated inside the intrinsic collector, base, and emitter resistances of the Mextram model within a subcircuit [41]. Embedding the bias-dependent model in a subcircuit with the Mextram model has two primary advantages: 1) the bias-dependent calculations can account for the parasitic resistances at the terminals of the HBT model, and 2) there is no interruption to the typical design and simulation flow in the commercial tool flow e.g. there are no extra devices or instances that a designer needs to attach to a device or circuit node. To use the model, a designer merely specifies which device uses the single-event model and the parameters for the single-event pulse generated by the model.

Because the model has bias-dependent sources for each junction, the amount of deposited charge for each junction can be specified, or calculated with functions, individually. Therefore, in the case of charge sharing, the model can be parameterized in a manner where only the collector-substrate junction of the non-primary struck device will be pulsed. TCAD simulations showed that the only junction to collect shared charge is the collector-substrate. With the charge sharing characteristics derived from the varied strike location in TCAD simulations the parameters for the bias-dependent model can be empirically fit and parameterized with a lookup table for the collector-substrate junction of neighbor devices when simulating single-events and charge sharing in SiGe HBT circuits.

Calibration to TCAD

The bias-dependent model was calibrated to 3-D TCAD simulations. Model parameters were extracted for: 1) a direct single device strike, and 2) cases of shared charge being collected by multiple devices, as in Fig. 31. A lookup table, using the distance between the single-event hit location and the device collecting the shared charge, was derived from the results of the varied strike location TCAD simulations. Fig. 32 shows the TCAD and the bias-dependent model terminal currents for a single struck device. Fig. 33 shows the collector currents of two devices from TCAD, where the strike is positioned 4μm from one device and 12μm from the other, and the calibrated bias-dependent model that is parameterized using the lookup table and the strike to device distances.

Circuit Simulation Results

The bandgap reference circuit was simulated using the TCAD calibrated bias-dependent model. Two simulations were performed, one with the bias-dependent model applied to a single transistor as was done in the simulation using the double-exponential current source, and another including the charge sharing parameters applied to neighbor devices in the circuit layout.

The device Q1 showed the greatest propensity for producing long transients during the microbeam testing [64]. In the circuit layout, device Q1 comprises 32 identical devices that form a ring (a common centroid layout [65]) around the four identical devices that comprise Q2. The Q1 devices also abut the four identical devices that comprise Q3. Fig. 34 shows circuit layout with the anticipated charge sharing radius and the struck Q1 device highlighted. The devices within the charge sharing

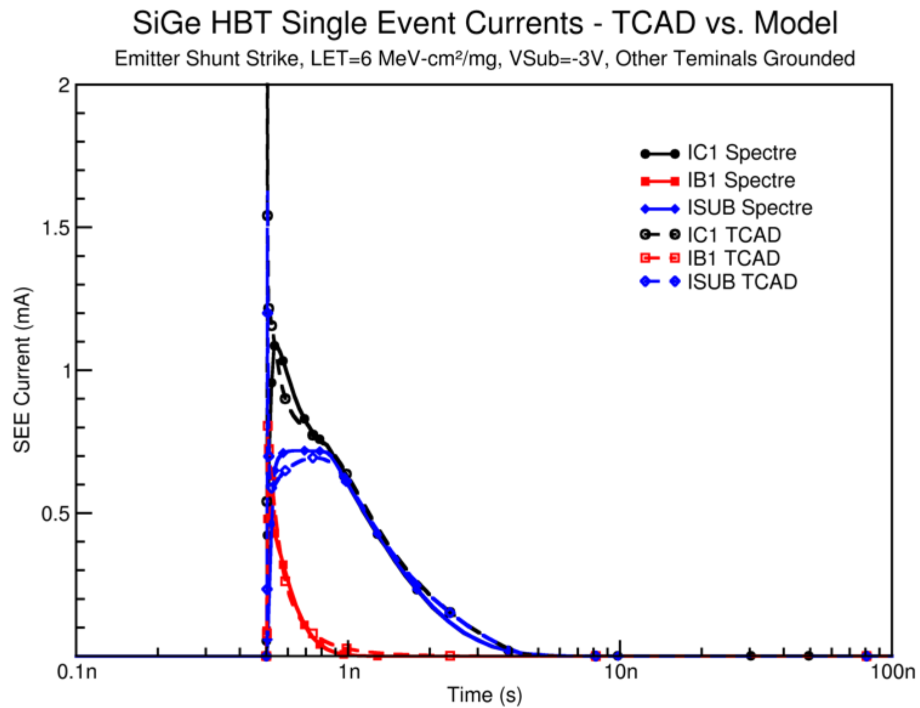

Figure 32: The collector, base, and substrate terminal currents for a 3-D TCAD simulation compared to the currents from the bias-dependent model. The bias-dependent model captures the current limiting in the substrate due to the intrinsic resistances, unlike the double-exponential model in Fig. 30.

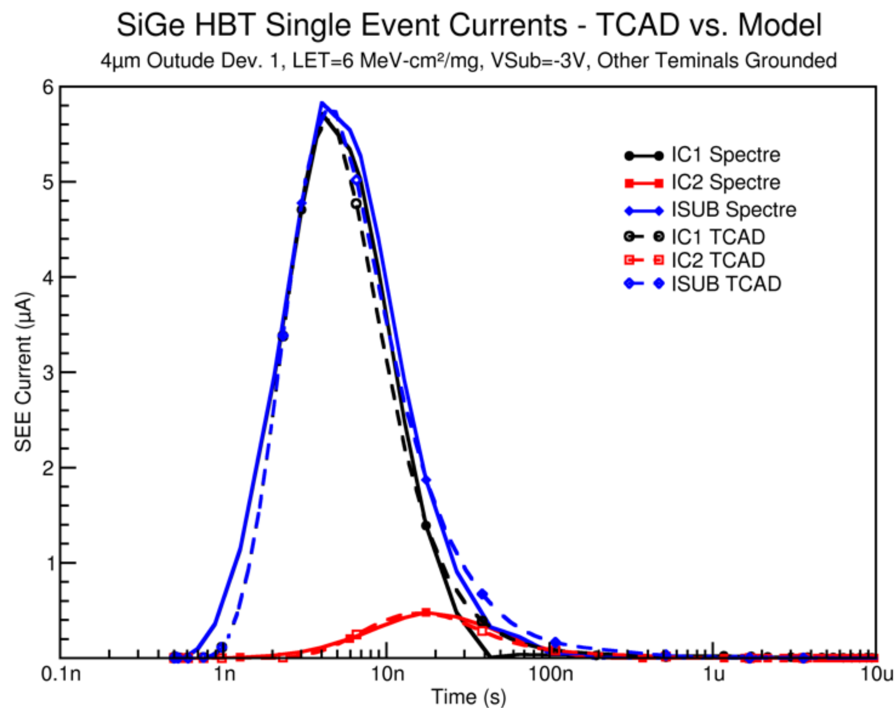

Figure 33: The collector currents from 3-D TCAD and the calibrated bias-dependent model. The strike was simulated 4μm from one device and 12μm from the other. The currents are the result of shared charge collected at the collector/substrate junction of the devices. The currents are much smaller in magnitude and longer in duration.

radius were modeled using the single-event enabled model, including bias-dependent effects and charge sharing, and the remaining devices use the foundry-provided PDK Mextram model. The collector-substrate single-event parameters for charge sharing were calculated using the lookup table derived from the TCAD simulation results. Fig. 35 shows the transient measured during the microbeam testing and the two simulation cases: 1) a single device with the bias-dependent single-event model, and 2) the primary struck device with charge sharing parameters applied to neighbor devices.

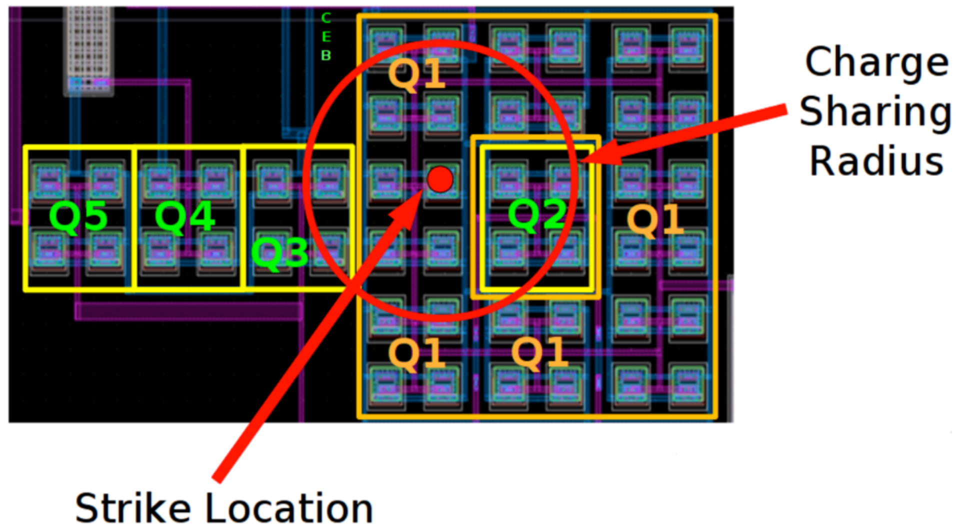

Figure 34: The layout of the SiGe HBT devices Q1-Q5, where Q1 and Q2 are in a common centroid layout. The charge sharing radius and the strike location are highlighted. The simulation parameters were calculated using the distances of devices from the strike and a lookup table. Schematic in Fig. 28 [64].

Using the bias-dependent model, the output transient resembles the measured transient. In the simple case, where a strike was simulated on a single instance of Q1, the elongated tail is not present. When charge sharing parameters were added to the neighbor devices within the charge sharing radius, the simulated result is a long duration transient with a peak magnitude similar to the measured transient. While

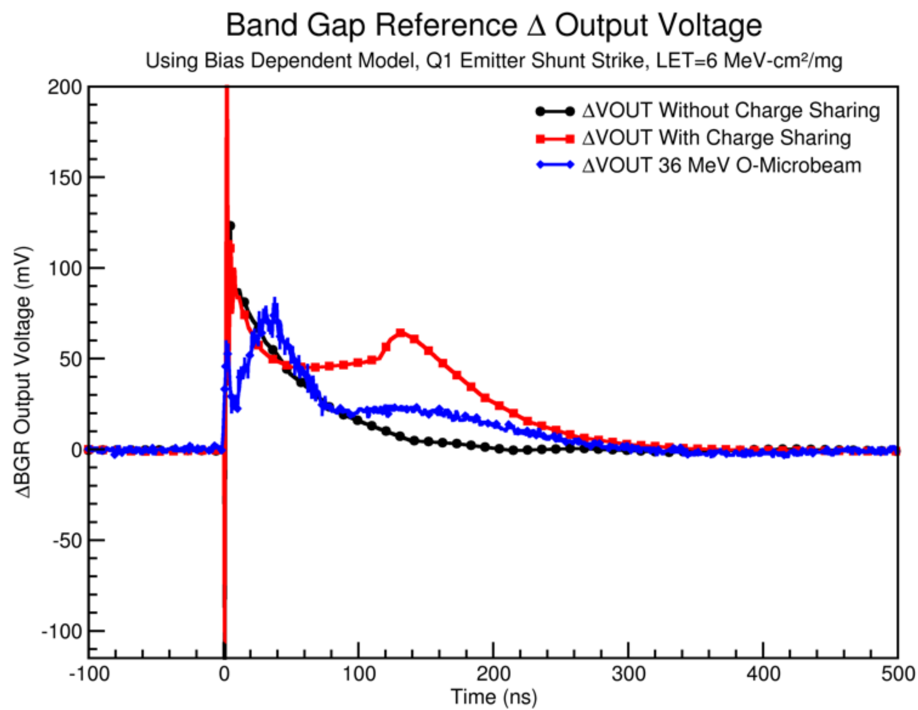

Figure 35: The comparison of the measured transient and the simulated transients using the bias-dependent single-event model. The simulation of the single device does not produce the elongated tail. The charge sharing simulation results in an elongated tail, however the magnitude is about 2X measured.

the elongated tails from the measured and simulated transients are only somewhat similar in magnitude, they are very similar in duration. The closeness of these results is remarkable considering the bias-dependent model is calibrated to TCAD only and not to single-device or charge sharing test data.

Geometry-Aware Single-Event Model for SOI MOSFETs

As discussed in Chapter II, the Kerns and Massengill model topology for single-event simulation in partially depleted silicon-on-insulator CMOS devices has been the standard since the late 1980's [22], [23]. A geometry-scalable and geometry-aware single-event enabled model topology has been developed for sub-50nm partially depleted silicon-on-insulator technologies. The model implements bias-dependent modeling concepts and charge collection amplification resulting from the parasitic lateral BJT that is inherent in in the physical structure of the SOI MOSFET. The parasitic BJT amplification is implemented using equations based on the SPICE Gummel Poon BJT model [66], [3]. The bias-dependent single-event current model and the parasitic BJT model have been integrated in a single Verilog-AMS module, which also includes functions for geometry scalability and ion angle incidence calculations.

Lateral BJT Implementation in Single-Event Model

The industry standard model for partially depleted SOI MOSFET modeling in SPICE simulators is BSIMSOI. The BSIMSOI model includes a lateral parasitic BJT, where the base of the BJT is connected to the internal body node. The BSIMSOI model has two externally accessible body nodes, internal and external, where the

intrinsic body resistance is between the two nodes [44]. The external body node is required to be included in the MOSFET instance in SPICE, however the inclusion of the internal body node is optional and often not utilized. In SPICE models of floating body SOI devices, the external body node is connected to a floating node, where each device has a unique floating node.

Injecting a single-event current into the internal body node should result in an amplification of the injected current, as a result of forward biasing the body-source junction and turning on the parasitic BJT. However, injecting current from a piece-wise-linear current source, using the output of 3D TCAD simulations, or a bias-dependent current source, calibrated to TCAD simulations, into the internal body terminal using the manufacturers supplied models did not result in amplification of the injected current by the parasitic BJT included in BSIMSOI. However, the parasitic BJT included in BSIMSOI did amplify DC and low frequency transient current pulses, indicating that the parasitic BJT in the BSIMSOI model does not respond to stimuli on the time-scales of a single-event current. Therefore, a lateral parasitic BJT model, capable of responding on the time-scales of a single-event current pulse was implemented as an integrated part of the bias-dependent single-event model.

In this work, the foundational modeling concepts developed with the bias-dependent single-event model are extended to include a parasitic BJT model for partially depleted SOI MOSFETs. The parasitic BJT model is implemented using the BJT equations developed for the SPICE Gummel Poon model, including the high injection effects, with the assumption that the Early effect of the parasitic BJT is negligible [7], [8]. The parasitic BJT equations have been integrated with the solution of the system of equations (16)-(18), presented in Chapter III, in the

behavioral modeling language, eliminating the additional SPICE BJT element in the model.

The parasitic BJT base is connected to the internal body node of the BSIMSOI model. The BJT collector and emitter are connected to the drain and source, inside the intrinsic drain and source resistances. In a typical digital NMOSFET application, where the drain is biased at a higher voltage than the source, the parasitic BJT is connected to the drain and the emitter is connected to the source. The implementation discussion will center on this case.

The bias-dependent single-event current source, as defined in (16)-(18), is injected into the body/base of the MOSFET and connected between the drain and body of the MOSFET. As the single-event source injects current into the body, the body voltage increases, especially in floating body devices, and the body-source junction is forward biased. The parasitic BJT sources additional current from the drain/collector terminal and shunts the current to the source/emitter as electrons are injected into the base from the source and are collected in the drain. As the drain potential drops, the BJT enters the saturation region and the drive current capability of the pull-up device sets the level of the plateau current until the potentials are restored.

The parameters for the BJT model equations are calculated from the technology construction, device dimensions, and the BSIMSOI model parameters provided by the manufacturer. For example, carrier mobility, lifetime, and doping concentration are a function of the technology and are used to calculate reverse saturation current and initial base charge. The geometry of the MOSFET is provided by the design parameters and impacts the calculation of the parasitic BJT parameters. The BSIMSOI SPICE model parameters in the process design kit (PDK) are used to

Table 5: Parameters Utilized in the Parasitic BJT Model

Parameter	Description	Source
n_{diode}	I_{BJT} diode ideality factor	PDK
n_{bjt}	Q_2 diode ideality factor	PDK
nch	Channel/body doping concentration	PDK
tsi	Top silicon thickness	PDK
tt	Transit time	PDK
W_{finger}	Drawn width of MOSFET finger	Design
L	The MOSFET drawn gate length	Design
W_{min}	The minimum drawn width	Technology
μ_n	Electron mobility	Technology
μ_p	Hole mobility	Technology
τ_n	Electron minority carrier lifetime	Technology
τ_p	Home minority carrier lifetime	Technology
$N_D(N_A)$	Drain/source doping concentration	Technology
nf_E	Number of fingers collecting charge	Calculated
n_d	$I_{BS'}$ diode ideality factor	Fitting Parameter

set diode ideality factors, body doping concentration, and junction transit times. Table 5 lists the model parameters for the BJT and body-source diode, as well as a brief description and the source of the parameters. The equations that govern the parameterization of the BJT and body-source diode model equations are

$$I_S = q\left(\sqrt{\frac{\mu_p V_t}{\tau_p}}\frac{n_i^2}{N_D} + \sqrt{\frac{\mu_n V_t}{\tau_n}}\frac{n_i^2}{nch}\right)\frac{W_{finger}}{W_{min}} \times nf_E \tag{34}$$

$$I_{KF} = I_{KR} = q \times nch \times \frac{W_{finger} \times L \times tsi}{tt} \times nf_E \tag{35}$$

$$Q_2 = \frac{I_S}{I_{KF}}\left(e^{\frac{V_{BS'}}{\left(n_{bjt}V_t\right)}} - 1\right) + \frac{I_S}{I_{KR}}\left(e^{\frac{V_{BD'}}{\left(n_{bjt}V_t\right)}} - 1\right) \tag{36}$$

$$Q_B = 0.5 + \frac{\sqrt{1 + 4Q_2}}{2} \tag{37}$$

where I_S is the reverse saturation current, q is the elementary charge in coulombs, n_i is the intrinsic carrier concentration of silicon, nf_E is the number of transistor

fingers that collect charge, and $V_{BS'}$ and $V_{BD'}$ are the body-source and body-drain biases, respectively. The assumption of the Early effect being negligible is shown in (36) and (37), where the traditional expression for Q_1 in the Gummel Poon model is set to unity [3]. The dependence on the width of the transistor-gate finger and the number of fingers collecting charge, nf_E, is required to calculate the impact of only the perturbed portion of the device. Within the electrical MOSFET model, the finger width and number of fingers, specified in the MOSFET instance line as nf, are multiplied to provide a total device width, which is used in the calculation of MOSFET electrical currents. If the single-event model calculations relied only on the total width of the device, the parasitic BJT amplification would be significantly over predicted.

The parasitic lateral BJT collector current equation

$$I_{BJT} = I_S \frac{e^{\frac{V_{BS'}}{(n_{diode} V_t)}} - e^{\frac{V_{BD'}}{(n_{diode} V_t)}}}{Q_B} \tag{38}$$

depends on the body-source and body-drain biases, as well as the parameters from Table 5 and the high injection factor Q_B from (37). The model includes an additional current source to handle the discharge of the body potential after the single-event, which is modeled as a very weak body-source diode

$$I_{BS'} = I_S \frac{e^{\frac{V_{BS'}}{(n_d V_t)}} - 1}{Q_B} \tag{39}$$

where n_d is large, approximately 1.6. The BJT and diode equations are implemented to maintain the symmetry of the MOSFET, where the drain and source terminals are interchangeable with respect to bias and connections in the circuit. At the time of the single-event pulse, the model determines which terminal will act as the collector in the parasitic BJT and which terminal will act as the emitter, based on which has

the higher bias with respect to ground. Additionally, the single-event model and parasitic BJT can be disabled with an instance switch, effectively removing the need to solve the equations at each time step, reducing the simulation overhead. This is an improvement over the use of full SPICE components for which the equations need to be solved at each time-step even if they are not being utilized to simulate a single-event on the device. Fig.36 shows a schematic representation of the SOI NMOSFET single-event model with the primary single-event and parasitic BJT sources biased for normal operation with the drain biased high and the source at a lower potential.

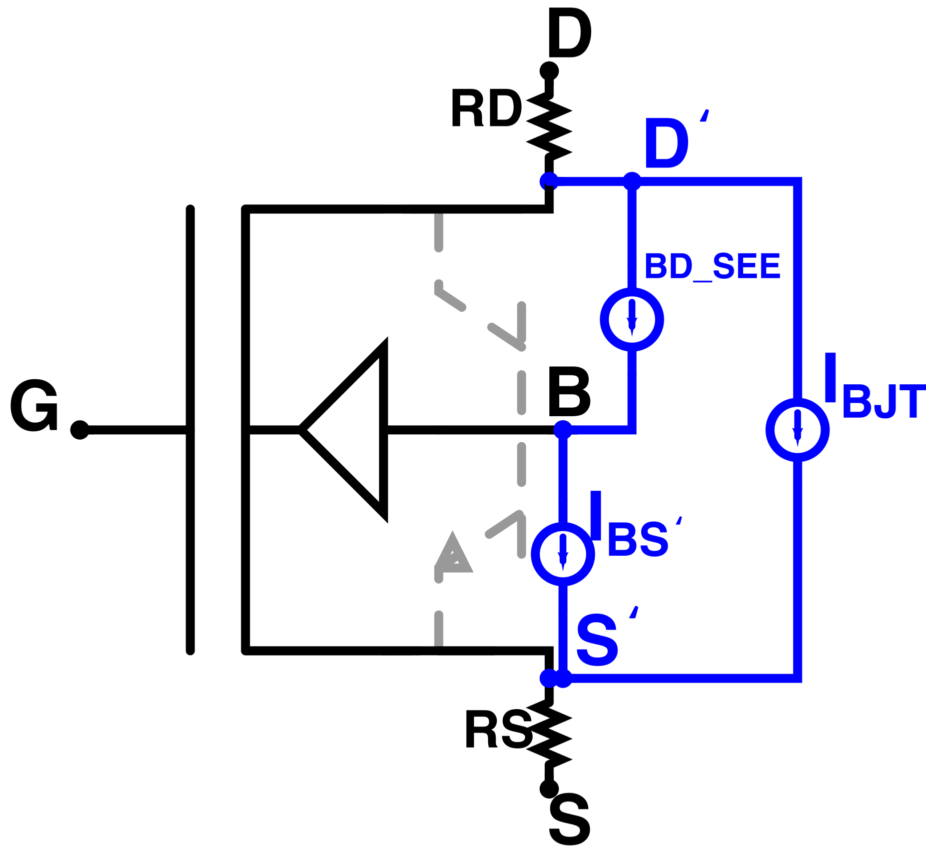

Figure 36: Schematic representation of the SOI single-event model developed in this work, with the bias-dependent single-event source BD_SEE, the BJT current source I_{BJT}, and the weak body-source diode model $I_{BS'}$. The parasitic BJT is shown as a dotted line BJT symbol overlaying the MOSFET.

Geometry-Aware Implementation

The ion incidence angle, physical layout, and geometry of the struck device influence the charge deposition and charge collection at the device junctions. Sub-50 nm technologies have very structured and gridded design rules for device construction. The single-event enabled model utilizes basic device layout parameters, e.g., width, length, and number of transistor-gate fingers, as well as technology design rules, such as the poly-poly pitch, to determine how the device layout and geometry will influence the device response. These parameters allow the single-event model to develop a basic geometrical representation of the MOSFET for ion track length calculations.

Tilt and roll angle of incidence determine the ion track length in the active silicon regions of the SOI device. Geometrical formulas are derived within the model to calculate the simulated ion track cord within the active silicon and the total charge deposition track length as a function of device layout parameters, technology design rules, and user provided tilt and roll angles. The total deposited charge is calculated by converting the user-provided LET and calculated deposition track length into the total deposited charge using

$$Q_{Dep}(pC) = 1.035 \times 10^{-2} * LET\left(\frac{MeV - cm^2}{mg}\right) * L_{Dep}(\mu m) \tag{40}$$

where Q_{Dep} is the total L_{Dep} is the track deposition length [5].

These geometrical formulas also calculate the number of SOI transistor body-drain, body-source junctions that will potentially collect charge, which is used as a scale factor, nfE, in the parasitic BJT model in equations (34) and (35) above. This scale factor is used in the same manner as the area parameter in the SPICE Gummel Poon BJT model instantiation [66]. Through TCAD calibration and data validation,

it was determined that devices with multiple transistor-gate fingers have parasitic BJT activation in two bodies with a shared drain (reverse biased) region between them. This dual parasitic BJT activation occurs when one of the two bodies is struck or when the shared drain is struck. This required an nf_E of 2 for normal incidence and low tilt angle simulations, indicating within the single-event model that multiple transistor bodies collect charge with a normal or near-normal incidence ion strike.

Calibration to 3D TCAD

TCAD is used as a calibration tool for transient radiation modeling, to understand the internal charge movement and to provide an initial data set for model comparison. 3D TCAD models for NMOSFET and PMOSFET devices were developed and calibrated to DC and transient electrical sweeps from the models contained in the manufactures PDK. A large matrix of TCAD simulations was performed covering a range of linear energy transfer and bias conditions. The results of these simulations clearly show the carrier movement in the parasitic BJT and provide a data set for calibrating the parasitic BJT model. Fig. 37 shows the parasitic BJT through electron and hole current densities, as well as a textbook example of the carrier movement in a BJT [67]. Fig. 38 compares the charge deposited, calculated based on simulated linear energy transfer and track length, in the TCAD simulation to the collected charge in the TCAD simulation and the single-event enabled SOI model with a parasitic BJT, for the drain hard biased to VDD and gate and source tied to ground. Fig. 39 compares the deposited charge to the TCAD and single-event enabled SOI model collected charge for an inverter off NMOSFET strike. Fig. 40 shows current and voltage waveform shape and pulse width generated by the single-event enabled model

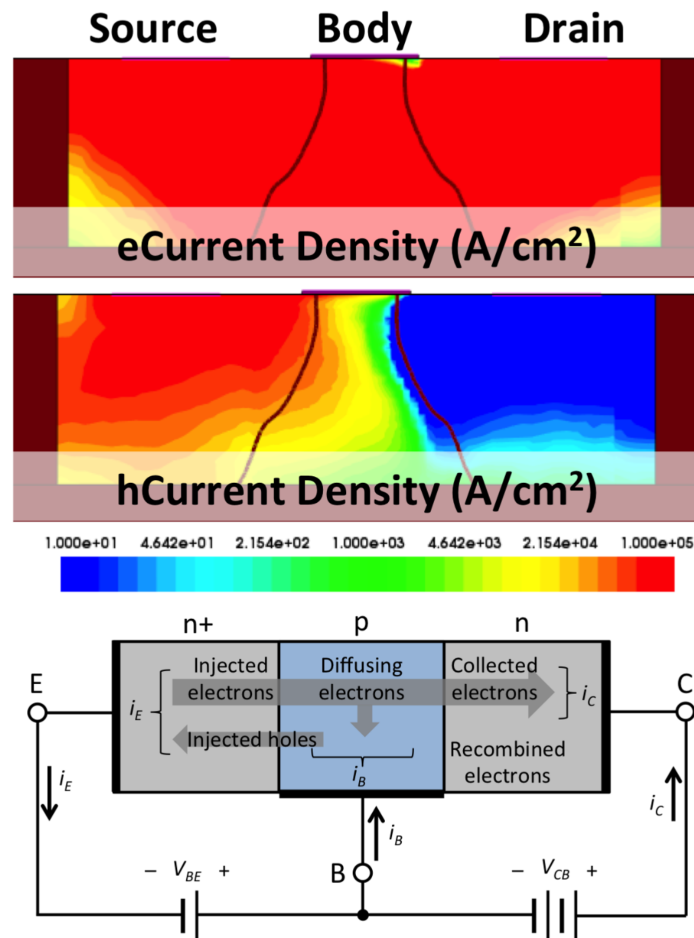

Figure 37: TCAD simulations highlight the parasitic BJT through electron and hole current densities. The carrier motion and SOI device construction is very similar to typical textbook drawings of carrier movement in basic BJT structures, after [67].

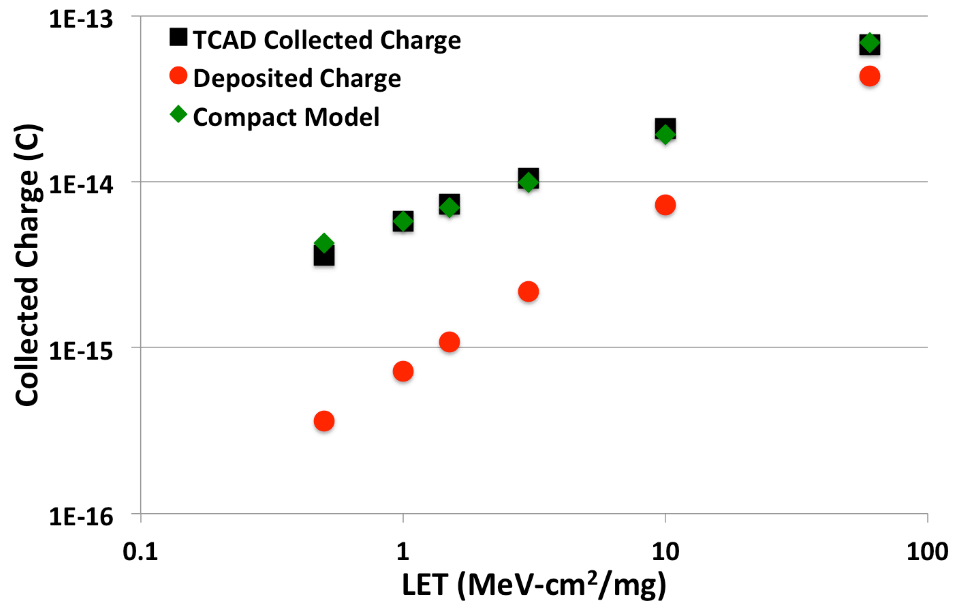

Figure 38: Single-event simulations were performed on an electrically calibrated 3D TCAD NMOSFET device, patterned after a standard SOI NMOSFET from the target technology, where the drain of the NMOSFET was hard biased to VDD, the gate and source were grounded, and the body was floating. TCAD simulations clearly show the amplification of collected charge, compared to deposited charge, where the deposited charge was calculated from the simulated LET and track length. The single-event enabled model compares well to the TCAD results.

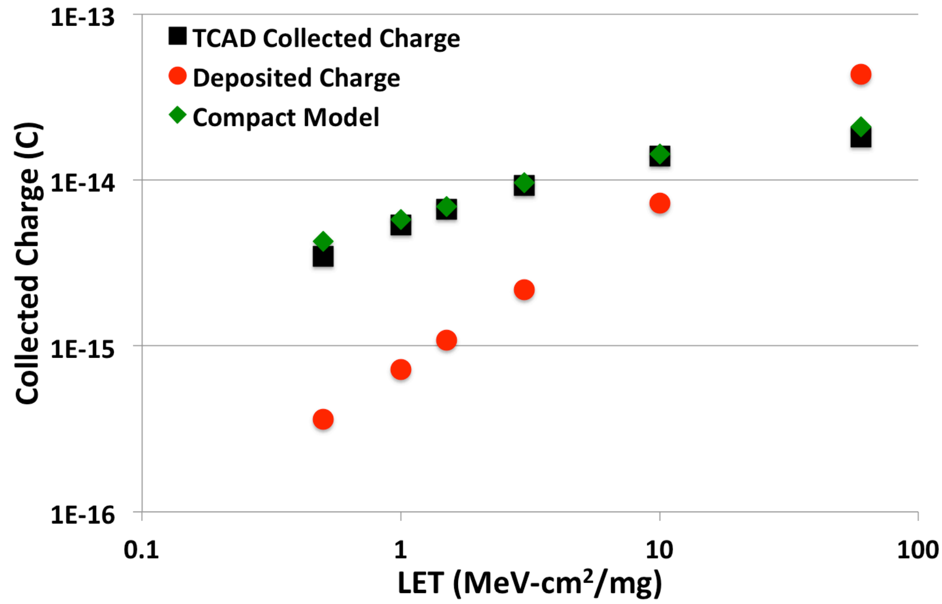

Figure 39: Single-event simulations were performed on an electrically calibrated 3D TCAD inverter with the input tied low, patterned after a 1X drive strength floating body inverter [68], [69]. TCAD simulations clearly show the amplification of collected charge, compared to deposited charge, where the deposited charge was calculated from the simulated LET and track length. The single-event enabled SOI compact model compares well to the TCAD results.

with the parasitic BJT compare well to 3D TCAD simulation results. Comparison of single-event enabled model pulse widths, 3D TCAD simulated pulse widths, and measured pulse-width data will be shown in the next section.

Validation with Heavy Ion Test Data

Heavy ion test data were obtained using the 10 MeV/amu cocktail at Lawrence Berkeley National Lab [70]. The test chips included multiple single-event transient targets, containing short inverter chains combined with an OR tree, and an on-chip single-event transient measurement circuit, as discussed in Appendix A and reported in [69] and [68]. The inverters in the chains were designed with PMOSFET and NMOSFET devices with width to length ratios for the 1X inverter of 214nm:32nm

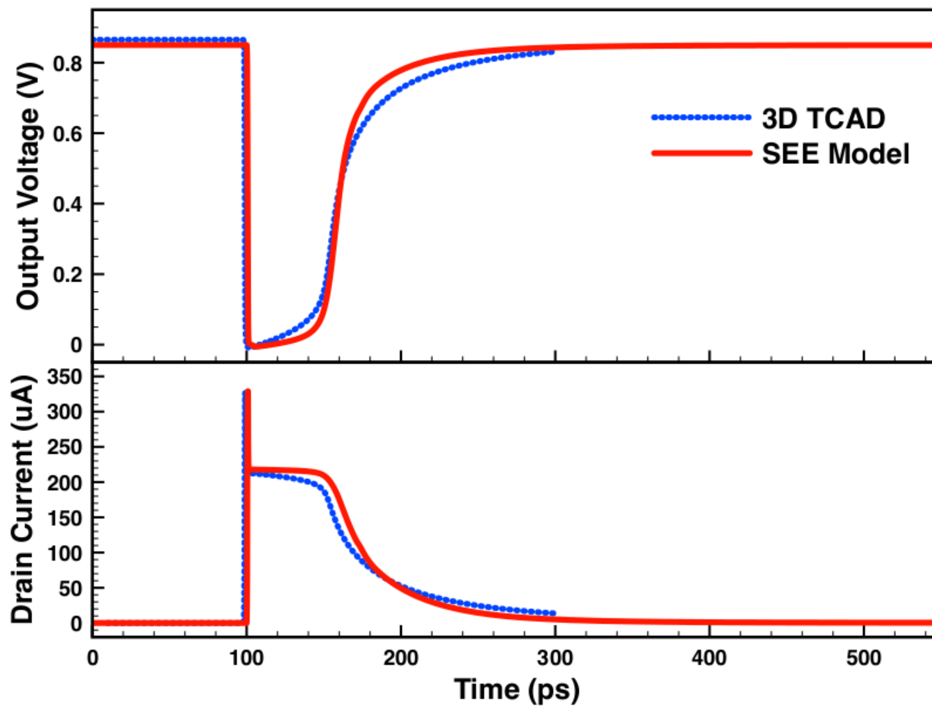

Figure 40: 3D TCAD and single-event model transient simulations show good agreement in current and voltage transient waveform shape and pulse width. The simulations were performed for a single-finger inverter at normal incidence with an LET of 60 $MeV - cm^2/mg$.

and 104nm:32nm, respectively. The larger inverters were designed as multiples of the 1X inverter, where the 3X inverter has a total PMOSFET and NMOSFET width of 642nm and 312nm, respectively. The 3X inverters had two design variants, where the straight design contained a single finger of the full width of the MOSFETs and the folded design contained three fingers of minimum width, as in the 1X inverter. Heavy ion irradiation was performed for multiple ions and energies, angles of incidence, and power supply voltages. Simulations of single-event transients using the compact model were performed to validate the model performance with the test data. The simulations included the short inverter chain, where an inverter in the middle of the chain was simulated as having been struck by an ion. The short chain was loaded with an OR gate, as found on the test chip, and the pulse width was measured as full-width half-rail at the input of the OR gate. Table 6 lists the species, energy, initial LET at normal incidence, and range in silicon for each of the ions utilized. Validation results are presented for normal incidence testing, angled incidence testing, and normal incidence testing over power supply variation.

Table 6: Ions Utilized in Heavy Ion Experiments (10 MeV/amu) [70]

Ion	Energy (MeV)	Initial LET ($MeV - cm^2/mg$)	Range (μm)
Ne	216.28	3.49	174.6
Si	291.77	6.09	141.7
Ar	400.00	9.74	130.1
V	508.27	14.59	113.4
Cu	659.19	21.17	108.0
Kr	906.45	30.23	113.1
Ag	1039.42	48.15	90.0
Xe	1232.55	58.78	90.0

Normal Incidence Validation

The single-event enabled model was validated for normal incidence behavior by comparing simulations to normal incidence experiments performed for multiple inverter based targets, utilizing the short chains and OR-tree combination circuits, with pulses being measured by the Vanderbilt University Autonomous Pulse Width Measurement Circuit [69], [68]. TCAD simulations were also performed using devices calibrated to the electrical performance of the nominal floating-body devices used in digital logic cells from the manufacturer's PDK, referred to as LowVT in this work, to validate the TCAD models. The single-event enabled compact model simulations using the LowVT devices compared well to the TCAD simulations and to the test data, which were obtained for the Cu and Xe ions. The compact model simulations using the HighVT devices, lower power devices from the PDK used in digital logic cells, also compared well to the test data for the HighVT target. Fig. 41 shows the compact model simulations results, TCAD simulations for the LowVT devices, and the normal incidence heavy ion test data over the full range of ion species from Table 6 and TCAD-based LET from 0.5 to 60 $MeV - cm^2/mg$. In Fig. 41, the simulated PMOSFET hits use open symbols, NMOSFET hits use closed symbols, the data symbols represent the average of the measured distribution and the error bars represent the maximum and minimum measured pulse widths, where the minimum measurable pulse width was 23 ps.

Angled Incidence Validation

The angled incidence behavior of the single-event enabled model was validated with angled ion-beam incidence experiments, using the Cu ion with a normal incidence

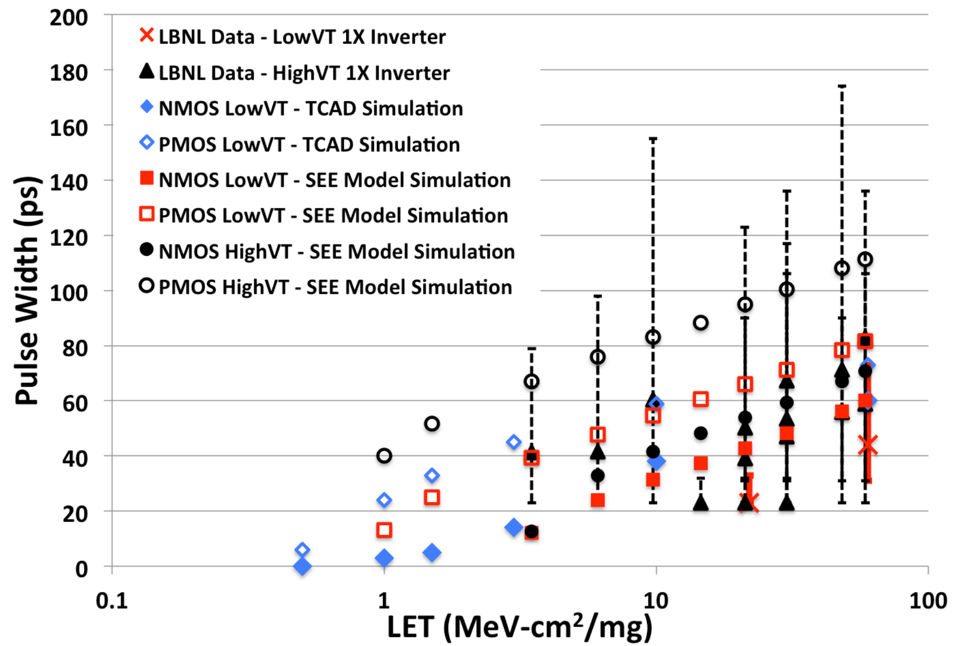

Figure 41: Compact model simulation results for LowVT and HighVT inverter NMOSFET and PMOSFET hits are compared to LowVT calibrated 3D TCAD simulations and LowVT and HighVT inverter chain heavy-ion data taken at LBNL. The error bars on the test data correspond to the maximum and minimum pulse-width measurements, and the data symbols are the distribution average.

LET of 21.17 $MeV - cm^2/mg$. The experiments were performed on two different LowVT inverter layout variations, with each inverter design having the same drive effective strength. The variations in the inverter layout were centered around the number of fingers utilized in each transistor. One variation had a single transistor gate for each MOSFET, or one finger. The one finger inverter had an NMOSFET width of three times the minimum for the technology, and the PMOSFET was sized such that the inverter output crossed mid-rail when the input crossed mid-rail. The second variation utilized devices with the same total width, however the MOSFETs were constructed with three fingers of transistor gates, each having a width of one-third the total MOSFET width of the single-finger design. This results in a MOSFET layout with a drain and source region on each end, shared drain between the one outer finger and the center finger, and a shared source between the other outer finger and the center finger. Irradiating with a roll angle of 0°aligned the ion beam to be parallel with the transistor gates, thus providing the longest potential ion track lengths in the body region of the device. The irradiations with a roll angle of 90°positioned the beam perpendicular to the gates. Fig. 42 shows a comparison of the angular test data for the single-fingered inverter target with tilt angles from 0°to 70°and a roll angle of 0°, or with the beam parallel to the transistor gate for the longest possible ion track length in the sensitive region. TCAD simulations for the 70°tilt angle are also shown in Fig. 42. Fig. 43 compares the angular test data for the three-fingered inverter target with tilt angles of 0°to 70°with a roll angle of 0°and tilt angles of 65°and 75°with a roll angle of 90°, where the beam is perpendicular to the transistor gate and the ion tracks can cross multiple MOSFET bodies. The results showed good agreement between the single-event model simulation for NMOSFET and PMOSFET

hits and the average measured pulse width from the data. The error bars in Figs. 42 and 43 represent the maximum and minimum measured pulse widths in the test data.

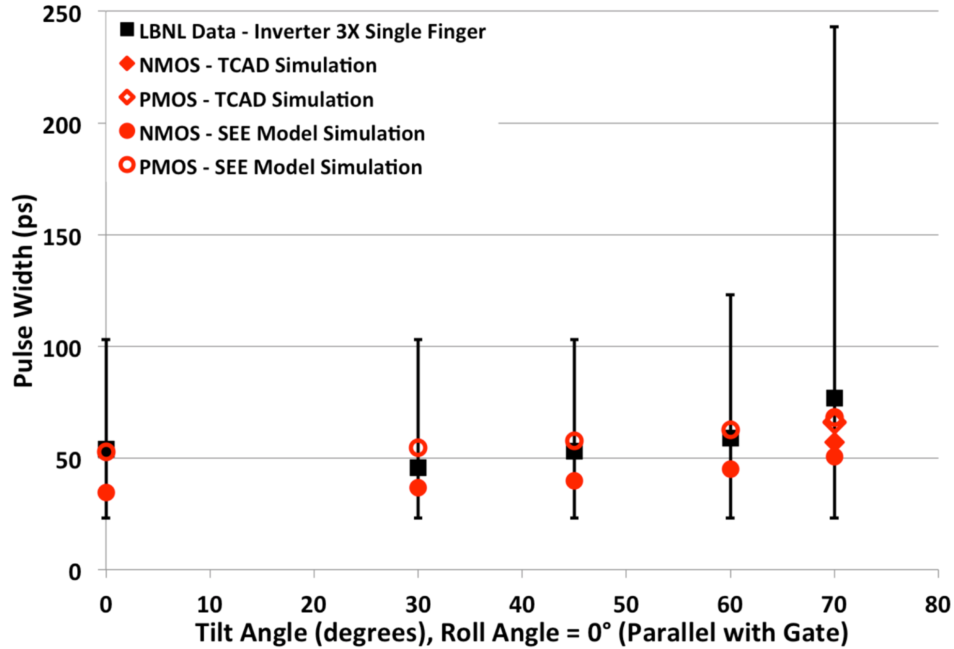

Figure 42: The single-event model simulations for single-finger inverter chains with NMOSFET and PMOSFET hits, closed and open symbols respectively, are compared to angled incidence test data with a roll angle of 0°, where the ion beam is parallel to the gate. The simulation results show good agreement with the test data, where the symbols represent the average pulse width and the bars represent the maximum and minimum measured pulse widths. The irradiations were done using Cu ions with a normal incidence LET of 21.17 $MeV - cm^2/mg$.

Bias Variation Validation

The single-event enabled model behavior was validated over bias voltage with heavy-ion experiments where the target supply voltage was varied from 0.7 V to 1.0 V. Irradiations were performed with Kr ions, which have a normal incidence LET of 30.23 $MeV - cm^2/mg$. Fig. 44 compares the single-event enabled model simulations of NMOSFET and PMOSFET hits to the HighVT inverters at multiple supply voltages

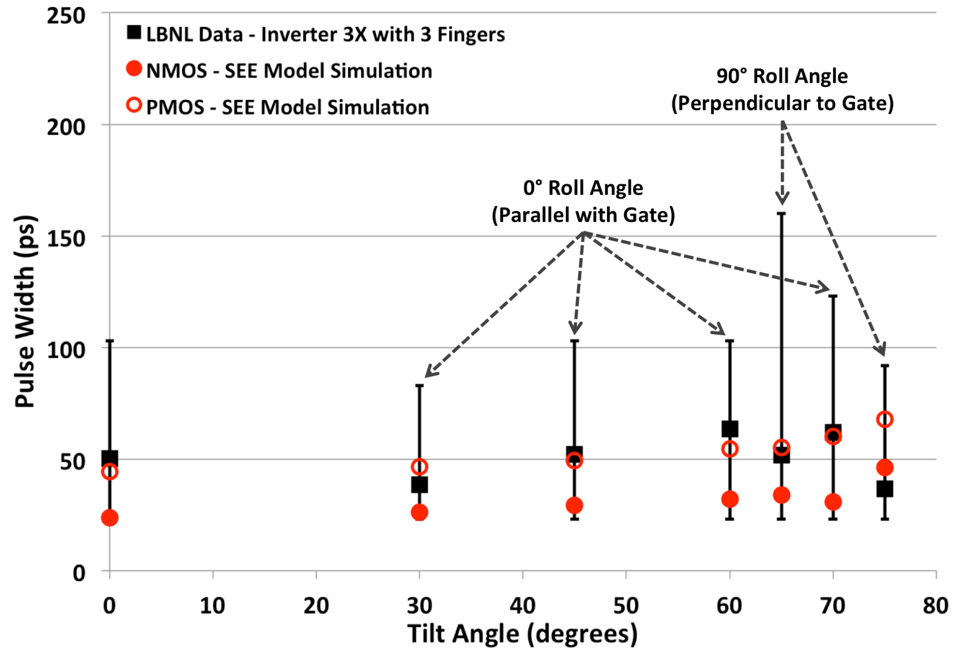

Figure 43: The single-event model simulations for three-finger inverter chains with NMOSFET and PMOSFET hits, closed and open symbols respectively, are compared to angled incidence test data with a roll angles of 0°or 90°, where the ion beam is parallel or perpendicular to the gate, respectively. The simulations results show good agreement with the test data, where the symbols represent the average pulse width and the bars represent the maximum and minimum measured pulse widths. The irradiations were done using Cu ions with a normal incidence LET of 21.17 $MeV - cm^2/mg$.

with the heavy-ion test data. The simulations and test data show good agreement. As expected the average pulse widths and the maximum pulse widths increased with reduced supply voltage due to the reduction in restoring drive current.

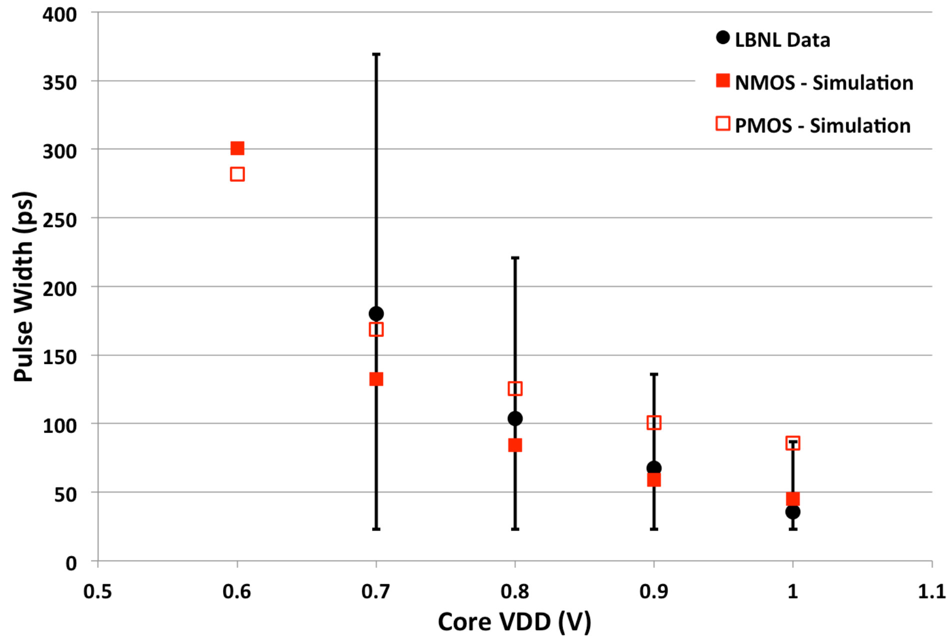

Figure 44: Single-event enabled model simulations for the HighVT inverter over supply voltage variation compare well to the heavy-ion test data. Simulated NMOSFET hit pulse widths are shown in closed symbols and simulated PMOSFET hits are shown with open symbols. The data points show the average measured pulse width and the bars represent the maximum and minimum measured pulse widths in the data set. Irradiations were performed at normal incidence with Kr ions, which have a normal incidence LET of 30.23 $MeV - cm^2/mg$.

Conclusions

The bias-dependent radiation-induced transient current modeling methods described in Chapter III have been implemented in single-event enabled models for bulk CMOS technologies. The models include the primary bias-dependent current at the device junctions and the n-well junction in PMOSFET devices as well as methods for modeling the modulation of the local well and substrate potentials as a result of the

transient currents. Parameterization of the models to capture charge sharing effects is possible with TCAD calibrated lookup tables that include the collected charge and time constants as a function of LET and distance from the device.

A single-event enabled Mextram HBT compact model that is capable of capturing bias-dependent charge collection behaviors in the simulation of SiGe HBT circuits has been developed. The application of the bias-dependent modeling techniques to the SiGe HBT Mextram models shows the cross-technology use and relevance the bias-dependent methods presented in Chapter III. The model was calibrated to 3-D TCAD simulations and exercised in a circuit simulation. The simulation of charge sharing effects is possible using lookup table parameters. Comparing the results of the bias-dependent single-event model to those obtained using the independent double-exponential method, it is clear that bias-dependent behaviors and charge sharing must be captured to obtain reasonably predictive simulations in agreement with measured data.

A new geometry-aware single-event enabled modeling methodology has been developed for bulk CMOS and partially depleted SOI CMOS devices. The SOI model is built upon a fundamental topology that has been employed for decades in the Kerns and Massengill model. The physical reality of a parasitic lateral BJT in SOI MOSFETs remains. However, the model utilizes single-event modeling enhancements for advanced technology modeling, such as the bias-dependent single-event current generation source and the use of behavioral modeling languages. Additionally this model departs from the traditional use of a full SPICE BJT device to model the parasitic BJT. Rather, a behaviorally modeled implementation of the SPICE Gummel Poon equations has been developed for collector current, including high injection

effects, and a diode model to restore floating body potential after a single-event. This behaviorally modeled parasitic BJT improves on the traditional methods with a lower simulation overhead and straightforward BJT model parameterization using technology and design parameters while maintaining the MOSFET drain/source symmetry that is not preserved when placing a standard SPICE BJT device in parallel with the MOSFET.

The layout-aware compact models for single-event simulation of devices and circuits are utilized in a novel circuit simulation and analysis capability that is detailed in Chapter VI.

CHAPTER VI

LAYOUT-AWARE CIRCUIT ANALYSIS

A layout-aware analysis method has been developed to utilize a novel hybrid of single-event-enabled compact models (for efficiency) and spatially-aware layout objects (for geometric charge collection accuracy) in an industry standard integrated circuit (IC) design tool flow. Simulations of single-event strikes at multiple locations, with full circuit layout coverage, can be completed in less than an hour using a single-processor desktop workstation. Using this method, a full layout can be analyzed in about the same amount of time required for a single, simple analysis using the fastest TCAD programs. This method sacrifices some of the physics-based fidelity of full 3-D TCAD analysis, however the simulations are many orders of magnitude faster than full 3-D TCAD and can be run by a typical IC designer using their standard design tools. TCAD simulations are still used in calibration to determine the charge transport characteristics for the target technology. Additionally, the use of industry standard commercial design tools provides a path for integration of this analysis method into a single-event hardened IC design flow.

Using this method, single-event simulations can be performed with strikes at arbitrary locations in the circuit layout, with each affected device having a calibrated response to the event. This simulation method includes the automated extraction of layout features and dimensions, the setup of a strike location mesh over the layout, dynamic netlist generation and simulation control, and a routine to calculate the single-event sensitive-area of the circuit. The bias-dependent model is utilized to

inject the single-event currents into the devices proximal to the strike location [27]. The layout-aware simulations are performed using an industry standard circuit-level simulator.

The analysis method has been successfully demonstrated on multiple flip-flop designs in 28nm and 40nm bulk CMOS technologies and on an operational amplifier in a 180nm bulk CMOS technology. The single-event sensitive areas for the designs are mapped by simulating normal incidence single-event hits over multiple locations in the design and over a range of linear energy transfer (LET) values. Simulation results and calculated sensitive areas compare well to test data.

Traditional Analysis Methods

TCAD Simulation Analysis

TCAD provides an accurate, physics-based simulation capability. However, the simulation of circuits in full 3-D TCAD is often difficult to setup and simulations can run for multiple days. The Accuro 3-D TCAD simulator from Robust Chip has demonstrated capability to simulate large circuits faster than full 3-D TCAD, by two orders of magnitude [71], [72], [73], [74]. The Accuro approach of coupling the high accuracy 3-D TCAD simulation of the charge transport and collection in the substrate with circuit-level simulation models of the devices provides a significant simulation speed increase with minimal sacrifice of physical accuracy when compared to full 3-D TCAD. Flip-flop simulations utilizing Accuro have shown good agreement with test data [71]. However, this approach is still orders of magnitude slower than circuit-level simulation.

Sensitive Node and Node Pairs

Circuit-level simulations to determine single-event upset susceptibility are often performed by injecting charge into a potentially vulnerable node using a current source, either a Technology CAD (TCAD) calibrated double-exponential or a bias-dependent single-event model [27], [75]. To account for multiple-transistor charge collection, single-event current sources are placed on all possible node-pair combinations in the circuit, with each pair being exercised in successive simulations [31], [75], [76]. This analysis method is useful for determining sensitive circuit nodes and node combinations, however a direct relationship cannot be easily drawn between the simulation analysis and the total sensitive-area as layout and hit location are typically not taken into consideration.

Distance Parameterized Lookup Table

Francis, et al. demonstrated a method that parameterized the injected charge for multiple instances of a bias-dependent single-event model using a look-up table based on the distance between two devices [27], [76]. This method provides a means of correlating charge injected on a device with the distance between the device and the primary struck device. However, this simulation method did not account for modifications to the timing parameters of the model, nor did it provide a means of calculating model parameters for arbitrary strike locations within or near a device. Simulations of an inverter chain utilizing the bias-dependent single-event models and a lookup table were also demonstrated in Chapter V.

Layout-Aware Analysis Methodology

The layout-aware analysis methodology utilizes integrated circuit design, simulation, and verification tools, as well as a series of automation scripts, to extract physical design information and couple that information with a circuit simulation netlist. The physical design information provides inputs to parameterization functions that calculate the single-event charge collection response of a device in the design as a function of distance from the simulated strike location. The parameterization functions are extracted from 2-D TCAD simulation results, where reverse biased diffusions are placed at multiple distances from the simulated strike in the TCAD simulation. The TCAD simulations solve the carrier generation and transport equations, and the results are combined into functions to parameterize the single-event models presented in Chapter V.

TCAD-Based Compact Model Calibration

2-D TCAD simulations are used to generate a set of data to describe the charge transport characteristics of the technology. By using TCAD to calibrate the characteristic charge transport for the technology rather than a specific circuit, TCAD calibration must be performed only once for the technology. The 2-D TCAD simulations include charge transport over distance within a well and across the nwell/pwell boundary. Fig. 45 shows a close-up of the nwell/p substrate junction and some of the n+ and p+ diffusions used to approximate drains and sources in the technology. The 2-D TCAD structure used for calibration in this work contains substrate and well doping profiles calibrated to spreading resistance measurements from the technology of interest, and drain/source doping profiles typical to the

technology node [77]. Single-event simulations are performed on this TCAD structure with the position of the simulated strike being varied across the region of interest in the structure, -2m to 2m, and the LET being varied from 0.6 to 100 MeV-cm2/mg. All single-event simulations were performed at normal incidence. A total of 120 2-D TCAD calibration simulations were performed. The time required for the TCAD simulations was approximately 3 hours per simulation utilizing only a single processor. These TCAD simulations were used to characterize the charge transport characteristics for the technologies of interest for the circuits presented in the Simulation and Test Results section.

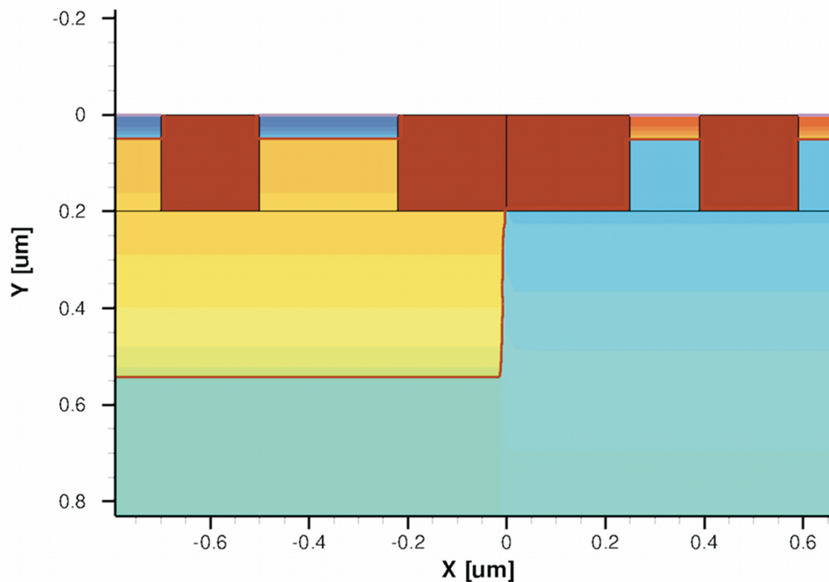

Figure 45: Part of the 2-D TCAD calibration structure used to generate the data for strike vs. distance and LET empirical functions and parameterization of the single-event enabled compact model. The structure includes a p-type substrate and an nwell to capture cross-well charge movement for inclusion in the calibration data.

The TCAD generated data set is used to develop a set of empirical functions that describe the single-event response of the technology. The transient characteristics from the TCAD simulations are extracted from the time-current waveforms from each

of the diffusion and well contacts. Each of these characteristic responses: collected charge, rising edge time constant (τ_R), pulse width, falling edge time constant (τ_F), and pulse rising edge delay, are associated with a specific distance from the strike and LET of the incident particle. The resulting empirical functions are used to parameterize the single-event compact model to fit the characteristic response data sets over distance from the strike.

Modulation of the charge transport characteristics, as a function of LET, is also included in the empirical functions. These empirical functions are used to calculate the timing and charge injection parameters of the single-event model presented in Chapter V. Fig. 46 shows the 2-D TCAD results for collected charge as a function of distance from the strike and LET, as well as the derived empirically fit function evaluated over distance and LET. The empirically fit functions in Fig. 46 trend toward worst case collected charge. A bias toward higher collected charge in this analysis will provide the designer with a conservative picture of how the design may respond to a single-event strike.

Single-Event Model Description

In circuit-level simulation, the single-event model follows the structure and methods described in Chapter V and shown in Fig. 21. The models can be used in any circuit simulator capable of using the Verilog-A behavioral modeling language [40]. The Cadence Spectre circuit simulation tool was utilized in this research, but the analysis framework is flexible and easily modified to accommodate other industry standard simulation tools [62]. The single-event model is given the distance to the strike location and the LET of the simulated strike. Using the empirical functions

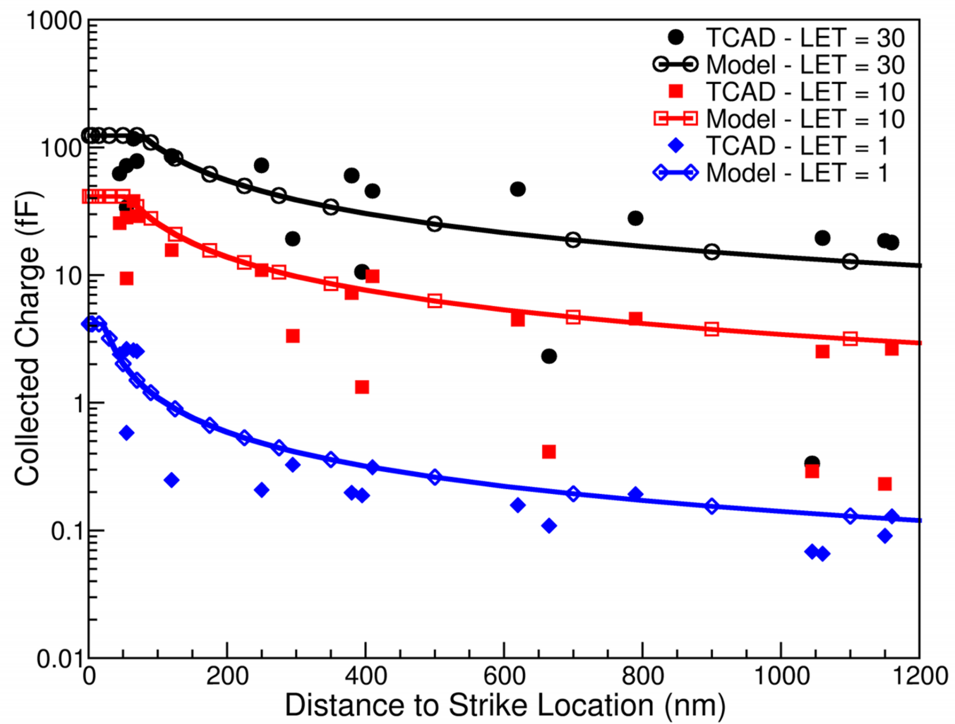

Figure 46: 2-D TCAD calibration results for collected charge as a function of distance from strike and incident particle LET. The empirically fit function, included in the model is evaluated over distance at each LET [54].

derived from the TCAD calibration, the model determines the pulse start time, rise and fall times, and the collected charge at the proximal device. Table 7 shows the form of the parameterization functions used to calculate the compact model parameters for each device in the region of multiple device charge collection.

Table 7: Empirical function forms, derived from TCAD calibration data, utilize distance from the strike and simulated LET. The functions either scale the initial characteristic value, as in the case of Charge, or they add a delay to the characteristic value, as in the case of τ_R.

Parameter	Parameterization Function Form	Definition
Charge	$Charge_0 \times f_{CHARGE}(distance, LET)$	Total Charge Deposited
τ_R	$\tau_{R0} + f_{TAUR}(distance, LET)$	Rising Time Constant
τ_F	$\tau_{F0} + f_{TAUF}(distance, LET)$	Falling Time Constant
$Start_{Time}$	$T_0 + f_{DELAY}(distance, LET)$	Transient Start Time

$Charge_0 \approx 1.035 \times 10^{-2} pC/\mu m \times LET \times Col.Depth(\mu m)$

Layout Feature Extraction

Developing the capability to perform a layout-aware simulation analysis requires detailed information about the circuit layout; including device and well boundaries. An automated process for extracting positional and boundary information for every device and well in the layout has been developed. The positional information is automatically extracted from the results of an industry standard layout verification software package using custom developed scripts for layout feature extraction, strike location mesh generation, and simulation netlist creation [78].

The automation scripts that control the information processing utilize the correspondence data contained in layout vs. schematic (LVS) results for the design being analyzed and some basic technology information, e.g. active to poly overlap, poly-to-poly pitch, etc. The correspondence data maps the physical location of a transistor

within a design and the transistor instance in the schematic generated netlist. Once all of the transistors are located, the scripts determine which devices share diffusions as well as the orientation of the source and drain within the design.

The device information from the layout is connected to the circuit-level netlist, via the custom netlist generation scripts, and is used in the parameterization of the compact model, which provides a positional awareness within the circuit-level simulation. Fig. 47 demonstrates three transistors in a layout and highlights the extracted boundary information for the drain and source terminals of the MOSFETs. The layout feature extraction techniques developed for this analysis automatically determine transistor position, drain and source boundaries, and drain and source orientation.

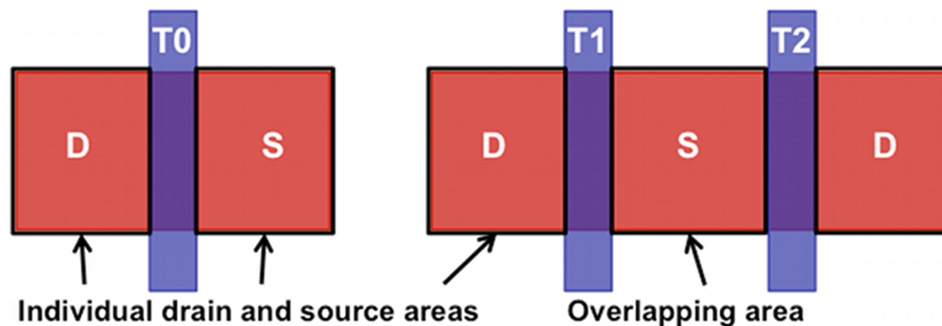

Figure 47: Three transistors, T0-T2, with the calculated boundaries of the drain and source terminals outlined. The boundaries and device position are used during netlist generation and distance to strike parameterization of the compact model [54].

Strike Location Mesh

Many of the traditional circuit-level simulation techniques for performing a single-event analysis approximate only strikes directly on a terminal of the device. The layout-aware simulation method accounts for strike locations inside and outside of

devices by generating a mesh of strike locations over the entire circuit layout. The distance between the location of the strike and the position of the device is a parameter used in the empirical functions derived from the 2-D TCAD calibration process.

The strike mesh determines the locations for the simulated single-event strikes over the layout. Fig. 48 shows the strike location mesh overlaid on a single device with a strike occurring in a mesh location outside of the drain. The charge collection

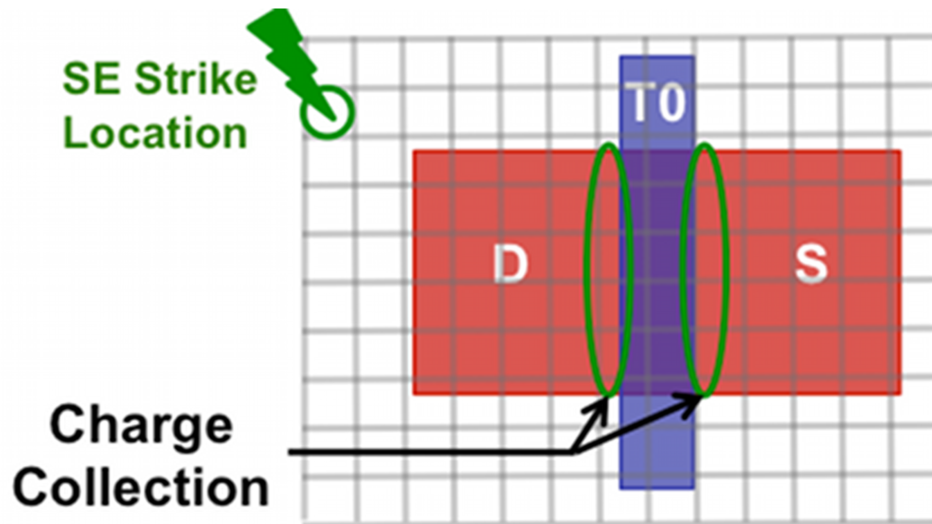

Figure 48: A mesh of strike locations is generated over the circuit layout. The compact model is parameterized using the distance from the strike mesh location to the proximal device [54].

markers in Fig. 48 are indicators of the region used to calculate distance of the drain and source from the strike. Fig. 49 shows TCAD generated single-event currents collected at the drain and source terminals for a strike 70 nm outside of a device drain. The TCAD current profiles, like those shown in Fig. 49, are the basis of the calibration data set used to generate the empirical functions for the compact model parameterization. As detailed in Chapters III and V, the bias-dependent single-event model used in this analysis has been shown to provide good agreement and handling

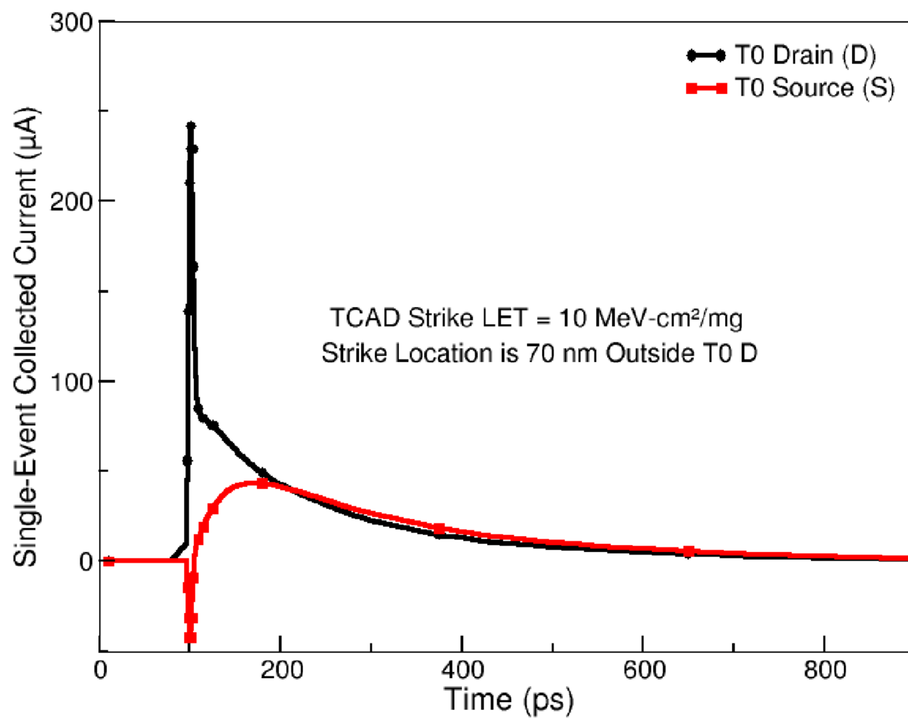

Figure 49: TCAD generated single-event currents on device T0 from Fig. 48 for a strike 70 nm outside of the drain region of T0. TCAD generated waveforms, like these, are used to develop the TCAD derived empirical functions for compact model parameterization [54].

of the junction bias perturbations that impact the current waveform [27].

The size of the strike mesh geometry has an impact on the resolution of the analysis (minimum sensitive-area unit) and the overall number of simulations to be performed. A small mesh with a minimum sensitive area unit on the order of $5 \times 10^{12} cm^2$ will have good resolution, but a very high simulation count, greater than 15,000 per simulated LET. Likewise, a large mesh will result in a large minimum sensitive-area unit, but a reduced number of simulations. When selecting a mesh size, the low LET sensitivity needs to be considered, because the collected charge at low LETs falls off rapidly with distance, as shown in Fig. 46. A large strike mesh size could impede the observation of measurable responses at low LETs due to the fact that a large mesh geometry could result in strike simulations occurring at a distance from the device collection region that is longer than the distance of peak collection at low LET.

Layout-Aware Simulation

Circuit-level simulation netlists are dynamically generated for each strike mesh location, including the single-event-enabled compact model parameterization of each of the proximal devices. Only the devices within the region of multiple device charge collection susceptibility are parameterized, thus reducing the overall number of single-event-enabled models included in each simulation. Netlists for strikes within the nwell, or near the nwell/pwell boundary, also include a single-event current source to model the nwell to pwell/p-substrate current. Well resistances are included between the nwell and pwell/p-substrate nodes and the supply voltage sources to allow for well voltage perturbation as a result of the single-event strike. The dynamic generation of individual netlists provides traceability between simulation results and specific strike

location.

The strike location in (X,Y) coordinates is saved by setting the DC value of a voltage source, VX and VY within the netlist, and extracting that voltage to the output file. Those source values are set by the automatic netlist generation scripts. The LET value for the simulation is also extracted in a similar manner, however multiple LET values are swept for each single point, therefore LET is a swept parameter in the simulation. The output signal is measured using in-line OCEAN commands in Spectre, which is possible when using MonteCarlo simulation methods [62]. The MonteCarlo simulation is set to run the nominal case only, and it sweeps through a list of values for the LET. Using the parametric sweep of LET allows for simulations of many LET values, while only going through the license check and program start-up once for each location. The circuit simulation times, in the case of flip-flops and even operational amplifiers, are often less that the time needed to check the license on the server, initialize the simulator, and run the dc operating point. Because the simulation at each location effectively runs many simulation cases with a single simulator startup time, a significant time savings is gained.

As a benchmark of overall layout-aware analysis simulation time, approximately 18,000 strike mesh locations were generated in a typical flip-flop design: that is 18,000 simulations for each desired LET to be included in the analysis. The extraction of the layout features and generation of the netlists for the 18,000 strike mesh locations was performed using the automation scripts. It takes approximately 5 minutes to generate the simulation files and directory structure for simulation data management. Using an industry-standard simulation tool on a single-processor desktop workstation, these 18,000 simulations took approximately 45 minutes for all strike locations at one LET

value. In the case of flip-flop simulations, 10-12 LET values are often simulated, increasing the total simulation time to 3-3.5 hours, which is a significant time savings over the 7.5-9 hours that would be required to run each LET as a separate simulation rather than a parametric sweep.

Results Generation

The simulation output for a flip-flop analysis is a simple binary output to denote an upset, 1, or no upset, 0, in the flip-flop output value. Output values can also be extracted for maximum perturbation from nominal, full-width half max pulse width of the transient, and even error energy in the output signal [79]. The output value is generated using a waveform feature extraction method included in the simulation netlist as part of the simulation commands section. Most industry standard simulation tools have an extract or measure syntax capable of measuring the desired characteristics of the output signal.

A similar output could be obtained through a post-processing of the waveform output files as an additional step in the automation. The use of the built-in waveform feature extraction is more efficient because it does not require the simulator to write the waveform output file to the disk, resulting in a reduction in total simulation time. For every strike mesh location, the strike LET and simulation output value are stored in a single file. The circuit response to a specific strike location over LET can be easily extracted from these stored results. Additionally, all of these files are automatically collected to create a response file that characterizes the whole circuit. In addition to the simulated LET and the output result, the strike location associated with each entry in the file is included. Automation scripts have been developed for

post-processing the data. The scripts produce a single-event sensitive area file, for import into a plotting program, and a heat-map image that can be overlaid on an image of the layout. Post-processing of the full data set, including multiple LET values requires about 5 minutes using the automation scripts.

The single-event-upset sensitive area for each LET is calculated for comparison to test data, and the specific sensitive strike mesh locations at each LET are used to generate a heat-map to overlay on the layout image. The total sensitive area at each LET is calculated by summing the number of mesh locations that resulted in an upset. If an upset or measurable response occurs as a result of a strike at a mesh location, the sensitive area for each LET resulting in a measured response is increased by the minimum sensitive-area unit, which is a function of the mesh resolution. Similarly, the heat-map is generated by coloring the strike location mesh with the heat color that corresponds to the lowest LET resulting in an upset. Fig. 50 shows a heat-map overlay on a subset of devices from a flip-flop layout. The sensitive area vs. LET plot provides a metric for determining single-event-upset hardness and latch-to-latch comparison. The heat-map provides visual guidance to designers as layout hardening decisions are being made. The heat-map relates sensitive regions at each LET directly to the device positions on the layout.

Simulation and Test Results

The layout-aware simulation method has been exercised with multiple flip-flops designed in a 40nm and 28nm bulk CMOS processes, as well as an operational amplifier designed in a 180nm bulk CMOS process.

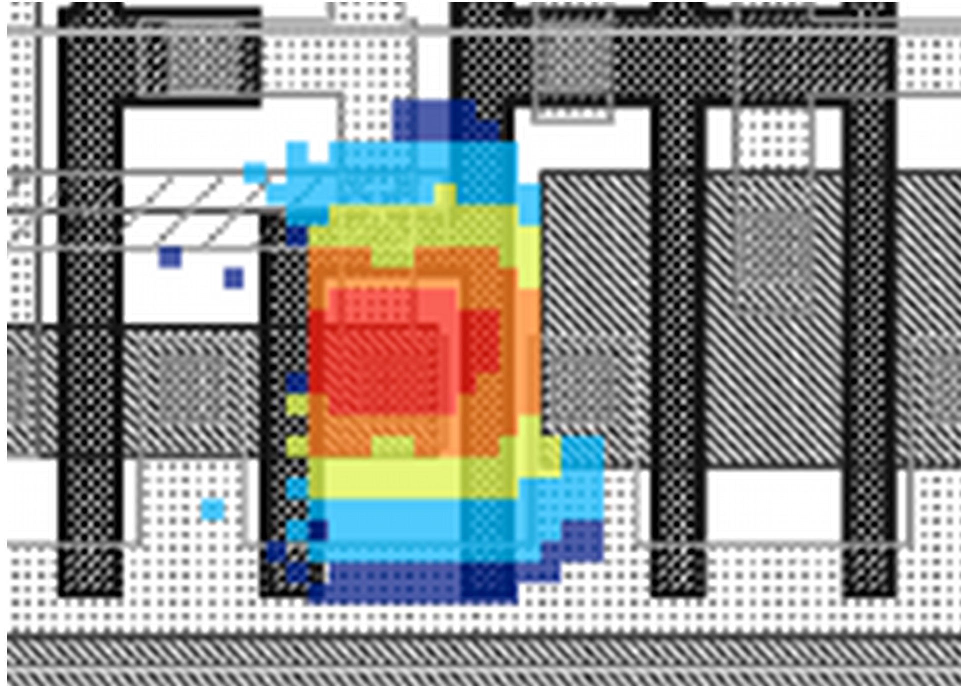

Figure 50: An example heat-map superimposed on a few devices in a flip-flop layout [54].

Flip-Flop Analysis Results

The analysis method is exercised on rising-edge triggered master-slave D-flip-flop variants. In the circuit simulation analysis, the flip-flop input was held at a fixed logic state, high or low, and the flip-flop was setup to have a latched logic state at the output. This simulation setup mirrored the heavy-ion test conditions used for verification of the simulation method, where a blanket pattern input was utilized. The flip-flops were also simulated for the clock low and clock high states. The results presented here are only for the clock low state, as there was little difference in the simulated overall sensitive area of these master-slave flip-flops for the clock low vs. clock high states. This also accounts for the heat-maps showing a majority of the sensitive area only in the slave latch.

40nm Flip-Flops

The 40nm flip-flop variants were fabricated in a commercially available 40nm bulk CMOS technology and heavy-ion tested at the Brookhaven National Laboratory Tandem Van de Graaff with ions from boron to nickel for an LET range of approximately 1 to 26.5 $MeV-cm^2/mg$ at normal incidence [80]. The flip-flops were tested to a fluence of $1 \times 10^8 ions/cm^2$. The test structures were designed in CREST shift-register fashion and included 8,056 flip-flops, with many flip-flop variants being tested [81]. A high logic state was held constant at the input of the shift register and high states were subsequently shifted through the chain during test.

A comparison of the layout-aware analysis and heavy-ion test results from two flip-flops, FFA and FFB, showed good agreement. Fig. 51 shows the heat-map overlay on the layout of FFA for a simulated LET of 0.6 to 28 $MeV-cm^2/mg$, and Fig. 52 shows the heat-map image for FFB over the same LET range. The heat-map provides designers with visual feedback of sensitive devices and regions within the layout of the circuit. A designer may know the most sensitive devices within the circuit; however, the heat-map also shows the areas outside of the transistor active regions that can contribute to the overall upset susceptibility of the circuit. If the sensitive area estimation was made using only the active area of the known sensitive devices, the overall sensitive area of the circuit would be underestimated. Additionally, a circuit designer can use the visual information contained within the heat-map to make more informed device spacing decisions, to reduce the susceptibility of circuit upset as a result of multiple device charge collection.

The simulated sensitive area at each LET was calculated from the layout-aware analysis of FFA and FFB by summing the area of the mesh grid locations resulting

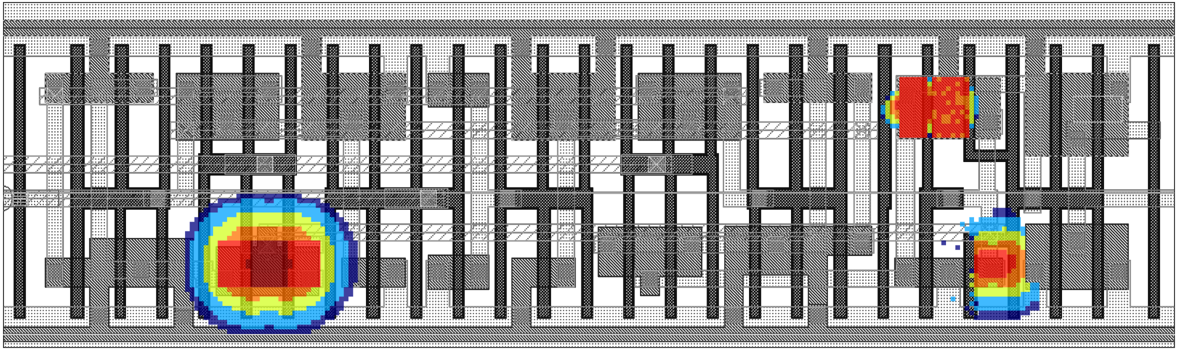

Figure 51: Layout-aware single-event analysis generated sensitive-area heat-map overlay on the layout of FFA [54].

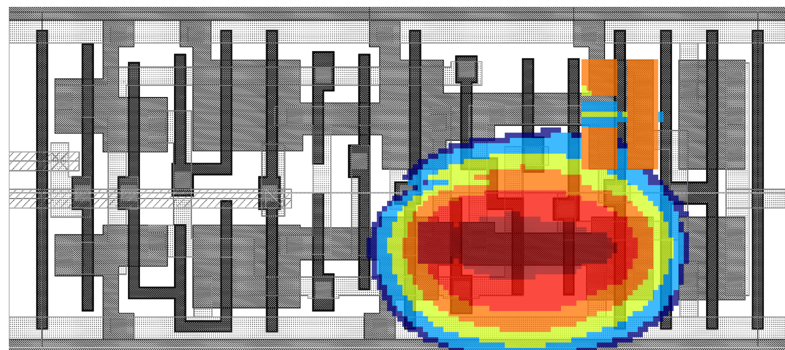

Figure 52: Sensitive-area heat-map overlay on the layout of FFB [54].

in an upset. The sensitive area was calculated for each LET simulated in the layout-aware analysis. The sensitive areas for the FFA and FFB shift registers from the heavy-ion testing were calculated by dividing the number of flip-flop errors by the fluence, $1x10^8$ ions/cm^2. Dividing the sensitive area of the shift register by the total number of flip-flops in the shift register, 8,056 flip-flops, provides a good approximation of sensitive area for a single flip-flop. Fig. 53 shows the comparison of the layout-aware analysis calculated sensitive area compared to the measured sensitive area for FFA (a) and FFB (b). The simulation results and heavy-ion test data show simulated and measured values well within a factor of 2x over the range of LET values, with the layout-aware simulation method showing a slightly higher overall sensitive area.

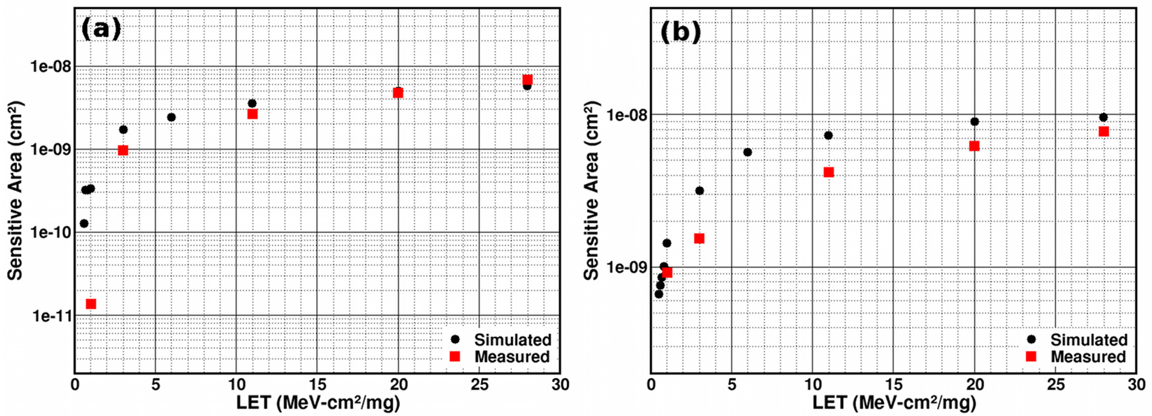

Figure 53: Comparison of the layout-aware analysis generated single-event sensitive areas of flip-flops FFA (a) and FFB (b) and the broadbeam heavy-ion data collected on shift registers of 8,056 flip-flops. Heavy-ion data was collected at the Brookhaven National Laboratory Tandem Van de Graaff with ions from boron to nickel at normal incidence [54].

The layout-aware single-event analysis provides two very useful elements of feedback for circuit designers and for those making decisions about which specific design variants should be used in a system. A circuit designer can use the heat-map

images to determine the location and severity of the sensitive regions in the circuit. For example, the heat-map of FFA in Fig. 51 tells the circuit designer that the most sensitive region of the circuit is the transistor on the left side of the design. The inner region of that portion of the heat-map corresponds to an LET of 0.6 MeV-cm^2/mg. The other regions of the circuit do not upset until about an LET of 1 MeV-cm^2/mg. Additionally, the designer can see that the grounded source regions to the left and right of the NMOSFET transistor on the bottom right bound the sensitive region around the device. In contrast to the NMOSFET device, the PMOSFET device above it shows fairly low LET sensitivity in both the drain and the source region, however that sensitivity does not appear to extend significantly outside of the device. Knowing these specific locations and details about the sensitive regions will allow a designer to make intelligent hardening and device spacing decisions. In the case of the sensitive device acting as a pass-transistor at the left of FFA in Fig. 51, the designer may choose to make a topological modification to the flip-flop design. The total sensitive-area vs. LET plots in Fig. 53 can provide a system designer with a means of comparing multiple similar designs to determine which should be used in the system.

28nm Flip-Flops

A test chip containing multiple flip-flop designs was designed and fabricated in a commercially available 28nm technology. The flip-flops were placed in a shift-register of 8,056 flip-flops with a CREST style upset detection scheme [81]. Over 40 flip-flops were characterized using the layout-aware analysis methods. A baseline DFF design, patterned after the 40nm design shown in Fig. 52 was tested and compared to the

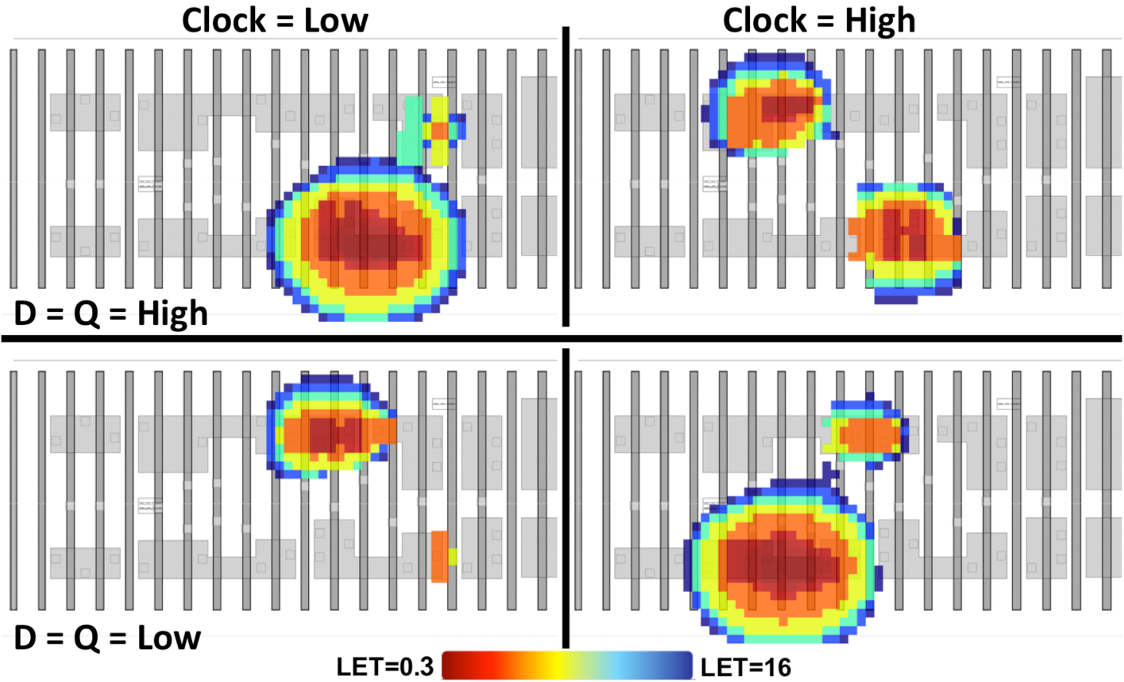

Figure 54: Sensitive-area heat-map overlay on the baseline 28nm DFF.

layout-aware results. Figs. 54 and 55 show the layout-aware analysis generated heat map for all four clock and data input combinations and the sensitive area of the flip-flop over different LET values.

Narasimham utilized the layout-aware analysis capability to compare a hardened flip-flop design and a baseline DFF design in 28nm [82]. The flip-flops were master-slave designs, and the master and slave latch schematic for the baseline and hardened designs are shown in Fig. 56. The normalized sensitive areas for each of the flip-flop designs, calculated by the layout-aware analysis method and experimentally measured, are shown in Figs. 57 and 58. The layout-aware analysis calculated sensitive area and the measured sensitive area show good agreement.

As discussed previously, charge sharing in advanced technologies can negatively impact methods utilized to harden circuits to single-event upset. A layout-aware

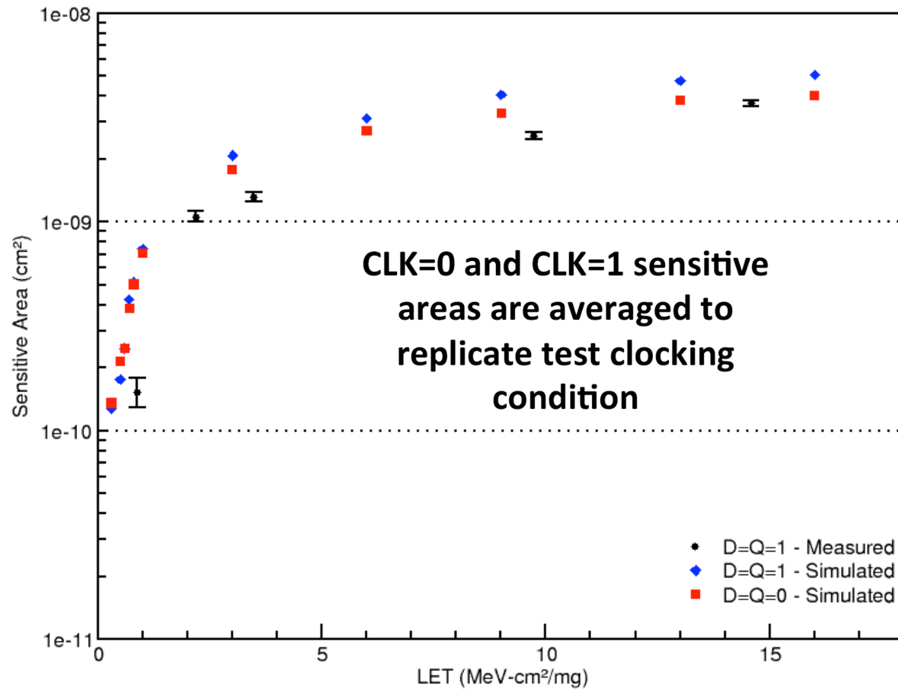

Figure 55: Comparison of the layout-aware analysis generated single-event sensitive areas of the baseline 28nm flip-flop design and heavy-ion test data.

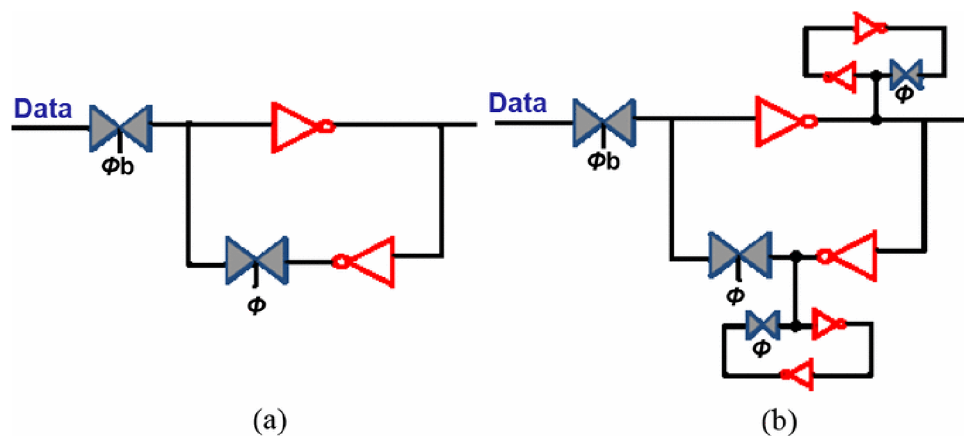

Figure 56: Schematics of the baseline and hardened latch designs utilized in the baseline and hardened master slave flip-flops [82].

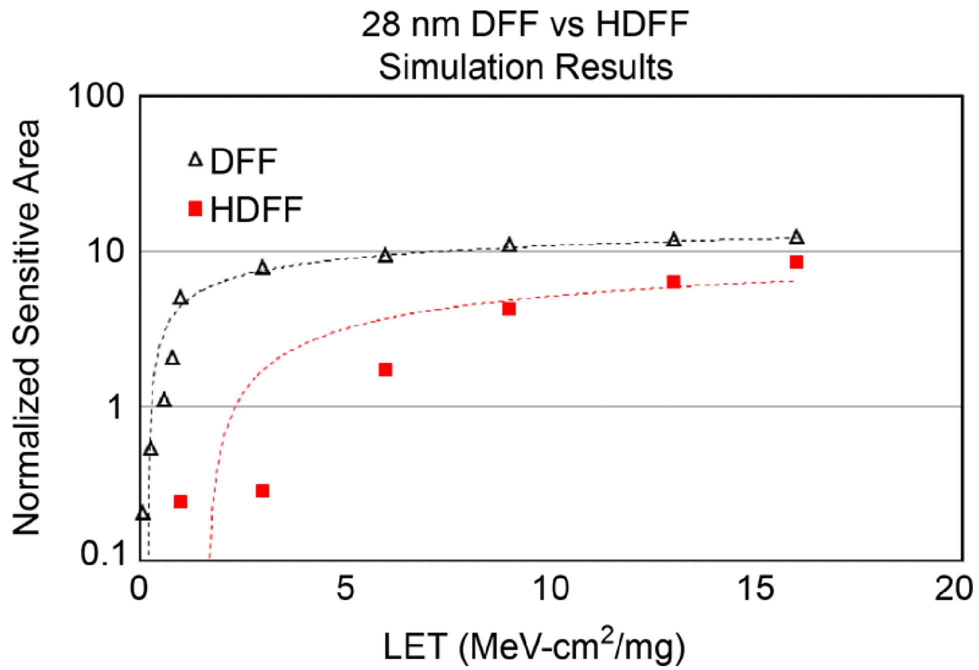

Figure 57: The sensitive area of the baseline DFF and the hardened DFF as calculated by the layout-aware analysis method [82].

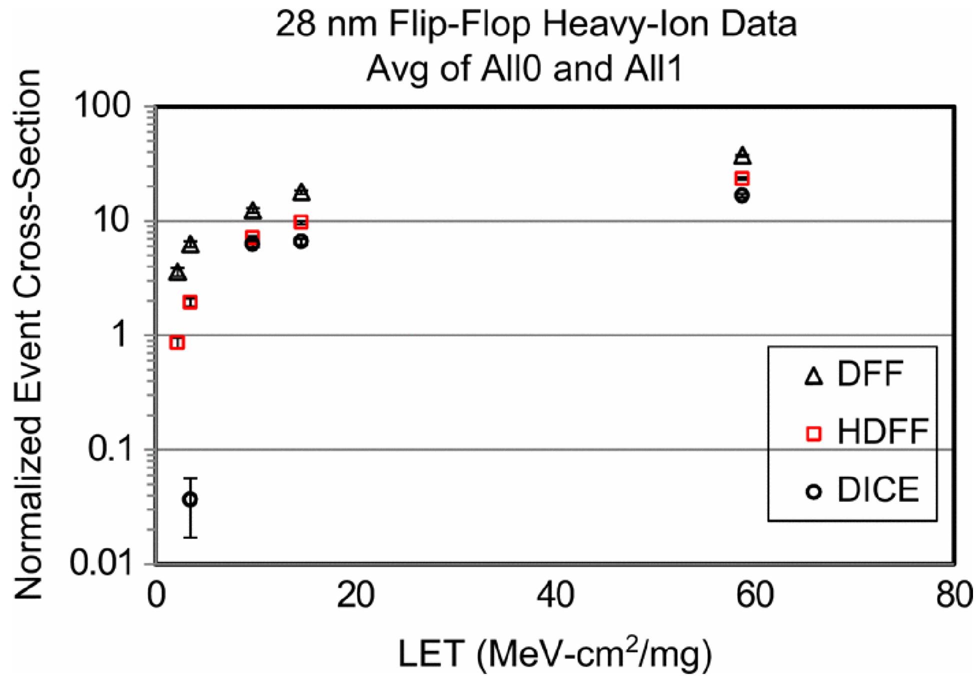

Figure 58: The sensitive area of the baseline DFF, the hardened DFF, and a DICE flip-flop measured in heavy-ion testing [82].

analysis was performed on a dual interlocked storage cell (DICE) hardened flip-flop [83], and the hardened flip-flop was found to be vulnerable to single-ion, low-LET upsets. The DICE hardened flip-flops are supposed to be immune to single-node strikes, however with reduced feature size and increased device density, DICE cells have been found to upset due to low LET particles [49], [83]. The DICE flip-flop analyzed with the layout-aware methods were observed to be sensitive to upset from a simulated particle with an LET of 0.3MeV-cm^2/mg. Figs. 59 and 60 show the heat maps and sensitive areas calculated by the layout-aware analysis methods.

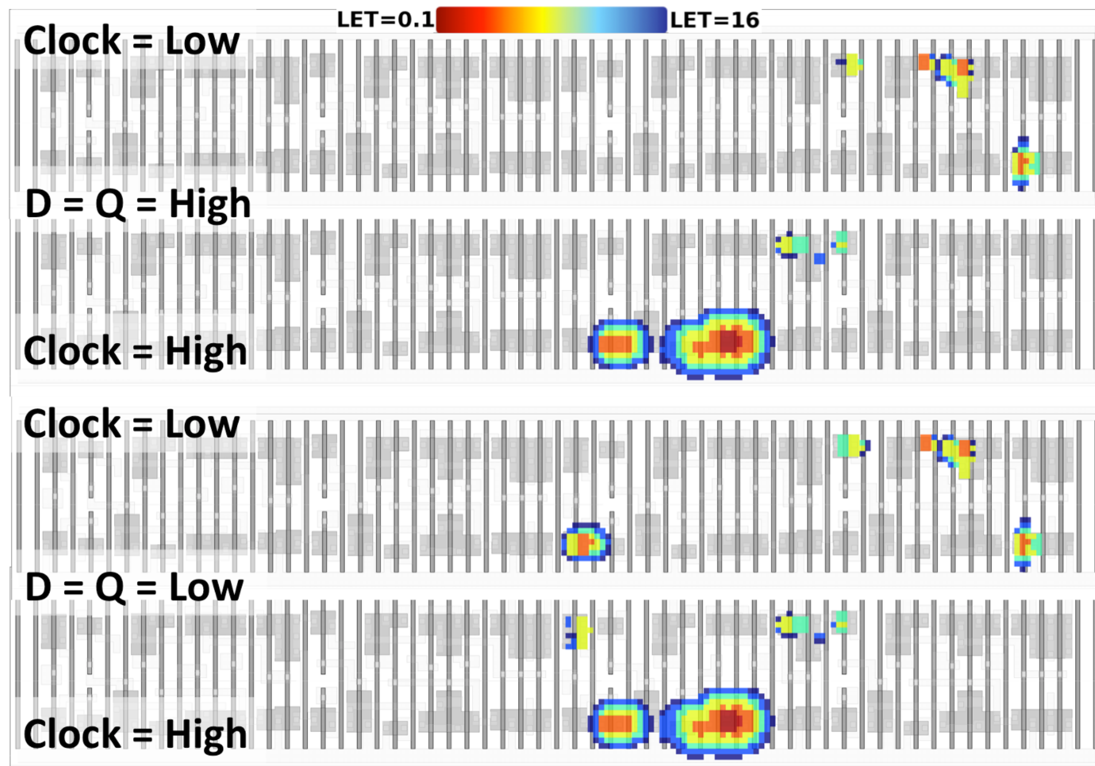

Figure 59: Heat maps of sensitive regions in the DICE flip-flop design under all four combinations of clock and input.

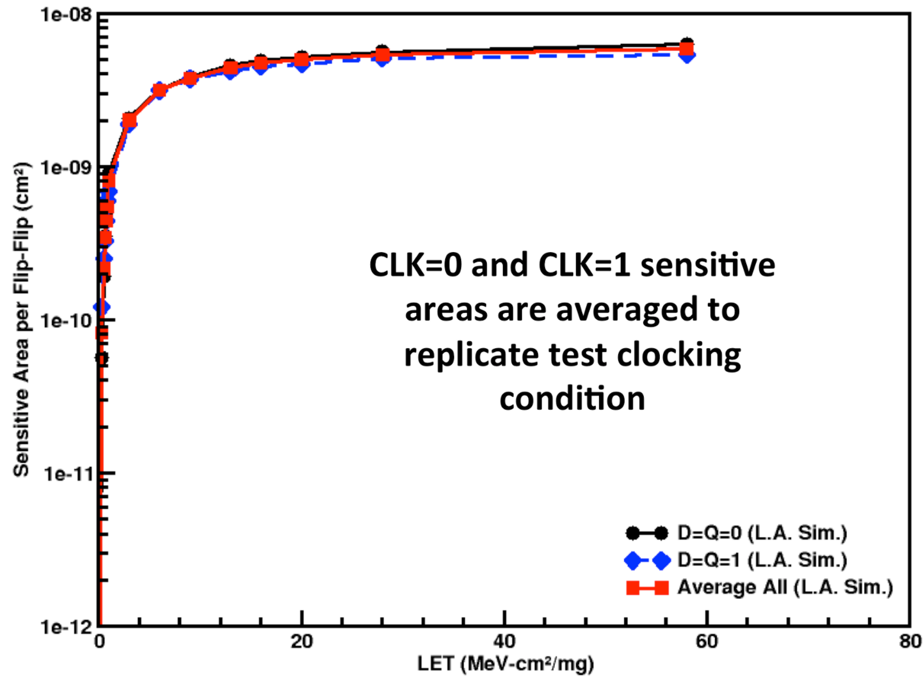

Figure 60: The calculated sensitive area DICE flip-flop for high and low input values.

Operational Amplifier Analysis

Blaine utilized the layout aware simulation methodology and modeling capability in the design and characterization of hardened operational amplifier designs [51], [52]. The layout aware techniques were applied to analysis of the input stage, bias stage, and output stage of a complementary folded cascade operational amplifier. The amplifier is detailed in Appendix A and the schematic is shown in Fig. 69. Using the layout aware simulation capability, Blaine demonstrated the efficacy of multiple hardening techniques that exploited charge sharing to eliminate errant signals through the common mode rejection of the amplifier circuit. Multiple folded-cascode operational amplifiers were designed and fabricated in a commercially available 180nm bulk CMOS technology. Among the amplifier variants were two identically sized amplifiers with a slight variation in the layout of the input transistors.

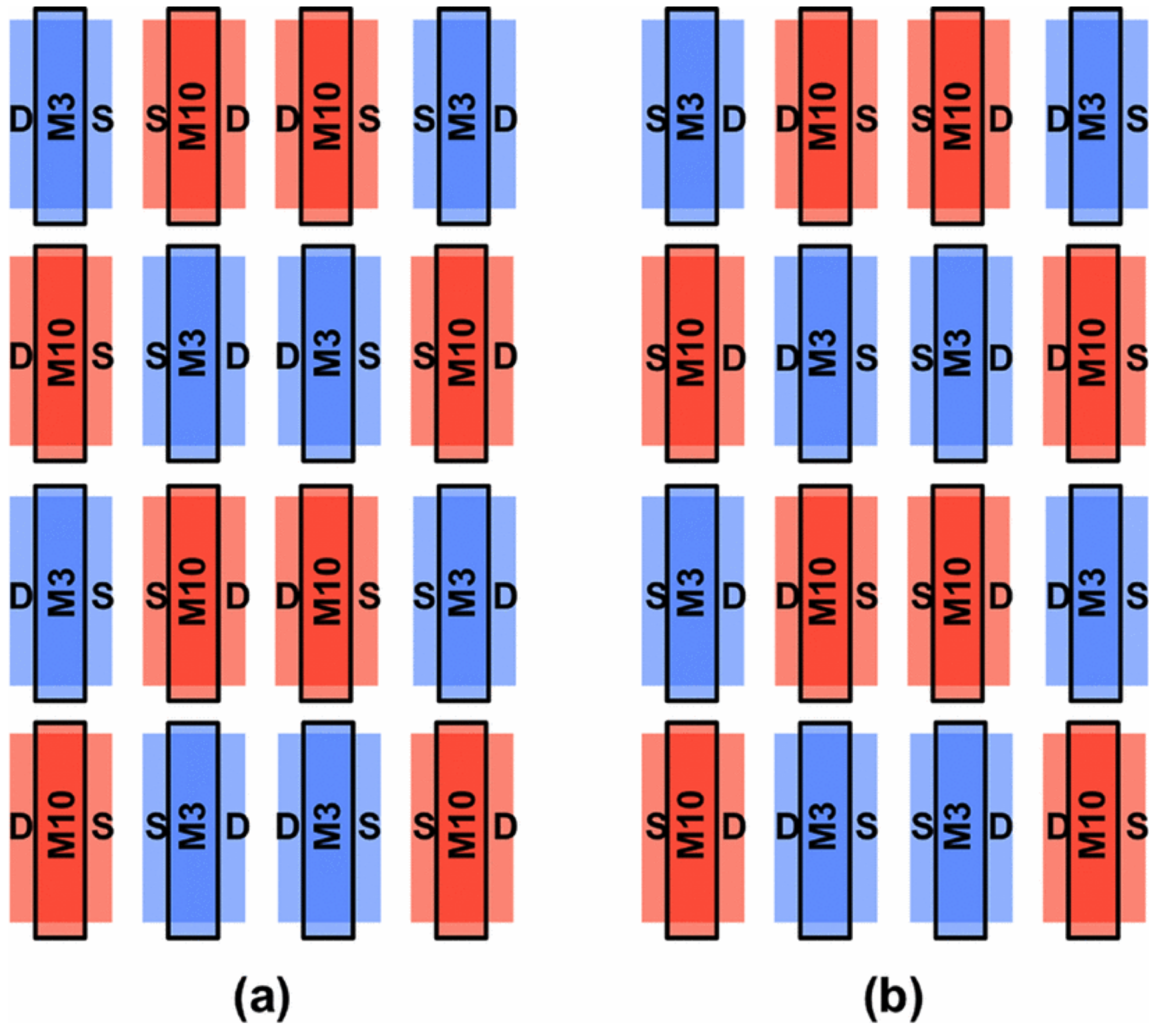

Figure 61: Standard common-centroid layout (a) verses a DCC hardened layout (b) of an amplifier differential input stage [51], [52], [65]. The transistor names, M3 and M10, refer to transistor instances shown in Fig. 69 in Appendix A.

The traditional common centroid layout was utilized in the baseline amplifier design. Blaine utilized the differential charge cancellation technique in the layout of the input transistors of the hardened amplifier [51], [52], [65]. Fig. 61 demonstrates the difference between the layout of the input stage using common centroid and the DCC hardening technique. The amplifier designs are discussed in detail in [51] and [52], however a schematic of the amplifier design is shown in Fig. 69 in Appendix A.

Blaine performed two-photon absorption (TPA) laser testing on the PMOSFET

and NMOSFET transistors in the operational amplifier input stage, to assess experimentally the single-event transient mitigation capability of the DCC technique in a circuit application compared to common centroid layouts in differential amplifier inputs. Blaine measured the peak voltage of the output transient with the amplifier in a non-inverting configuration with a gain of 10V/V. In addition to confirming the efficiency of DCC at mitigating peak transient magnitudes, the data served as a validation of the layout-aware analysis in analog circuits. Fig. 62 shows a heat map of peak voltage pulses, generated from the laser testing on the PMOSFET devices, with a laser energy of 5.1nJ, where laser energy squared is directly proportional to deposited charge. Fig. 63 shows a heat map generated by the layout-aware analysis method, where the peak output voltage was measured during the analysis and mapped to the location of the simulated strike in the layout. The range of the transient peaks in the layout aware analysis ranged from -35mV to 93mV, however only transients with peaks of 20mV and larger are shown in Fig. 63. The layout-aware analysis results show good agreement to the TPA laser test data, both quantitatively and qualitatively. Fig. 64 shows a heat map of peak voltage pulses, generated from the laser testing on the NMOSFET devices, with a laser energy of 5.1nJ. Fig. 65 shows a heat map generated by the layout-aware analysis method, where the peak output voltage was measured during the analysis and mapped to the location of the simulated strike in the layout. The range of the transient peaks in the layout aware analysis on the NMOSFET input transistors ranged from -103mV to 28mV, however only negative pulsing transients with peaks of -20mV and larger are shown in Fig. 65.

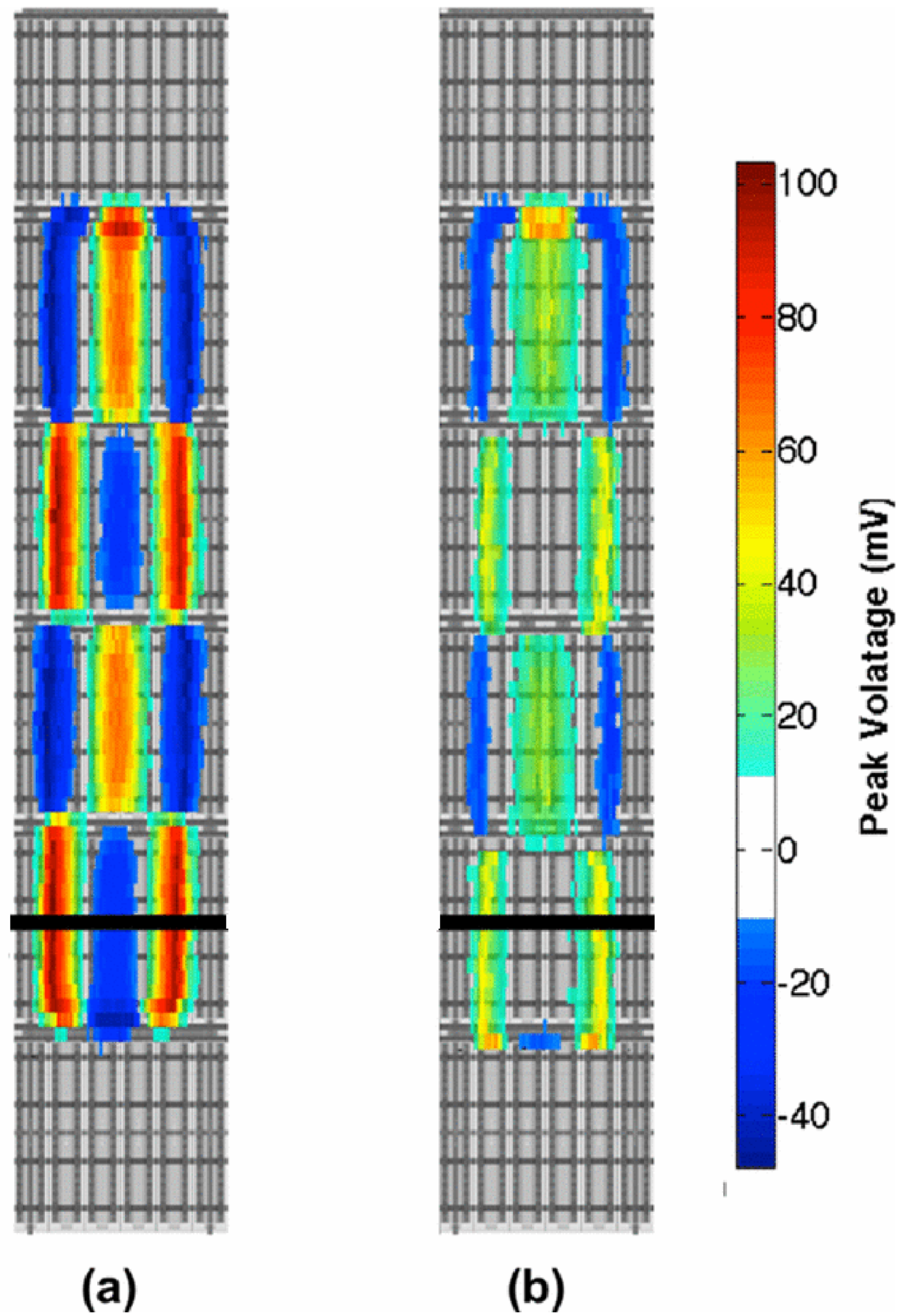

Figure 62: Error map of the maximum output perturbation following 5.1nJ TPA laser strikes to the PMOSFET input transistors using common centroid (a) and DCC layout (b) techniques [52], [65].

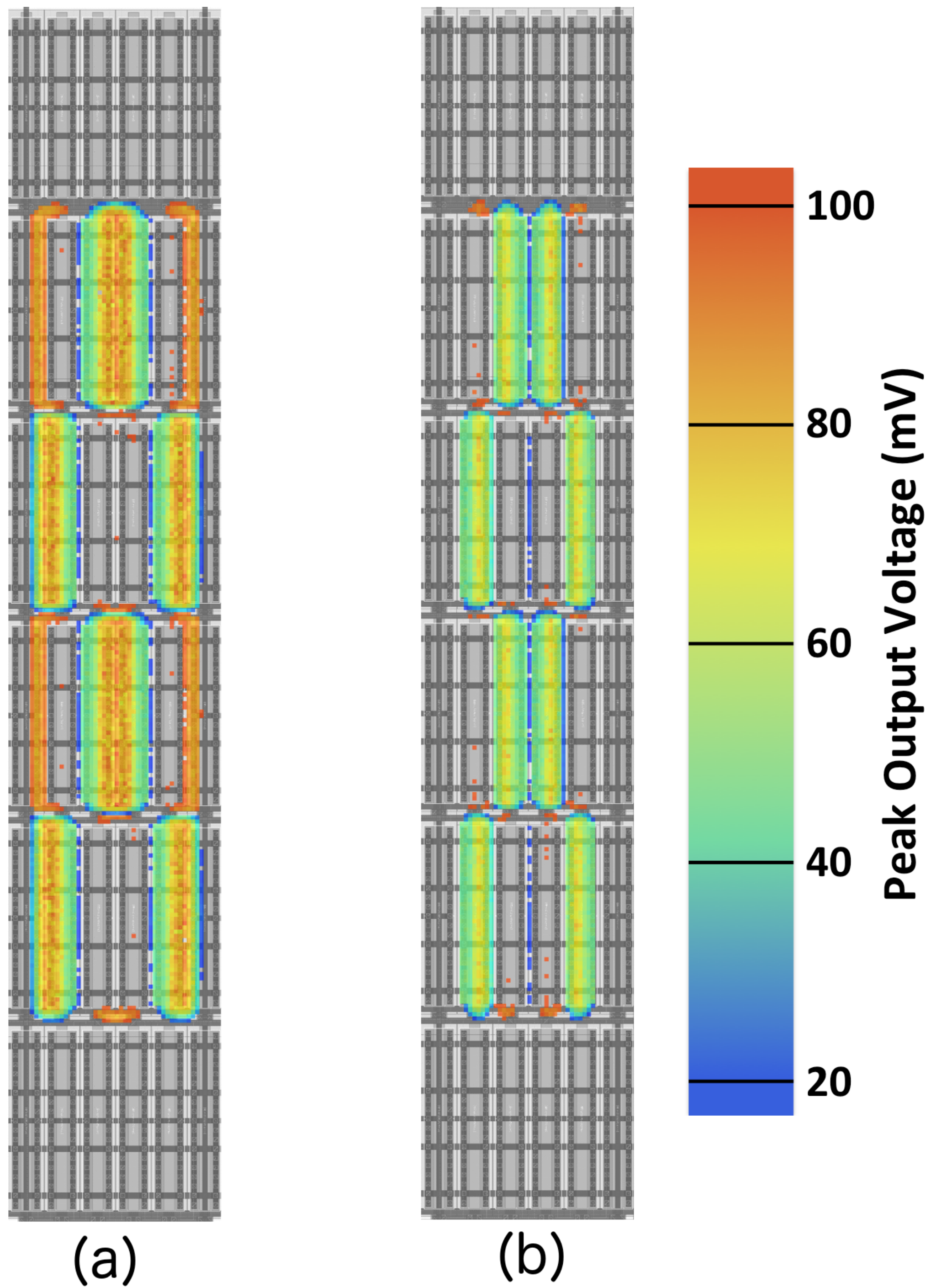

Figure 63: Layout-aware analysis generated heat map of the PMOSFET input transistors for simulated single-event strikes of 30MeV-cm^2/mg using common centroid (a) and DCC layout (b) techniques.

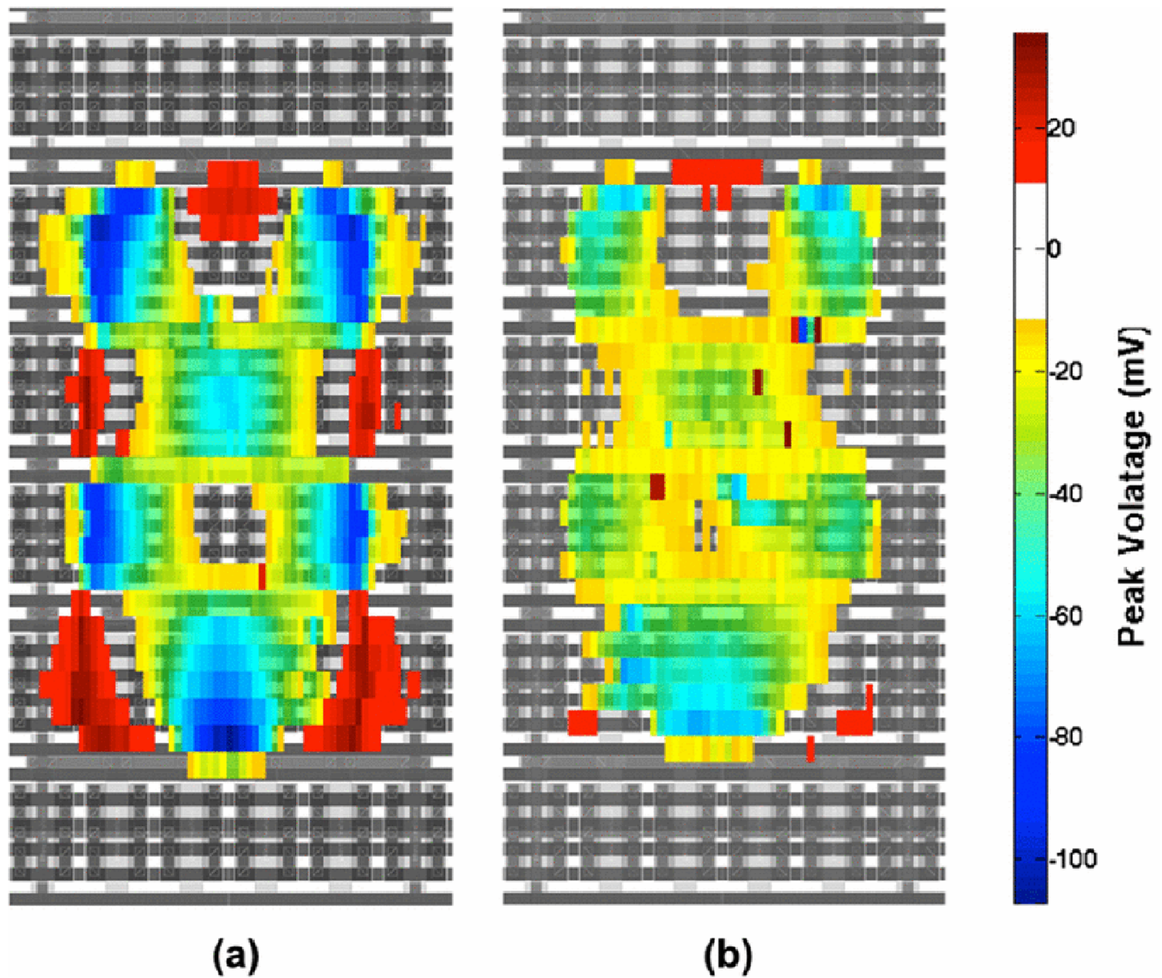

Figure 64: Error map of the maximum output perturbation following 5.1nJ TPA laser strikes to the NMOSFET input transistors using common centroid (a) and DCC layout (b) techniques [52], [65].

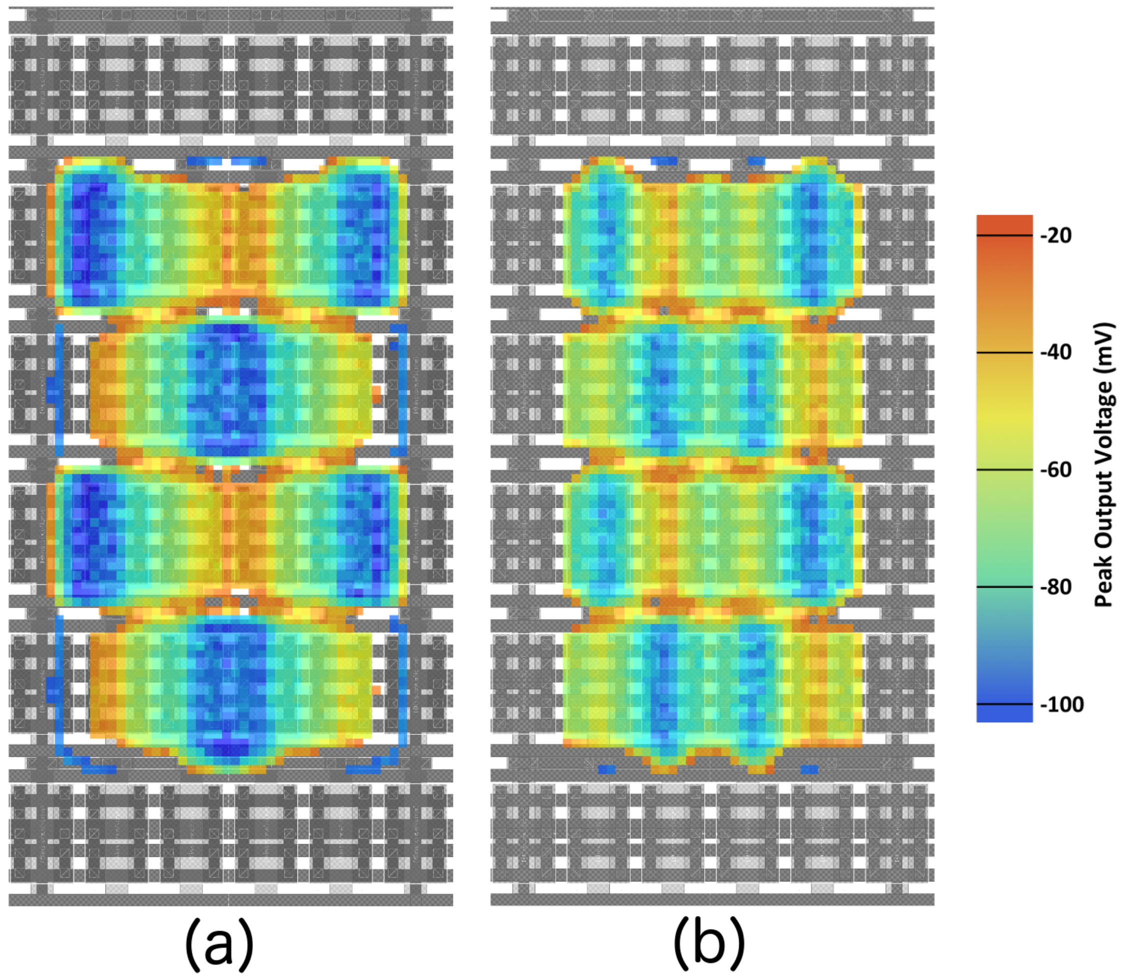

Figure 65: Layout-aware analysis generated heat map of the NMOSFET input transistors for simulated single-event strikes of 30MeV-cm^2/mg using common centroid (a) and DCC layout (b) techniques.

Conclusions

The ability to perform a layout-aware single-event analysis without requiring TCAD for every simulation provides the capability to quickly determine the likely response of a design. The TCAD that is required for technology characterization requires a relatively small number of 2-D TCAD simulations compared to the number of TCAD simulations that would be required for full circuit analysis. The method does sacrifice the ultra high fidelity that full 3-D TCAD can provide, but the fidelity of the results agree well with experimental results and do so with orders of magnitude reduction in total simulation time. Additionally, when comparing designs, this method provides a consistent basis for circuit comparison compared to full 3-D TCAD. Because this method characterizes the technology, the uncertainty of how the TCAD circuit model was developed and if the TCAD devices are placed correctly is eliminated. The layout-aware analysis directly and consistently parses the layout and provides the spatial information to the single-event enabled compact model.

The layout-aware analysis is performed with a circuit-level simulator; therefore, it is considerably faster than 3-D TCAD approaches, while maintaining a level of charge transport fidelity capable of making reasonable estimations of circuit response. On a single-processor desktop workstation, 18,000 strike locations in a 40nm flip-flop were simulated in approximately 45 minutes for each LET included in the analysis. The layout-aware single-event analysis capability that has been developed is orders of magnitude faster than full 3-D TCAD, yet still provides high fidelity results for determining a circuits sensitivity to single-event upset.

The use of industry standard IC design tools at the core of this analysis method provides a path for integration of this analysis into a standard hardened IC design

flow. This prevents the need for a designer to be trained for multiple tool flows, one for electrical design and one for radiation-enabled analysis. Additionally, the ability to stay within one design flow reduces the need for licensing multiple, expensive software packages. The layout-aware analysis provides the designer with a good engineering tool for design analysis in a familiar tool flow that rapidly provides accurate results about the single-event response of their circuit.

CHAPTER VII

IMPACT AND CONCLUSIONS

This research provides integrated circuit designers with tools and methodologies to design radiation-hardened and high-reliability circuits. The models and analysis techniques developed in this research can be utilized prior to circuit fabrication to increase confidence that the circuit will function, as desired, in the intended application and radiation environment. Models, once calibrated and parameterized for a technology, have been applied over multiple geometrical and bias variations in test circuits and compare well to test data. The models are also diagnostic tools to understand unexpected circuit responses to a transient radiation stimulus of an existing circuit. As technologies continue to scale, circuit designs grow in complexity and density, and fabrication costs increase dramatically, modeling and analysis of transient radiation effects on circuits intended for application in a radiation environment is critical prior to fabrication of the design. Early-pass success in the design and fabrication cycle of radiation hardened parts results in reduced costs through fewer design, fabricate, test, and redesign cycles. This research has developed advancements over the historical transient radiation modeling methods through the incorporation of real-time bias dependencies, methods to address the scalability of device layouts in advanced technologies, model parameterization linked to physical processes, and direct analysis of the physical placement of devices within a circuit layout.

Layout-aware dose rate enabled compact modeling methodologies were developed

for application to the modern integrated circuit processes with complex 3-D geometries, device layout configurations, and multiple bias conditions. The historical models have been advanced though the incorporation of bias-dependent modeling methods, generation-rate dependent carrier lifetime models, and scalability over geometry and bias. The methodologies have been applied to multiple dielectically isolated processes across technology type, showing good agreement with test data. The compact models developed in this research enable accurate simulation of the dose rate response of an integrated circuit. The models provide a tool that enables designers to make design decisions with greater confidence of successful circuit operation prior to release for fabrication.

Single-event modeling methodologies have been developed and applied to bulk CMOS, SOI CMOS, and SiGe HBT technologies. The models incorporate bias-dependent transient current generation at each of the P-N junctions in the device. Using TCAD simulations, bulk models have been parameterized to simulate charge sharing resulting from a single-event strike near multiple devices. Device-level layout awareness has been incorporated with a physically parameterized, layout-dependent behavioral parasitic BJT implementation in silicon-on-insulator CMOS technologies. Models have been calibrated to 3-D TCAD simulations and compare well with test data. The combination of bias-dependent response, layout-aware modeling concepts, and parameterization for charge sharing provides the device level modeling capability to perform a layout-aware circuit analysis using standard integrated circuit design and simulation tools.

This research has developed a novel layout-aware analysis capability using circuit-level simulation tools rather than relying on TCAD simulations to characterize the

interaction of multiple devices in a transient radiation environment. The analysis method sacrifices the ultra-high fidelity of 3-D TCAD, however the results have been shown to agree well with digital and analog circuit test data and do so with orders of magnitude reduction in total simulation time. The circuit layout is directly analyzed and the correspondence between the device position in the layout and the schematic instance in the netlist are utilized to calculate the distance from the simulated single event. Results of the analysis can be obtained in the form of heat maps highlighting sensitive regions of the circuit and familiar cross-section type curves. The analysis of a flip-flop design in a 40nm CMOS technology required approximately 45 minutes for each LET included in the analysis. The novel layout-aware analysis techniques provide designers with visual feedback about the sensitivity of a design directly referenced to the layout of the circuit. The use of industry standard IC design tools provides a path for incorporation into a hardened IC design flow and prevents the need for a designer to be trained in multiple tool flows.

Reduced feature sizes, lower supply voltages, and increased device density with technology scaling bring greater sensitivity to low energy transient radiation effects and a charge sharing region that encompasses additional devices, compared to previous technology nodes. Bias-dependence and layout-aware modeling at the device level will be important to capture the transient current and voltage perturbations resulting from a transient radiation event. Highly scaled bulk, partially-depleted and fully-depleted SOI (FD-SOI), and FinFET CMOS technologies will have layout-dependent responses to transient radiation effects. Planar bulk CMOS will be highly susceptible to charge sharing between devices through the substrate, impacting MOSFETs with multiple fingers as well as devices in close proximity. SOI technology

response will be dependent on the layout of the device and the single-event angle of incidence in determining the total collected charge and the strength of the parasitic BJT. For high angle of incidence single events, device placement in SOI technologies is also a significant factor, as a single ion may deposit charge in multiple devices. FinFET device response will depend on the number of fins impacted by the transient radiation event, and where the charge is deposited within the fins. Bulk FinFET technologies will also be susceptible to charge sharing through the substrate, where the charge can be collected in multiple fins. Layout-aware analysis methods will provide a critical capability to the design of hardened circuits, where device separation will be crucial for designs hardened with redundancy [83] and device proximity will be a significant factor in designs that exploit charge sharing for hardness [53], [52], [84].

The modeling and analysis methods developed in this research are being actively utilized in radiation-effects research at universities, aerospace and defense organizations, and commercial integrated circuit design and manufacturing facilities [84]. Layout-aware radiation-enabled models using the methodologies developed in this work have been integrated with process design kits and deployed to the radiation-hardened-by-design community [85]. This research provides methods and capabilities that provide a path forward to enable modeling and simulation of transient radiation effects on radiation-hardened integrated circuits in advanced integrated circuit technologies.

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Appendix A

CIRCUITS FOR MODEL CALIBRATION AND VALIDATION

Model calibration and validation is a critical step in the model development process. Device and circuit models must produce in simulation the response observed in physical measurement of test structures or circuits. This Appendix describes some test structures and circuits that were utilized in this research and are useful in the calibration and validation of transient radiation effects models.

Dose Rate Calibration and Validation Circuits

Photocurrent Collection Arrays

The primary mechanism captured in the layout-aware, bias-dependent dose rate models developed in this research is the photocurrent generated at each junction in the device as a result of a prompt gamma exposure. While 3-D TCAD simulations provide a close estimate of the device response, measured data is the primary calibration source. Flash X-ray and LINAC sources can provide high intensity, short pulses of ionizing radiation. Measuring the photocurrent at the device level is not practical for a single device due to background noise and small geometries. However, a large array of identical devices, wired in parallel, can generate a combined photocurrent capable of being measured.

The design of a photocurrent collection array is relatively straightforward. Geometry based estimations, source dose rate range, and background noise levels are

used to estimate the number of devices required in the array to generate a target photocurrent above the background noise at a specific rate. The array must also be designed with enough margin in metal sizing to withstand the current densities generated in the array. Additionally, MOSFET arrays should use metal lines, rather than polysilicon, to connect the parallel gates. Polysilicon charging could result in localized voltage increases within the array, potentially turning on NMOSFET devices in the array. Schematic representations of an NPN BJT array and NMOSFET array are shown in Figs. 66 and 67, respectively.

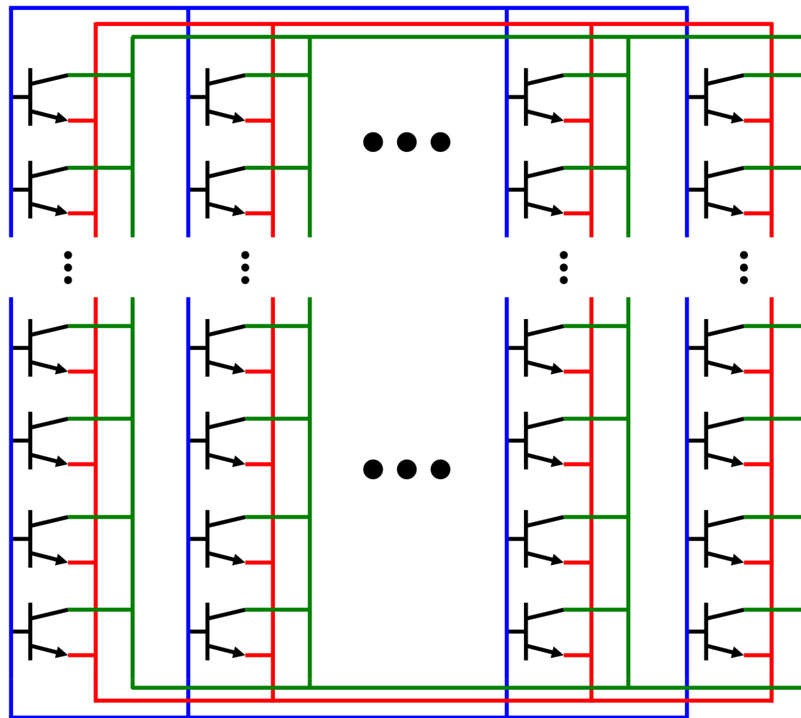

Figure 66: Schematic representation of an NPN BJT array for calibrating dose rate models.

Photocurrent arrays of this type were used to calibrate the dose rate models discussed in Chapter IV. Photocurrents were measured at multiple dose rates to calibrate the peak current value, and the waveform shape was compared to the model generated waveform. Arrays were designed and fabricated to cover multiple

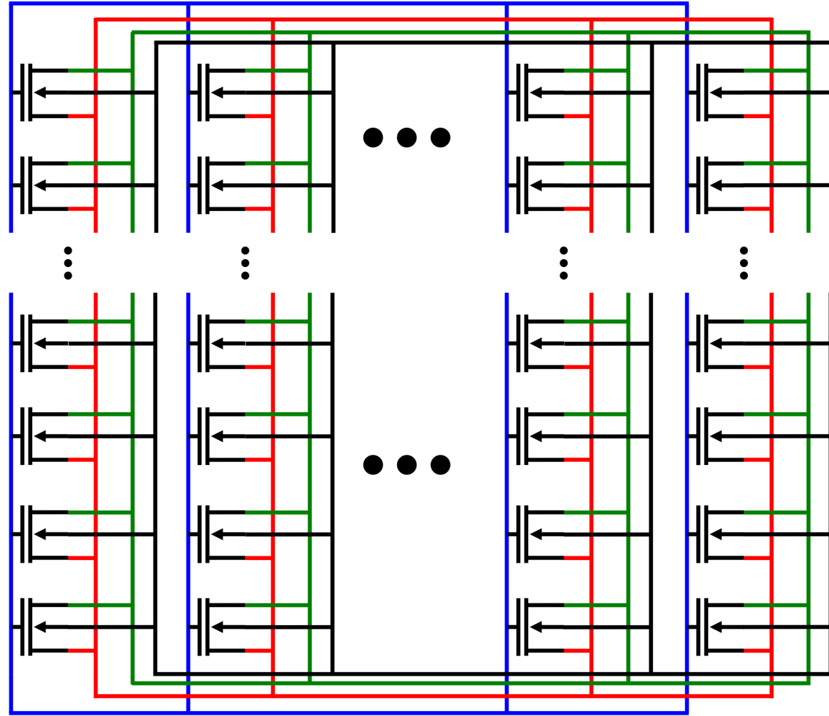

Figure 67: Schematic representation of an NMOSFET array for calibrating dose rate models.

device types and layout geometries. Measurements were also performed at multiple reverse bias voltages (see Fig. 20). The data measured from the arrays were central to the calibration of the photocurrent generation models. Validation of the model performance in a circuit application was performed using measurements obtained from operational amplifiers designed at Vanderbilt University.

Basic Circuits for Dose Rate Response

While large arrays of transistors are useful for calibrating the photocurrent and conductivity modulation response of dose rate models, it is also critical to validate the response of the models in a circuit application. The dose rate models in this research have been validated using complementary folded-cascode operational amplifiers designed at Vanderbilt University [46], [86], [51], [52], [87]. Vallee

introduced the folded-cascode topology in 1994 [88]. BJT and CMOS variants of complementary folded-cascode amplifiers were utilized in the validation of the dose rate models discussed in Chapter IV. A comparison of the models and the test data for the BJT variant are shown in Figs. 17 and 18.

The schematic of the BJT complementary folded-cascode amplifier is shown in Fig. 68. The BJT amplifier is based on a design presented in [46], [79], and [89]. The amplifier used for calibration of models in this research includes a unity-gain output buffer (Q18-Q25) to lower the output impedance of the circuit, improving testability in dose rate experiments. The comparison of the test data and model performance showed good agreement.

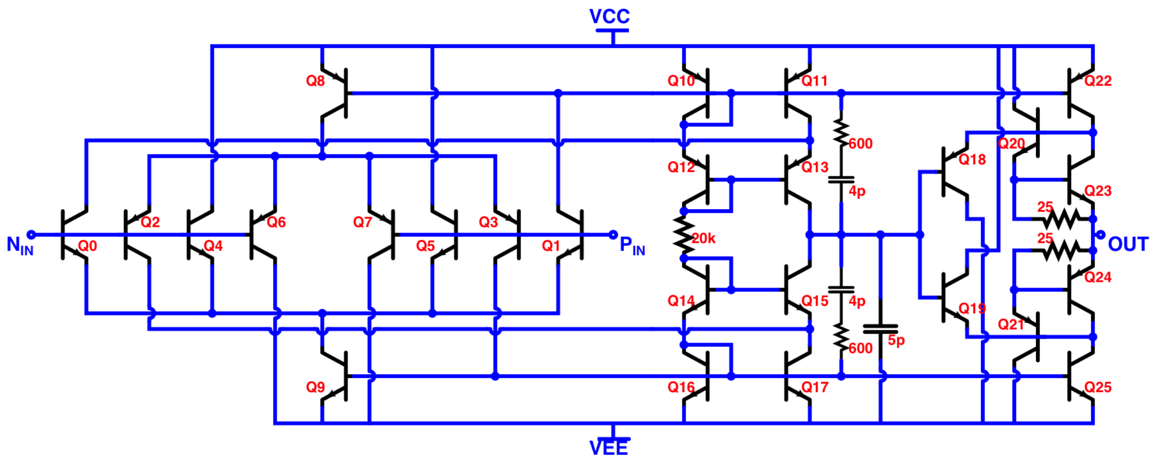

Figure 68: Schematic of the BJT complementary folded-cascode amplifier used to validate model performance in this research [46], [79], [89].

Similarly, a CMOS complementary folded-cascode design was utilized in the validation of the dose rate models. The schematic of the CMOS complementary folded-cascode amplifier is shown in Fig. 69. The design is patterned after the design in [88] and [86] with the addition of a buffer circuit to lower the output impedance to improve testability.

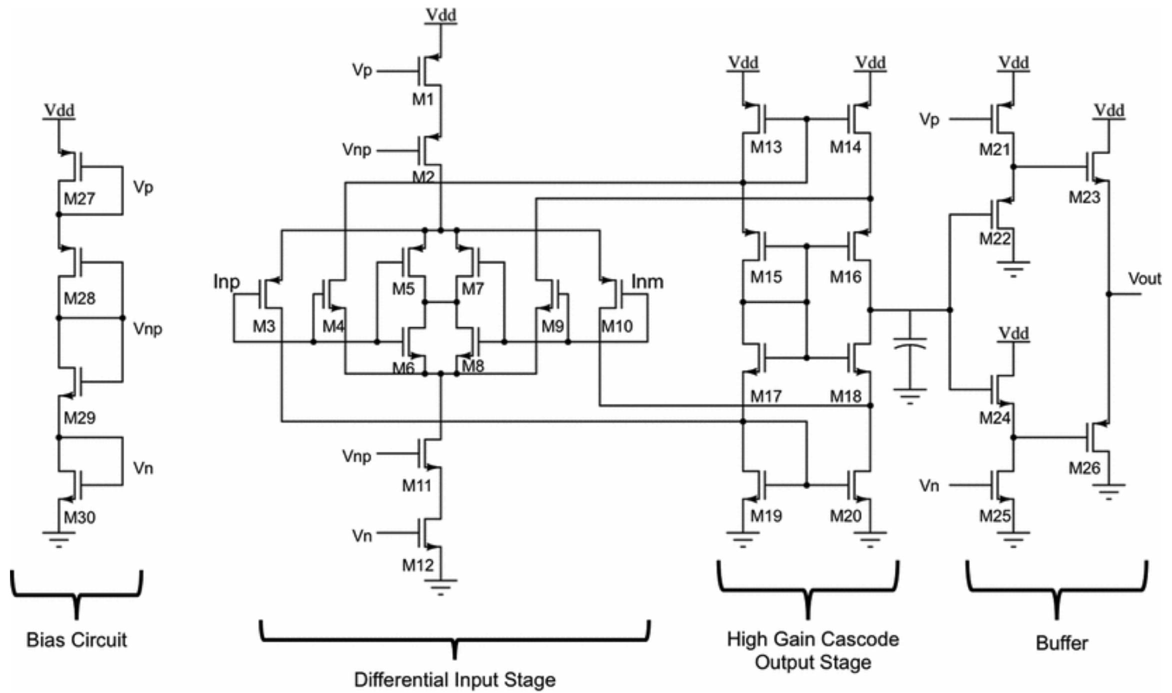

Figure 69: Schematic of the CMOS complementary folded-cascode amplifier used to validate dose rate model and layout-aware analysis performance in this research [88], [86], [51], [52].

Single-Event Calibration and Validation Circuits

On-Chip Measurement of Single-Event Transients

Calibration and validation of single-event enabled models requires the measurement of single-event transients for model to measurement comparison. In some cases, transients have been measured directly using oscilloscopes, however the distortion of the signals due to stray capacitances introduces significant uncertainty [90]. Another common technique is to latch a transient signal after it has gone through a known logic delay path, providing insight into the number of pulses of the delay length or longer [48]. In 2006, Narasimham presented an autonomous on-chip circuit to measure single-event transient pulse widths [91] and physical measurements at the sub-100nm node obtained with this circuit topology [92].

In advanced SOI technologies, significant propagation-induced pulse distortion (broadening and compression due to circuit-level parameters), has been observed and introduces another source of uncertainty between the measured pulse and the originating SET pulse width [93], [94], [95], [96]. Research presented by Loveless in 2012 introduced improvements to the Narasimham circuit and addressed the uncertainty introduced by pulse distortion in the target circuit and quantization error in the measurement circuit [69].

The measurement circuit implementation presented in [69] was fabricated in a 45nm partially-depleted SOI process. The circuit was also fabricated in a 32nm partially-depleted SOI technology [68]. The basic block diagram of the SET characterization test chips in [69] and [68] is shown in Fig. 70. The chip includes

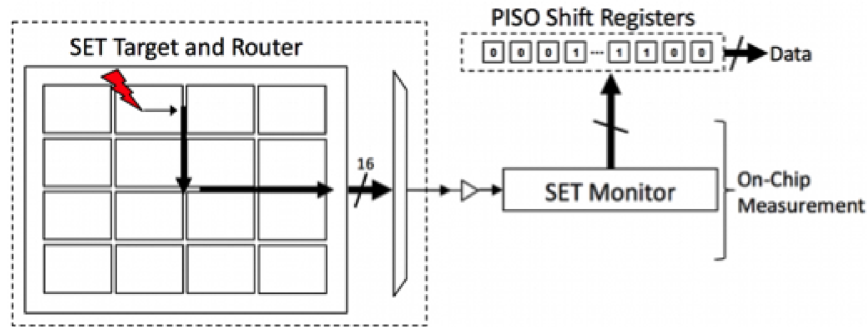

Figure 70: Basic block diagram of SET characterization test chips implemented in 45nm and 32nm partially depleted SOI technologies [69], [68].

radiation target circuitry (the SET target) followed by a multiplexer and distribution network (the SET router) that feeds into an on-chip measurement circuit to capture transient characteristics in this case the pulse width (the SET monitor). The SET target circuitry is comprised of inverter chains of various gate lengths, widths, fingers, threshold implants, oxide thicknesses, serial chain lengths, as well as calibration structures intended for measuring necessary parameters from peripheral circuitry.

Ion-induced transient signals generated within the logic of the target circuitry will propagate through the router to the monitor circuit, which digitizes the SET pulse widths via a basic pipelined time-to-digital converter, and sends the signals off chip through a parallel-in serial-out (PISO) shift register. The foundation of the measurement circuit is based on techniques demonstrated in previous generation technologies [92].

The on-chip SET measurement circuit (SET monitor) used in [69] and [68] was designed to detect pulses as narrow as 15 ps and measure pulse widths greater than 30 ps in increments of approximately 30 ps, up to 1.92 ns. Therefore, it is desirable for the target and the routing from the target to the measurement circuit to be capable of propagating pulse widths of 30-50 ps with a total pulse distortion of less than 30 ps. Simulations of the chip parasitic elements indicate that pulses greater than approximately 50 ps propagate through the logic flow and reach the on-chip measurement circuit, thus setting the lower bound of quantization. This analysis was validated through a comparison of the measured data with that of 3D technology computer-aided design (TCAD) and mixed-mode simulations.

The SET targets require a large total area with high inverter count, to obtain significant statistics in broadbeam heavy-ion testing. In [69] and [68] the required target size was estimated to be equivalent to 24,000 inverters. Based on the observations in [95], [96], and [93], an inverter chain of this length would have significant pulse-width broadening distortion. Therefore, a parallel chain target circuit was designed and implemented.

SET Target to Minimize Pulse Broadening [69]

Pulse broadening in inverter chains occurs in each stage and is an additive effect, thus long inverter chains may exhibit significant pulse broadening. Additionally, such long chains produce a wide pulse-width distribution histogram because of the random nature of strike locations within the chain relative to the output [95], [96], [36], [94]. However, the large sensitive area of long inverter chains is necessary for achieving significant measured SET pulse statistics at reasonable fluences in broadbeam testing.

Utilizing many parallel short inverter chains (twenty-four inverters per chain in [69]) and performing a logical OR of the chain outputs, a new SET characterization target design that achieves the desirable sensitive area for heavy-ion testing, while maintaining the limited pulse distortion benefits of short inverter chain designs, has been designed. Conceptually the design methodology is relatively simple; however the implementation of the design requires careful planning to balance the propagation path through the OR-gate network, and to minimize and match the overall parasitic loads on each propagation path to the on-chip measurement circuit. By implementing this detailed matching and symmetry, the target design ensures propagation paths from each originating inverter chain are identical in loading, thus minimizing/eliminating any positional dependences between individual short chains.

An even number of inverters in the chain will maintain an equal number of sensitive NMOS and PMOS devices per chain. The selection of twenty-four inverters per chain in [69] was determined in order to minimize pulse broadening as well as the cross-sectional area of the OR-Gate network required for logically connecting the chains. The inverter chains were stacked into 16 columns with 64 chains per column, resulting in a total of 24,576 inverters in the minimally sized floating-body inverter target design

[69], [68]. Each short inverter chain output is connected to a single input of the OR-Gate network, resulting in a fan-out of one for each inverter in the target, which avoids the loading based effects observed in [96], [93].

The OR-gate network in [69] is comprised of four-input OR-gates, with 5 levels of OR-gates in the signal path between the inverter chains and the target output. The first three levels combine the 64 rows of inverter chains per column. The final two levels of OR-gates combine the columns to generate the target output. Each four-input OR-gate in the network has a fan-out of one. Additionally, for each level of depth in the OR-gate network, the parasitic load at the OR-gate output is identical to all other OR-gates of that level of depth across the full SET target circuit. This ensures that the propagating transient encounters the same parasitic impedance loading effects, independent of the origination point in the target circuit. Fig. 71 shows a schematic representation of the SET target design, including the inverter chains and the OR-gate network [69]. Fig. 72 shows the layout of the SET target with two different, but equivalent propagation paths highlighted, the full parasitic load network is included in the highlighted area [69]. In the implementation of the 45nm test chip in [69], the sensitive area of the OR-gate network accounts for about 10% of the total target sensitive area. Broadbeam heavy-ion testing performed on the OR-gate network calibration structure (the target design with only the OR-gate network and no inverter chains) yielded a single SET pulse with a width between 52-58 ps up to a fluence of 410^8 particles/cm^2 at an LET of 49 MeV-cm^2/mg [69].

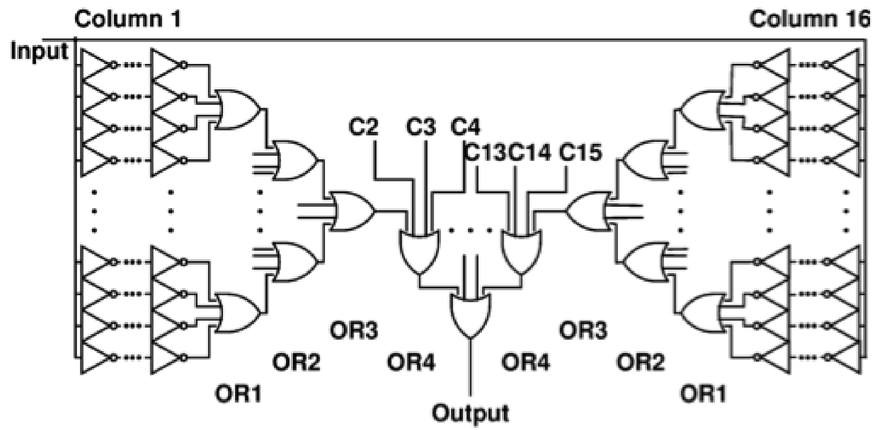

Figure 71: Schematic representing two columns of inverters, columns 1 and 16, and the five levels of the OR-gate network that connect the 1024 inverter chains [69], [68].

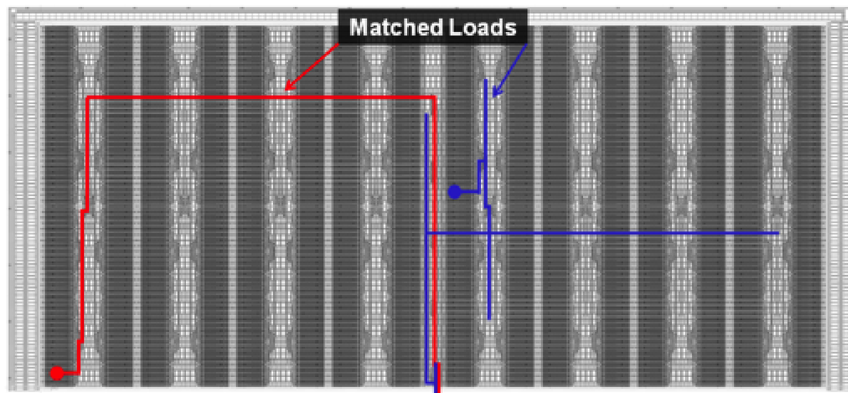

Figure 72: Layout of the SET target with two example propagation paths with identical parasitic loading at each level of the OR-gate network [69], [68].

On-Chip SET Monitor [69]

Loveless presented a novel improvement to the SET measurement circuit in [92], which was implemented for direct quantification of the error due to the on-chip measurement, allowing for a more accurate estimation of the generated SET following an ionizing radiation event. Fig. 73 illustrates a simplified schematic of the on-chip measurement circuit, termed the VU Autonomous Pulse Capture (VUAUTO) circuit. The design is a basic pipelined time-to-digital converter based on principles

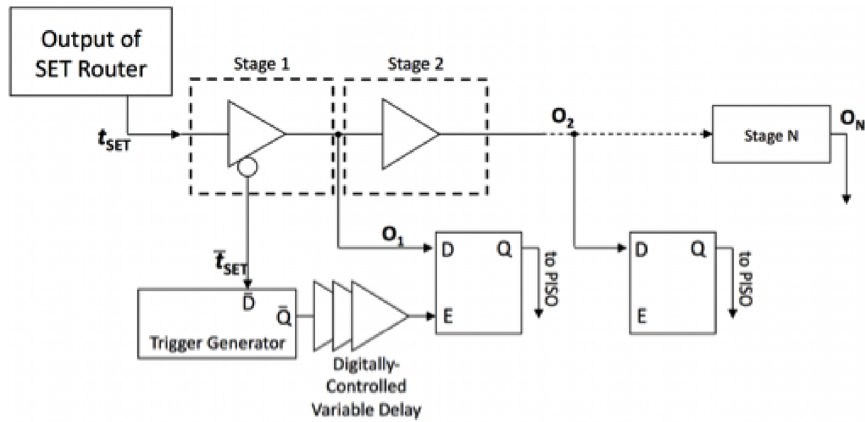

Figure 73: Simplified schematic of the VU Autonomous Pulse Capture Circuit (VUAUTO) implemented in a 45 nm SOI technology. The measurement circuit is capable of detecting pulses as narrow as 15 ps and measuring pulses greater than 30 ps in increments of 30 ps. [69], [68].

described in [92] with three primary modifications for improving the measurement uniformity, decreasing the minimum measurable SET, and allowing for experimental characterization of quantization error. VUAUTO digitizes SET pulse widths in units of the propagation delay of each stage. Functionality details can be found in [92].

The measurement uniformity was improved by implementing non-inverting delay elements in each stage of the measurement circuit to remove the asymmetrical latching preference of the propagating SET. Previous designs have used inverting stages that may result in a skew in the write time in neighboring stages (i.e., write time for logic

HIGH may be different than for logic LOW). A similar improvement was implemented in a measurement circuit proposed in [97].

The minimum detectable SET was improved by modifying the trigger generation block such that pulse widths that are one half the propagation delay of each stage are sufficient to flag an event occurrence (i.e., the minimum detectable event is one half the resolution of the minimum measurable event). The trigger generator consists of a basic D-latch followed by a buffer and delay element. In the event that a transient (tSET) arrives at the input of the measurement circuit (the transient will always be a logic-HIGH pulse), a complementary pulse (tSET bar) will be generated by the first measurement stage and will propagate to the input of the trigger generator. The trigger generator will latch the occurrence of the event until an external reset signal is provided and propagate the latched signal through a delay element in order to halt the digitization of the SET.

Finally, a mechanism was designed to experimentally measure the quantization error of the measurement circuit. A digitally controlled variable delay element was utilized to delay the event trigger such that various numbers of measurement stages may be utilized to digitize the SET. For example, 10% measurement utilization indicates that the first 10% of the serially connected delay elements were utilized for quantizing the SET pulse width. Increasing the utilization factor increases the maximum measurable pulse, but also requires the transients to propagate through more stages.

The offset (i.e. measurement bias) and/or skew associated with the on-chip capture and measurement of the SET pulse width were extracted by adjusting the percentage of the measurement circuit utilized. Experiments on three devices

(minimal inverter with 24,576 inverters in one long chain, and two short-chain targets with inverters 5 times the minimum inverter size) were performed for measurement utilization factors of 30%, 49%, 56%, 70%, and 80%. Fig. 74 shows the average SET pulse width for each target normalized to the value obtained at 30% measurement utilization versus the percent utilization. Increasing the percent utilization introduces a positive offset (increased average value) to the measurement. The offset is a consequence of the increased propagation path of the SET through the circuit and the resulting broadening of the transient. Increases in SET pulse widths of 60% are observed for the range of utilization factors used during the measurements. Additionally, a negative offset (decreased average value) is observed between 49% and 56% utilization due to a parasitic capacitance formed from a serpentine bend in device and interconnect structures in the circuit layout.

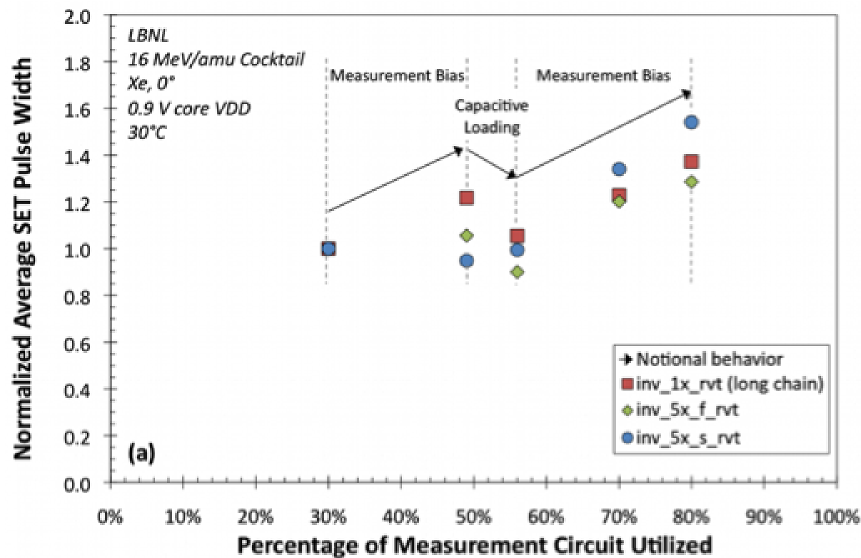

Figure 74: Average of the measured SET pulse widths normalized to the value obtained at 30% measurement utilization verses the percent utilization [69].

Fig. 75 shows the standard deviation (σ) of the SET distribution normalized to the value obtained at 30% measurement utilization versus the percent utilization.

The standard deviation is an indication of the distribution spread; results indicate that increasing percent utilization results in a positive skew in the distribution, thus longer positive tails and higher standard deviations. The standard deviation for the range of utilization factors used increases by as much as 260% over baseline values. This is most likely due to error accumulation through the pipelined serial chain.

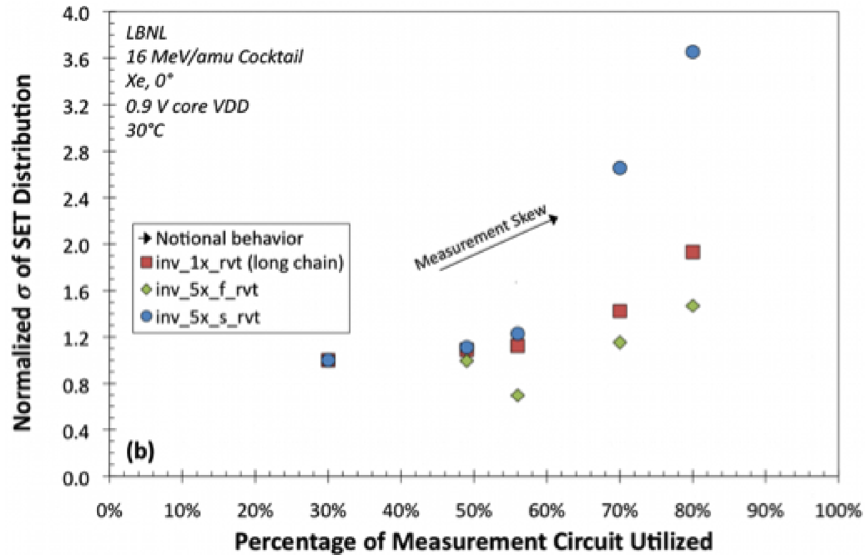

Figure 75: Standard deviation of the SET distribution normalized to the value obtained at 30% measurement utilization verses the percent utilization [69].

Conclusions

Direct measurement of fast-transient single event signatures often involves considerable uncertainty due to the limitations of monitoring circuitry. A built-in-self-test circuit (using a pipelined time-to-digital architecture) for the measurement of SETs has been presented by Loveless in a 45nm SOI technology, and by Maharrey in a 32nm SOI technology, that allows for the extraction of measurement-induced uncertainty [69], [68]. The measurement bias and skew was found to increase with increasing pipeline stages. Experimental capture of the phenomenon allows for a removal of the

error from the data sets and improves the fidelity of the measurements.

SET pulse-width data from heavy-ion exposures using the improved on-chip measurement circuit presented by Loveless has been used to calibrate the layout-aware single-event SOI CMOS compact models discussed in Chapter V. The data provides critical information on pulse width distribution for a large sample of transients.

Circuits for Radiation Effects Self Test (CREST)

The measurement of single-event upsets in a flip-flop design is another useful calibration and validation point for single-event models and the layout-aware analysis methods. In 2005, Marshall, et. al., presented the design of a circuit for radiation self-test (CREST) circuit to measure single-event upsets in flip-flops. This self-test method has been implemented on many test chips used in the calibration and validation of models in this research [49], [82], [98]. The CREST circuit contains a flip-flop shift register, error detection circuitry, and an error counter. A basic block diagram of the CREST circuit is shown in Fig. 76.

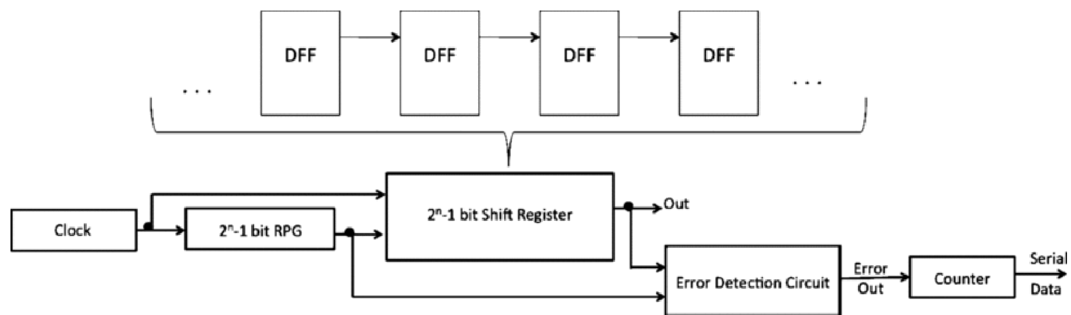

Figure 76: Circuit for Radiation Effects Self-Test (CREST) configuration used for direct measurement of upsets [49], [81].

The measurements utilized in this research bypassed the random pattern generator shown in Fig. 76. The inputs to the shift registers were blanket patterns of either

zero or one. The output of the shift register are compared to the input pattern using an exclusive OR (XOR) gate to determine if there was an upset shifted to the output of the register. If an upset is detected, the low to high transition at the output of the XOR is detected by an asynchronous counter, hardened using triple-modular redundancy. The counter is periodically read and reset by an FPGA control board, and the counter output is logged to a test results file.

During the course of this research, some modifications to CREST were designed to handle at speed pattern testing, without having to synchronize the input pattern generator and register output [81]. Additionally, an on-chip variable frequency clock and on-chip checkerboard pattern generator were designed. The modification still provides the capability for an off-chip shift-register clock and the use of blanket patterns. The block diagram of the modified error detection circuitry is shown in Fig. 77. This modification utilizes hardened XOR gates, with a flip-flop latching the output, to compare the outputs of the last four flip-flops in the shift register, rather than synchronizing the input and output signals. The modification provides for the capability to detect upsets for blanket patterns and checkerboard patterns. The flip-flops in the XOR gates latch the signal at the clock edge following the data latching into one of the final four flip-flops. Table 8 shows the propagation of an upset through the shift register and error detection, and Table 9 shows the propagation of an upset through the register and error detection.

The on-chip variable frequency clock generator, shown in Fig. 78, consists of a differential voltage-controlled oscillator with a simulated maximum frequency capability of 10GHz, followed by a single-ended amplifier in order to interface with CMOS logic. Two trim terminals, Ntune and Ptune, are available to tune out

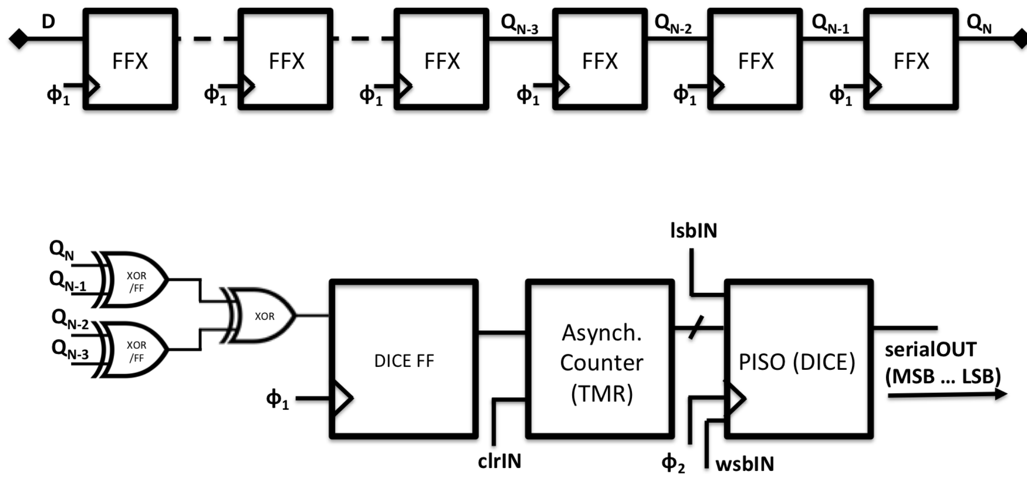

Figure 77: Block diagram of the flip-flop error detection circuit modification using XOR gates to compare the outputs of the final four flip-flops in the shift register.

Table 8: Propagation of an upset in a blanket zero pattern, starting in data as 1, through the final four flip-flops and the XOR based error detection circuit. The flip-flops in the XOR latch the signal at the clock edge following the data latching into one of the final four flip-flops. An error is counted when the Error output transitions from the low state (0) to the high state (1).

Clock	Data	Q_{N-3}	Q_{N-2}	Q_{N-1}	Q_N	$Q_{N-3} \oplus Q_{N-2}$	$Q_{N-1} \oplus Q_N$	Error
0	0,0,1,0	0	0	0	0	0	0	0
1	0,0,0,1	0	0	0	0	0	0	0
2	0,0,0,0	1	0	0	0	0	0	0
3	0,0,0,0	0	1	0	0	1	0	0
4	0,0,0,0	0	0	1	0	1	0	1
5	0,0,0,0	0	0	0	1	0	1	1
6	0,0,0,0	0	0	0	0	0	1	1
7	0,0,0,0	0	0	0	0	0	0	1
8	0,0,0,0	0	0	0	0	0	0	0
9	0,0,0,0	0	0	0	0	0	0	0
10	0,0,0,0	0	0	0	0	0	0	0

Table 9: Propagation of an upset in a checkerboard pattern, starting in data as 1, through the final four flip-flops and the XOR based error detection circuit. The flip-flops in the XOR latch the signal at the clock edge following the data latching into one of the final four flip-flops. An error is counted when the Error output transitions from the low state (0) to the high state (1).

Clock	Data	Q_{N-3}	Q_{N-2}	Q_{N-1}	Q_N	$Q_{N-3} \oplus Q_{N-2}$	$Q_{N-1} \oplus Q_N$	Error
0	0,1,1,1	0	1	0	1	1	1	0
1	1,0,1,1	1	0	1	0	1	1	0
2	0,1,0,1	1	1	0	1	1	1	0
3	1,0,1,0	1	1	1	0	0	1	0
4	0,1,0,1	0	1	1	1	0	1	1
5	1,0,1,0	1	0	1	1	1	0	1
6	0,1,0,1	0	1	0	1	1	0	1
7	1,0,1,0	1	0	1	0	1	1	1
8	0,1,0,1	0	1	0	1	1	1	0
9	1,0,1,0	1	0	1	0	1	1	0
10	0,1,0,1	0	1	0	1	1	1	0

mismatch in the VCO, and vIN controls the frequency of the VCO. The VCO output is frequency divided by a factor of two, limiting the maximum clock frequency to an appropriate range for the shift registers. A 2:1 multiplexer is used to select either the on-chip generated clock or an external clock signal, with clkSELIN as the select signal. The multiplexer output is buffered to each of the shift register clock trees. The frequency divided VCO output is further divided by a factor of 64 and buffered off chip for monitoring the clock during testing.

The basic block diagram of the pattern generator is shown in Fig. 79. The clock input to the circuit is provided from the output of the CREST clock tree nearest to the physical location of the pattern generator, and is labeled cout. The signal is buffered and the frequency divided by a factor of two in order to generate logic high and low signals spanning one complete clock cycle each. The output of the frequency divider is triplicated, delayed, and inverted in order to generate a 90 degree phase shift from the input clock (this ensures that the data pattern changes state only during

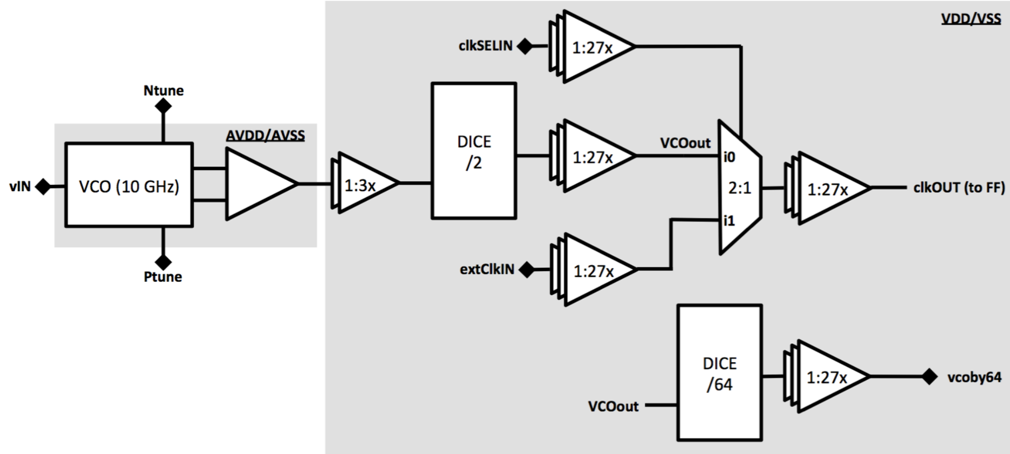

Figure 78: Block diagram of the on-chip clock generation circuit.

the LOW portion of the clock cycle. The output signal represents a checkerboard data pattern (i.e., logic high followed by logic low). A 2:1 multiplexer is used to select either the static input data provided off chip as in_crest or the checkerboard, where p_sel is utilized as the off-chip selection signal. The three data signals (pA, pB and pC) are then passed to a majority voter to generate the input data signal to the CREST block, where the triple redundancy is used to hardened the input pattern against single-event transients. Synchronization of the input data pattern with the clock is not required because the data is generated from the clock signal near the physical location of the data input to the CREST block.

The measured data from CREST circuits was utilized in the calibration and validation of single-event models discussed in Chapter V, and the data was used to validate the layout-aware analysis results discussed in Chapter VI.

Complementary Folded-Cascode Operational Amplifier

A variant of the amplifier design shown in Fig. 69 was designed and fabricated in a 180nm bulk CMOS technology. This amplifier design, and variants of hardening

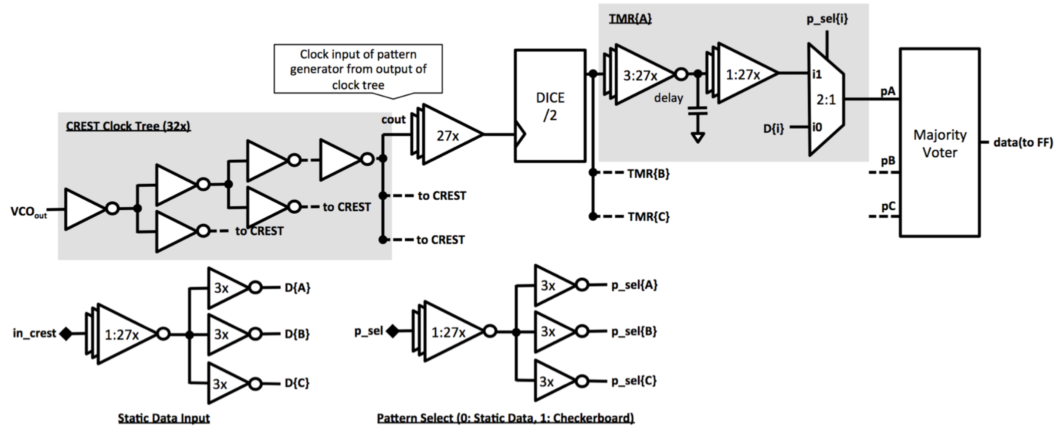

Figure 79: Block diagram of the on-chip input pattern generation circuit.

techniques were used to validate the layout-aware analysis methods discussed in Chapter VI [51], [52]. Different methods of input stage and cascode stage layout based hardening techniques were tested using TPA laser stimulus in [52] and [87]. The measurements were compared to the simulation results from the layout-aware analysis and showed good agreement (Figs. 62, 63, 64, and 65), as discussed in Chapter VI.

Appendix B

EXAMPLE SPICE MODEL CARDS

This Appendix contains freely available SPICE model files used in the example integration cases in Appendix C. The included model cards cover bulk CMOS, SOI CMOS, and BJT technologies using BSIM4 (Tables 11 and 12), BSIMSOI (Tables 13 and 14), and MEXTRAM (Table 15) models, respectively. Table 16 is a SPICE compatible netlist of the bias-dependent current source for single-event simulation, implementing the schematic in Fig. 8. The SPICE models will simulate directly in Mentor Graphics Eldo [39] and in the Cadence Spectre Simulator [62], with slight modification. Spectre requires a directive before the files are included and again after the include statements. Table 10 demonstrates the Spectre directives and inclusion of the 45nm BSIM4 Bulk CMOS Models and the SPICE component bias-dependent source implementation in Tables 11, 12, and 16.

Table 10: Spectre directives for inclusion of SPICE format models

```
// Begin of SPICE file inclusion section
// Directive syntax: simulator lang=spice |spectre
simulator lang=spice
.include 45nm_nmos.mod
.include 45nm_pmos.mod
.include Bias_Dep_SET.mod
simulator lang=spectre
```

45nm BSIM4 Bulk CMOS Models

Table 11: 45nm bulk NMOSFET model from the Arizona State University Predictive Technology Models [55], [57]

```
* PTM High Performance 45nm Metal Gate / High-K / Strained-Si
* nominal Vdd = 1.0V
.model nmos nmos level = 54
+ version   = 4.0        binunit   = 1          paramchk  = 1
+ mobmod    = 0          capmod    = 2          igcmod    = 1
+ igbmod    = 1          geomod    = 1          diomod    = 1
+ rdsmod    = 0          rbodymod  = 1          rgatemod  = 1
+ permod    = 1          acnqsmod  = 0          trnqsmod  = 0
+ tnom      = 27         toxe      = 1.25e-009  toxp      = 1e-009
+ toxm      = 1.25e-009  dtox      = 2.5e-010   epsrox    = 3.9
+ wint      = 5e-009     lint      = 3.75e-009  ll        = 0
+ wl        = 0          lln       = 1          wln       = 1
+ lw        = 0          ww        = 0          lwn       = 1
+ wwn       = 1          lwl       = 0          wwl       = 0
+ xpart     = 0          toxref    = 1.25e-009  xl        = -20e-9
+ vth0      = 0.46893    k1        = 0.4        k2        = 0
+ k3        = 0          k3b       = 0          w0        = 2.5e-006
+ dvt0      = 1          dvt1      = 2          dvt2      = 0
+ dvt0w     = 0          dvt1w     = 0          dvt2w     = 0
+ dsub      = 0.1        minv      = 0.05       voffl     = 0
+ dvtp0     = 1e-010     dvtp1     = 0.1        lpe0      = 0
+ lpeb      = 0          xj        = 1.4e-008   ngate     = 1e+023
+ ndep      = 3.24e+018  nsd       = 2e+020     phin      = 0
+ cdsc      = 0          cdscb     = 0          cdscd     = 0
+ cit       = 0          voff      = -0.13      nfactor   = 2.22
+ eta0      = 0.0055     etab      = 0          vfb       = -0.55
+ u0        = 0.054      ua        = 6e-010     ub        = 1.2e-018
+ uc        = 0          vsat      = 170000     a0        = 1
+ ags       = 0          a1        = 0          a2        = 1
+ b0        = 0          b1        = 0          keta      = 0.04
+ dwg       = 0          dwb       = 0          pclm      = 0.02
+ pdiblc1   = 0.001      pdiblc2   = 0.001      pdiblcb   = -0.005
+ drout     = 0.5        pvag      = 1e-020     delta     = 0.01
+ pscbe1    = 8.14e+008  pscbe2    = 1e-007     fprout    = 0.2
+ pdits     = 0.08       pditsd    = 0.23       pditsl    = 2300000
+ rsh       = 5          rdsw      = 155        rsw       = 80
+ rdw       = 80         rdswmin   = 0          rdwmin    = 0
+ rswmin    = 0          prwg      = 0          prwb      = 0
+ wr        = 1          alpha0    = 0.074      alpha1    = 0.005
```

+ beta0	= 30	agidl	= 0.0002	bgidl	= 2.1e+009
+ cgidl	= 0.0002	egidl	= 0.8	aigbacc	= 0.012
+ bigbacc	= 0.0028	cigbacc	= 0.002	nigbacc	= 1
+ aigbinv	= 0.014	bigbinv	= 0.004	cigbinv	= 0.004
+ eigbinv	= 1.1	nigbinv	= 3	aigc	= 0.02
+ bigc	= 0.0025	cigc	= 0.002	aigsd	= 0.02
+ bigsd	= 0.0025	cigsd	= 0.002	nigc	= 1
+ poxedge	= 1	pigcd	= 1	ntox	= 1
+ xrcrg1	= 12	xrcrg2	= 5	cgso	= 1.1e-010
+ cgdo	= 1.1e-010	cgbo	= 2.56e-011	cgdl	= 2.653e-010
+ cgsl	= 2.653e-010	ckappas	= 0.03	ckappad	= 0.03
+ acde	= 1	moin	= 15	noff	= 0.9
+ voffcv	= 0.02	kt1	= -0.11	kt1l	= 0
+ kt2	= 0.022	ute	= -1.5	ua1	= 4.31e-009
+ ub1	= 7.61e-018	uc1	= -5.6e-011	prt	= 0
+ at	= 33000	fnoimod	= 1	tnoimod	= 0
+ jss	= 0.0001	jsws	= 1e-011	jswgs	= 1e-010
+ njs	= 1	ijthsfwd	= 0.01	ijthsrev	= 0.001
+ bvs	= 10	xjbvs	= 1	jsd	= 0.0001
+ jswd	= 1e-011	jswgd	= 1e-010	njd	= 1
+ ijthdfwd	= 0.01	ijthdrev	= 0.001	bvd	= 10
+ xjbvd	= 1	pbs	= 1	cjs	= 0.0005
+ mjs	= 0.5	pbsws	= 1	cjsws	= 5e-010
+ mjsws	= 0.33	pbswgs	= 1	cjswgs	= 3e-010
+ mjswgs	= 0.33	pbd	= 1	cjd	= 0.0005
+ mjd	= 0.5	pbswd	= 1	cjswd	= 5e-010
+ mjswd	= 0.33	pbswgd	= 1	cjswgd	= 5e-010
+ mjswgd	= 0.33	tpb	= 0.005	tcj	= 0.001
+ tpbsw	= 0.005	tcjsw	= 0.001	tpbswg	= 0.005
+ tcjswg	= 0.001	xtis	= 3	xtid	= 3
+ dmcg	= 0	dmci	= 0	dmdg	= 0
+ dmcgt	= 0	dwj	= 0	xgw	= 0
+ xgl	= 0	rshg	= 0.4	gbmin	= 1e-010
+ rbpb	= 5	rbpd	= 15	rbps	= 15
+ rbdb	= 15	rbsb	= 15	ngcon	= 1

Table 12: 45nm bulk PMOSFET model from the Arizona State University Predictive Technology Models [55], [57]

```
* PTM High Performance 45nm Metal Gate / High-K / Strained-Si
* nominal Vdd = 1.0V
.model pmos pmos level = 54
+ version   = 4.0         binunit   = 1          paramchk  = 1
+ mobmod    = 0           capmod    = 2          igcmod    = 1
+ igbmod    = 1           geomod    = 1          diomod    = 1
+ rdsmod    = 0           rbodymod  = 1          rgatemod  = 1
+ permod    = 1           acnqsmod  = 0          trnqsmod  = 0
+ tnom      = 27          toxe      = 1.3e-009   toxp      = 1e-009
+ toxm      = 1.3e-009    dtox      = 3e-010     epsrox    = 3.9
+ wint      = 5e-009      lint      = 3.75e-009  ll        = 0
+ wl        = 0           lln       = 1          wln       = 1
+ lw        = 0           ww        = 0          lwn       = 1
+ wwn       = 1           lwl       = 0          wwl       = 0
+ xpart     = 0           toxref    = 1.3e-009   xl        = -20e-9
+ vth0      = -0.49158    k1        = 0.4        k2        = -0.01
+ k3        = 0           k3b       = 0          w0        = 2.5e-006
+ dvt0      = 1           dvt1      = 2          dvt2      = -0.032
+ dvt0w     = 0           dvt1w     = 0          dvt2w     = 0
+ dsub      = 0.1         minv      = 0.05       voffl     = 0
+ dvtp0     = 1e-011      dvtp1     = 0.05       lpe0      = 0
+ lpeb      = 0           xj        = 1.4e-008   ngate     = 1e+023
+ ndep      = 2.44e+018   nsd       = 2e+020     phin      = 0
+ cdsc      = 0           cdscb     = 0          cdscd     = 0
+ cit       = 0           voff      = -0.126     nfactor   = 2.1
+ eta0      = 0.0055      etab      = 0          vfb       = 0.55
+ u0        = 0.02        ua        = 2e-009     ub        = 5e-019
+ uc        = 0           vsat      = 150000     a0        = 1
+ ags       = 1e-020      a1        = 0          a2        = 1
+ b0        = 0           b1        = 0          keta      = -0.047
+ dwg       = 0           dwb       = 0          pclm      = 0.12
+ pdiblc1   = 0.001       pdiblc2   = 0.001      pdiblcb   = 3.4e-008
+ drout     = 0.56        pvag      = 1e-020     delta     = 0.01
+ pscbe1    = 8.14e+008   pscbe2    = 9.58e-007  fprout    = 0.2
+ pdits     = 0.08        pditsd    = 0.23       pditsl    = 2300000
+ rsh       = 5           rdsw      = 155        rsw       = 75
+ rdw       = 75          rdswmin   = 0          rdwmin    = 0
+ rswmin    = 0           prwg      = 0          prwb      = 0
+ wr        = 1           alpha0    = 0.074      alpha1    = 0.005
+ beta0     = 30          agidl     = 0.0002     bgidl     = 2.1e+009
```

+ cgidl	= 0.0002	egidl	= 0.8	aigbacc	= 0.012
+ bigbacc	= 0.0028	cigbacc	= 0.002	nigbacc	= 1
+ aigbinv	= 0.014	bigbinv	= 0.004	cigbinv	= 0.004
+ eigbinv	= 1.1	nigbinv	= 3	aigc	= 0.010687
+ bigc	= 0.0012607	cigc	= 0.0008	aigsd	= 0.010687
+ bigsd	= 0.0012607	cigsd	= 0.0008	nigc	= 1
+ poxedge	= 1	pigcd	= 1	ntox	= 1
+ xrcrg1	= 12	xrcrg2	= 5	cgso	= 1.1e-010
+ cgdo	= 1.1e-010	cgbo	= 2.56e-011	cgdl	= 2.653e-010
+ cgsl	= 2.653e-010	ckappas	= 0.03	ckappad	= 0.03
+ acde	= 1	moin	= 15	noff	= 0.9
+ voffcv	= 0.02	kt1	= -0.11	kt1l	= 0
+ kt2	= 0.022	ute	= -1.5	ua1	= 4.31e-009
+ ub1	= 7.61e-018	uc1	= -5.6e-011	prt	= 0
+ at	= 33000	fnoimod	= 1	tnoimod	= 0
+ jss	= 0.0001	jsws	= 1e-011	jswgs	= 1e-010
+ njs	= 1	ijthsfwd	= 0.01	ijthsrev	= 0.001
+ bvs	= 10	xjbvs	= 1	jsd	= 0.0001
+ jswd	= 1e-011	jswgd	= 1e-010	njd	= 1
+ ijthdfwd	= 0.01	ijthdrev	= 0.001	bvd	= 10
+ xjbvd	= 1	pbs	= 1	cjs	= 0.0005
+ mjs	= 0.5	pbsws	= 1	cjsws	= 5e-010
+ mjsws	= 0.33	pbswgs	= 1	cjswgs	= 3e-010
+ mjswgs	= 0.33	pbd	= 1	cjd	= 0.0005
+ mjd	= 0.5	pbswd	= 1	cjswd	= 5e-010
+ mjswd	= 0.33	pbswgd	= 1	cjswgd	= 5e-010
+ mjswgd	= 0.33	tpb	= 0.005	tcj	= 0.001
+ tpbsw	= 0.005	tcjsw	= 0.001	tpbswg	= 0.005
+ tcjswg	= 0.001	xtis	= 3	xtid	= 3
+ dmcg	= 0	dmci	= 0	dmdg	= 0
+ dmcgt	= 0	dwj	= 0	xgw	= 0
+ xgl	= 0	rshg	= 0.4	gbmin	= 1e-010
+ rbpb	= 5	rbpd	= 15	rbps	= 15
+ rbdb	= 15	rbsb	= 15	ngcon	= 1

Table 13: SOI NMOSFET model from the BSIMSOI Benchmarking Suite [44]

```
* BSIMSOI4.5 example modelcard
.model nmossoi bsimsoi version = 4.5
+ type      = 1           binunit    = 1            mobmod     = 1
+ capmod    = 3           shmod      = 0            paramchk   = 0
+ soimod    = 0           igcmod     = 1            igbmod     = 1
+ tsi       = 9e-008      tox        = 2e-009       toxref     = 2e-9
+ tbox      = 4e-007      toxqm      = 2e-009       tnom       = 27
+ rbody     = 0           rbsh       = 0            rsh        = 0
+ dtoxcv    = 0           xj         = 7e-008       rhalo      = 0
+ nch       = 1.7e+017    ngate      = 3e+020       wint       = 5.5544e-9
+ lint      = 2e-009      xpart      = 1            toxm       = 2e-009
+ k1        = 0.6         k2         = 1e-010       k3         = 0.231
+ k3b       = 0           kb1        = 1            w0         = 0
+ dvt0      = 2.2         dvt1       = 0.53         dvt2       = 0.127
+ dvt0w     = 0           dvt1w      = 0            dvt2w      = 0
+ eta0      = 1.7958      etab       = -0.07        dsub       = 1.7577
+ voff      = -0.10382    nfactor    = 1            cdsc       = 0.00024
+ cdscb     = 0           cdscd      = 0            cit        = 0
+ u0        = 200         ua         = 2.25e-009    ub         = 5.9e-019
+ uc        = 2.9e-011    prwg       = 2.5          prwb       = 0.76
+ wr        = 1           rdsw       = 0.695        a0         = 0
+ ags       = 0           a1         = 0            a2         = 0.7
+ b0        = 0           b1         = 0            vsat       = 99820
+ keta      = 0           ketas      = 0            dwg        = 0
+ dwb       = 0           dwbc       = 0            pclm       = 1.3
+ pdiblc1   = 0.39        pdiblc2    = 0.05         pdiblcb    = 0.89459
+ drout     = 2           pvag       = 0.116        delta      = 0.01
+ vevb      = 0.075       vecb       = 0.026        alpha0     = 5.0707e-9
+ beta0     = 0.0007605   beta1      = 0.0002767    beta2      = 0.094512
+ alphagb1  = 0.35        alphagb2   = 0.43         betagb1    = 0.03
+ betagb2   = 0.05        fbjtii     = 0            vdsatii0   = 0.72051
+ tii       = -0.5062     lii        = 2.835e-009   esatii     = 2213500
+ sii0      = 2.0387      sii1       = 0.04093      sii2       = 9.8e-011
+ siid      = 0.008025    aigc       = 1            bigc       = 0.05022
+ cigc      = 0.075       aigsd      = 0.43         bigsd      = 0.054
+ cigsd     = 0.075       nigc       = 1            poxedge    = 1
+ pigcd     = 1           agidl      = 0            bgidl      = 0
+ ebg       = 1.2         vgb1       = 300          vgb2       = 17
+ voxh      = 1.5         deltavox   = 0.004        ntox       = 1
+ ntun      = 1           ndiode     = 1            nrecf0     = 1.5
```

+ nrecr0	= 2	isbjt	= 1e-006	isdif	= 0.0001
+ isrec	= 0.01	istun	= 5e-005	vrec0	= 1
+ vtun0	= 0	nbjt	= 0.7888	lbjt0	= 1.4381e-6
+ vabjt	= 0.001	aely	= 1.0819e+010	ahli	= 0
+ lpe0	= 3e-009	cjswg	= 1e-010	mjswg	= 0.5
+ pbswg	= 0.7	tt	= 4e-010	ldif0	= 1
+ cgso	= 5e-011	cgdo	= 5e-011	dlc	= 0
+ dwc	= 0	dlcb	= 0	dlbg	= 0
+ fbody	= 1	clc	= 1e-008	cle	= 0
+ cf	= 0	csdmin	= 0	asd	= 0.3
+ csdesw	= 8.73e-011	delvt	= -0.031456	acde	= 1
+ moin	= 25	ckappa	= 3.2309	cgdl	= 1.5533e-10
+ cgsl	= 1.5533e-010	ndif	= -1	kt1	= -0.11573
+ kt1l	= -4e-010	kt2	= -0.25	ute	= -1.2189
+ ua1	= 5.005e-012	ub1	= -8.835e-019	uc1	= -6e-11
+ prt	= 51.149	rth0	= 0.02	cth0	= 1e-005
+ at	= 8479	tpbswg	= 5.86e-005	tcjswg	= 9.2578e-4
+ ntrecf	= -0.55338	ntrecr	= -0.15688	xbjt	= 1.0968
+ xdif	= 1.4551	xrec	= 2.6e-011	xtun	= 25.308
+ fnoimod	= 0	tnoimod	= 2	af	= 2.15
+ ef	= 1.119	kf	= 1.67e-026	w0flk	= 0.001

Table 14: SOI PMOSFET model from the BSIMSOI Benchmarking Suite [44]

```
* BSIMSOI4.5 example modelcard
.model pmossoi bsimsoi version = 4.5
+ type      = -1          binunit   = 1           mobmod    = 1
+ capmod    = 3           shmod     = 0           paramchk  = 0
+ soimod    = 0           igcmod    = 1           igbmod    = 1
+ tsi       = 9e-008      tox       = 2e-009      toxref    = 2e-9
+ tbox      = 4e-007      toxqm     = 2e-009      tnom      = 27
+ rbody     = 0           rbsh      = 0           rsh       = 0
+ dtoxcv    = 0           xj        = 7e-008      rhalo     = 0
+ nch       = 1.7e+017    ngate     = 3e+020      wint      = 5.5544e-9
+ lint      = 2e-009      xpart     = 1           toxm      = 2e-009
+ k1        = 0.6         k2        = 1e-010      k3        = 0.231
+ k3b       = 0           kb1       = 1           w0        = 0
+ dvt0      = 2.2         dvt1      = 0.53        dvt2      = 0.127
+ dvt0w     = 0           dvt1w     = 0           dvt2w     = 0
+ eta0      = 1.7958      etab      = -0.07       dsub      = 1.7577
+ voff      = -0.10382    nfactor   = 1           cdsc      = 0.00024
+ cdscb     = 0           cdscd     = 0           cit       = 0
+ u0        = 200         ua        = 2.25e-009   ub        = 5.9e-019
+ uc        = 2.9e-011    prwg      = 2.5         prwb      = 0.76
+ wr        = 1           rdsw      = 0.695       a0        = 0
+ ags       = 0           a1        = 0           a2        = 0.7
+ b0        = 0           b1        = 0           vsat      = 99820
+ keta      = 0           ketas     = 0           dwg       = 0
+ dwb       = 0           dwbc      = 0           pclm      = 1.3
+ pdiblc1   = 0.39        pdiblc2   = 0.05        pdiblcb   = 0.89459
+ drout     = 2           pvag      = 0.116       delta     = 0.01
+ vevb      = 0.075       vecb      = 0.026       alpha0    = 5.0707e-9
+ beta0     = 0.0007605   beta1     = 0.0002767   beta2     = 0.094512
+ alphagb1  = 0.35        alphagb2  = 0.43        betagb1   = 0.03
+ betagb2   = 0.05        fbjtii    = 0           vdsatii0  = 0.72051
+ tii       = -0.5062     lii       = 2.835e-009  esatii    = 2213500
+ sii0      = 2.0387      sii1      = 0.04093     sii2      = 9.8e-011
+ siid      = 0.008025    aigc      = 1           bigc      = 0.05022
+ cigc      = 0.075       aigsd     = 0.43        bigsd     = 0.054
+ cigsd     = 0.075       nigc      = 1           poxedge   = 1
+ pigcd     = 1           agidl     = 0           bgidl     = 0
+ ebg       = 1.2         vgb1      = 300         vgb2      = 17
+ voxh      = 1.5         deltavox  = 0.004       ntox      = 1
+ ntun      = 1           ndiode    = 1           nrecf0    = 1.5
+ nrecr0    = 2           isbjt     = 1e-006      isdif     = 0.0001
```

+ isrec	= 0.01	istun	= 5e-005	vrec0	= 1
+ vtun0	= 0	nbjt	= 0.7888	lbjt0	= 1.4381e-6
+ vabjt	= 0.001	aely	= 1.0819e+010	ahli	= 0
+ lpe0	= 3e-009	cjswg	= 1e-010	mjswg	= 0.5
+ pbswg	= 0.7	tt	= 4e-010	ldif0	= 1
+ cgso	= 5e-011	cgdo	= 5e-011	dlc	= 0
+ dwc	= 0	dlcb	= 0	dlbg	= 0
+ fbody	= 1	clc	= 1e-008	cle	= 0
+ cf	= 0	csdmin	= 0	asd	= 0.3
+ csdesw	= 8.73e-011	delvt	= -0.031456	acde	= 1
+ moin	= 25	ckappa	= 3.2309	cgdl	= 1.5533e-10
+ cgsl	= 1.5533e-010	ndif	= -1	kt1	= -0.11573
+ kt1l	= -4e-010	kt2	= -0.25	ute	= -1.2189
+ ua1	= 5.005e-012	ub1	= -8.835e-019	uc1	= -6e-11
+ prt	= 51.149	rth0	= 0.02	cth0	= 1e-005
+ at	= 8479	tpbswg	= 5.86e-005	tcjswg	= 9.2578e-4
+ ntrecf	= -0.55338	ntrecr	= -0.15688	xbjt	= 1.0968
+ xdif	= 1.4551	xrec	= 2.6e-011	xtun	= 25.308
+ fnoimod	= 0	tnoimod	= 2	af	= 2.15
+ ef	= 1.119	kf	= 1.67e-026	w0flk	= 0.001

Table 15: Mextram NPN BJT model using default model parameters [41], [42], [43]

```
* Mextram example modelcard
.model npn504 npn LEVEL = 6
+ VERS    = 504        TREF    = 25         DTA     = 0
+ EXMOD   = 1          EXPHI   = 1          EXAVL   = 0
+ EXSUB   = 0          IS      = 2.20E-17   IK      = 0.1
+ VER     = 2.5        VEF     = 44         BF      = 215
+ IBF     = 2.70E-15   MLF     = 2          XIBI    = 0
+ IZEB    = 0          NZEB    = 22         BRI     = 7
+ IBR     = 1.00E-15   VLR     = 0.2        XEXT    = 0.63
+ WAVL    = 1.10E-06   VAVL    = 3          SFH     = 0.3
+ RE      = 5          RBC     = 23         RBV     = 18
+ RCC     = 12         RCBLX   = 0          RCBLI   = 0
+ RCV     = 150        SCRCV   = 1250       IHC     = 4.00E-03
+ AXI     = 0.3        CJE     = 7.30E-14   VDE     = 0.95
+ PE      = 0.4        XCJE    = 0.4        CBEO    = 0
+ CJC     = 7.80E-14   VDC     = 0.68       PC      = 0.5
+ XP      = 0.35       MC      = 0.5        XCJC    = 3.20E-02
+ CBCO    = 0          MTAU    = 1          TAUE    = 2.00E-12
+ TAUB    = 4.20E-12   TEPI    = 4.10E-11   TAUR    = 5.20E-10
+ DEG     = 0          XREC    = 0          XQB     = 0.33
+ AQBO    = 0.3        AE      = 0          AB      = 1
+ AEPI    = 2.5        AEX     = 0.62       AC      = 2
+ ACBL    = 2          DAIS    = 0          DVGBF   = 5.00E-02
+ DVGBR   = 4.50E-02   VGB     = 1.17       VGC     = 1.18
+ VGJ     = 1.15       VGZEB   = 1.15       AVGEB   = 4.73E-04
+ TVGEB   = 636        DVGTE   = 0.05       AF      = 2
+ KF      = 2.00E-11   KFN     = 2.00E-11   KAVL    = 0
+ KC      = 0          ISS     = 4.80E-17   ICSS    = -1
+ IKS     = 2.50E-04   CJS     = 3.15E-13   VDS     = 0.62
+ PS      = 0.34       VGS     = 1.2        AS      = 1.58
+ ASUB    = 2          RTH     = 300        CTH     = 3.00E-09
+ ATH     = 0          MULT    = 1
```

Table 16: SPICE component based implementation of the bias-dependent single-event current source patterned after Fig. 8 [27]

```
* Copyright Jeff Kauppila and the Institute for Space and Defense Electronics
*   at Vanderbilt University (c) 2015, All Rights Reserved
*
* Publications utilizing this should reference the original IEEE TNS Paper:
* Kauppila, J.S.; Sternberg, A.L.; Alles, M.L.; Francis, A.M.; Holmes, J.;
*   Amusan, O.A.; Massengill, L.W.; , "A Bias-Dependent Single-Event Compact
*   Model Implemented Into BSIM4 and a 90 nm CMOS Process Design Kit,"
*   Nuclear Science, IEEE Transactions on , vol.56, no.6, pp.3152-3157, Dec. 2009
*   doi: 10.1109/TNS.2009.2033798
***********************Bias Dependent SET Model************************
.subckt Bias_Dep_SET n p see_tau1=0.5e-12 see_tau2=70e-12
+ see_start_time=1e-6 see_duration=1.5e-12 see_let=40 see_col_len=1.5e-6
+ see_recomb=1E11
.param F=0.05 CS=1e-9
.param IMAX='(see_let*1.035E-2*see_col_len*1E6*1E-12)/((see_duration +
+ see_tau2 - see_tau1)-(see_tau2-see_tau1)*exp(-1*(see_duration/see_tau1)))'
.param DELAY='see_start_time+see_duration'
* IMAX from equation in Massengill 1993 IEEE NSREC Short Course
*   see_let = LET Value in MeV-cm^2/mg
*   1.035E-2 is constant to go from LET to pC/um
*   see_col_len is the collection length in meters
*   1E6 converts to micro-meters
*   1E-12 converts to Coulombs
*
* The following components represent the items in the schematic representation
*   presented in the above referenced IEEE TNS paper
CHOLD VC 0 'CS'
IEXPSEE 0 VC EXP (0 IMAX see_start_time see_tau1 DELAY see_tau2)
GRECOMB VC 0 CUR='V(VC)*CS*see_recomb'
GSEE VC 0 CUR='V(VC)*(CS/see_tau1)*(1.0/(1.0+exp((V(p)-V(n)+3*F)/F)))'
GSEEP n p CUR='V(VC)*(CS/see_tau1)*(1.0/(1.0+exp((V(p)-V(n)+3*F)/F)))'
.ends Bias_Dep_SET
```

Appendix C

COMPACT MODEL INTEGRATION EXAMPLES

This Appendix contains examples of radiation-enabled models, specifically the subcircuit development methods, and a layout-aware netlist. Integration routines for including the radiation-enabled models in the Cadence Analog Design Environment graphical user interface (GUI) is also included. The SPICE transistor models referenced in this Appendix are detailed in Appendix B.

Mextram NPN BJT Radiation-Enabled Compact Model

Table 17 demonstrates the methods for modifying a Mextram BJT model for use with transient-radiation-enabled models. Specifically, the development of the collector, base, and emitter resistors using the modeling equations and temperature dependencies from the Mextram model [41]. Conductivity modulation in the resistors and the generation of transient currents is handled by the behavioral model npn_rad. In addition to modifications in the subcircuit in Table 17, the model file in Table 15 will need to be modified by setting resistor parameters to zero. Comments within the code presented in Table 17 can be used as a guide to specific parameter modification needs.

Table 17: Radiation-enabled subcircuit with Mextram resistors placed external to the NPN BJT model. The subcircuit references the NPN model from Table 15 in Appendix B.

```
**************************************************************
* This file contains material that is developed and maintained
```

```
* by the Institute for Space and Defense Electronics (ISDE) at
* Vanderbilt University
****************************************************************
* File: npn_rad_sub.scs
* Description: Rad. Model file for Mextram NPN BJT transistor.
****************************************************************
* Copyright (c) 2015 Jeff Kauppila, Institute for Space and
* Defense Electronics, All Rights Reserved
****************************************************************
inline subckt npn_rad_sub (C B E dt)
parameters area=1 le=4 we=4 T0=0 RLevel=0 Width=0
+ baselen=16 basewid=10 tubl=40 tubw=20
********************Begin RAD Insertion**************************
* Add the default temperature scaling parameters for Mextram
* Constant R's after all subckt parameters
parameters dta=0.0 ac=2.0 aex=0.62 aepi=2.5 ae=0.0 ab=1.0
+ rcc=12 rcv=150 rbc=23 re=5

rcc C Ci resistor r=rcc*(((temp+dta+273.15+v(dt))/
+ (tref+273.15))**ac)+0.5*rcv*(((temp+dta+273.15+v(dt))/
+ (tref+273.15))**aepi)
rbc B Bi resistor r=rbc*(((temp+dta+273.15+v(dt))/
+ (tref+273.15))**aex)
re E Ei resistor r=re*(((temp+dta+273.15+v(dt))/
+ (tref+273.15))**ae)
npn_rad_sub Ci Bi Ei dt npn504 area=area
npn_rad C Ci B Bi E Ei dt npn_rad le=le we=we bjttherm=1
+ rcc=rcc+0.9*rcv rcv=rcv baselen=baselen basewid=basewid
+ tubl=tublen tubw=tubwid temp=temp tref=tref dta=dta ac=ac
+ area=area T0=T0 RLevel=RLevel Width=Width
* NPN Model File Modification Needs
* Zero out the rcc, rbc, and re resistors in the SPICE models
* Scale rcv by 1-X, where X is the scale factor used above (0.5)
********************End RAD Insertion****************************
ends npn_rad_sub
```

Bulk NMOSFET Single-Event Enabled Compact Model

The single-event enabled subcircuit for an bulk NMOSFET is shown in Table 18. The methods for externalizing the drain, source, and body resistors are shown and

follow the equations for the BSIM4 MOSFET model [38]. The n_see instance is the behavioral model for transient current generation. In addition to modifications in the subcircuit in Table 18, the model file in Table 11 will need to be modified by setting resistor parameters to zero. Comments within the code presented in Table 18 can be used as a guide to specific parameter modification needs. The development of a bulk PMOSFET single-event enabled model would follow similar methods.

Table 18: Single-event enabled bulk NMOSFET subcircuit with resistors placed external to the MOSFET model. The subcircuit references the NMOSFET model from Table 11 in Appendix B [38].

```
***************************************************************
* This file contains material that is developed and maintained
* by the Institute for Space and Defense Electronics (ISDE) at
* Vanderbilt University
***************************************************************
* File: nmosfet_see.scs
* Description: Rad. Model file for Bulk NMOSFET device.
***************************************************************
* Copyright (c) 2015 Jeff Kauppila, Institute for Space and
* Defense Electronics, All Rights Reserved
***************************************************************
inline subckt nmosfet_see (D G S B)
parameters w=104n l=40n start=0 tau1=0.5p tau2=70p
+ duration=2p let=0 dist=0
********************Begin RAD Insertion*************************
* Resistor implementation does not include temp coefficients
* RDSMOD=0 and RBODYMOD=1 - See BSIM4 Resistor Calcs. in Manual
* Model parameters of RDSWMIN, PRWB, and PRWG=0 simplify RDS Calc.
parameters rdsw=155 rbps=15 rbpd=15 rbsb=15 rbdb=15 rbpb=5

rd D Di resistor r=rdsw/(1E6*w)
rs S Si resistor r=rdsw/(1E6*w)
*RB Network, RBODYMOD=1 no Resistor Scaling (RBODYMOD=2 Scales R)
rbps Si Bi resistor r=rdps
rbpd Di Bi resistor r=rbpd
rbpb Bi B resistor r=rbpb
rbsb Si B resistor r=rbsb
rbdb Di B resistor r=rbdb
```

```
nmosfet_see Di G Si Bi nmos w=w l=l
n_see Di Si Bi n_see w=w l=l start=start tau1=tau1
+ tau2=tau2 duration=duration let=let dist=dist
* NMOSFET Model File Modification Needs
* Zero out the rdsw, rbps, rbpd, rbpb, rbsb, rbdb in SPICE models
********************End RAD Insertion****************************
ends nmosfet_see
```

SOI CMOS Single-Event Enabled Compact Model

The single-event enabled subcircuit for a SOI NMOSFET is shown in Table 19. The methods for externalizing the bias-dependent drain and source resistors are shown and follow the equations for the BSIMSOI MOSFET model [44]. The n_soi_see instance is the behavioral model for transient current generation and parasitic BJT amplification. In addition to modifications in the subcircuit in Table 19, the model file in Table 13 will need to be modified by setting resistor parameters to zero. Comments within the code presented in Table 19 can be used as a guide to specific parameter modification needs. The development of a SOI PMOSFET single-event enabled model would follow similar methods.

Table 19: Single-event enabled SOI NMOSFET subcircuit with resistors placed external to the MOSFET model. The subcircuit references the SOI NMOSFET model from Table 13 in Appendix B [44].

```
***************************************************************
* This file contains material that is developed and maintained
* by the Institute for Space and Defense Electronics (ISDE) at
* Vanderbilt University
***************************************************************
* File: nmosfet_soi_see.scs
* Description: Rad. Model file for Floating Body SOI NMOSFET.
***************************************************************
```

```
* Copyright (c) 2015 Jeff Kauppila, Institute for Space and
* Defense Electronics, All Rights Reserved
*******************************************************************
inline subckt nmosfet_soi_see (D G S Sub)
parameters w=104n l=40n start=0 tau1=0.5p tau2=70p
+ duration=2p let=0
********************Begin RAD Insertion**************************
* Resistor implementation does not include temp coefficients
* RDSMOD=0 and RBODYMOD=0 - See BSIMSOI Resistor Calcs. in Manual
*
parameters rdsw=0.695 prwg=2.5 prwb=0.76 nch=1.7E17
+phi=2*0.026*log(nch/1.45E10)

if (v(Bi,Si) >= 0.95*phi) {
rd D Di resistor r=rdsw*(1+prwg*v(G,Si)+prwb*(sqrt(0.05*phi)
+ -sqrt(phi)))/(1E6*w)
rd S Si resistor r=rdsw*(1+prwg*v(G,Si)+prwb*(sqrt(0.05*phi)
+ -sqrt(phi)))/(1E6*w)
} else {
rd D Di resistor r=rdsw*(1+prwg*v(G,Si)+prwb*(sqrt(phi-v(Bi,Si))
+ -sqrt(phi)))/(1E6*w)
rd S Si resistor r=rdsw*(1+prwg*v(G,Si)+prwb*(sqrt(phi-v(Bi,Si))
+ -sqrt(phi)))/(1E6*w)
}
*Simplified Approx of RDS = rdsw*(1+prwg*v(G,Si))/(1E6*w)
*RB Network, RBODYMOD=0 no body resistor
nmosfet_soi_see Di G Si Sub nc Bi nmos w=w l=l
n_soi_see Di Si Bi n_soi_see w=w l=l start=start tau1=tau1
+ tau2=tau2 duration=duration let=let
* NMOSFET Model File Modification Needs
* Zero out the rdsw in SPICE models
********************End RAD Insertion****************************
ends nmosfet_see
```

Sample Layout-Aware Single-Event Analysis Netlist

The layout-aware analysis methods discussed in Chapter VI are demonstrated here with two example netlists. Table 20 shows a layout-aware enabled netlist for a D-flip-flop (DFF). Table 22 shows a layout-aware enabled netlist for the operational

amplifier discussed in Appendix A and shown in Fig. 69. Each of the netlists include standard MOSFET models used in the design of the circuit, and single-event enabled models for those transistors within the region of potential charge sharing, as discussed in Chapters V and VI. In addition to showing portions of the simulation netlist, the control and result extraction commands are also included, targeted to the Spectre circuit simulator from Cadence [62]. The netlists are automatically generated from scripts that extract information from the layout and parameterize the models with spatial information [54]. The strike location in (X,Y) coordinates is saved by setting the DC value of a voltage source, VX and VY, and extracting that voltage to the output file. The LET value for the simulation is also extracted in a similar manner. The output signal is measured using in-line OCEAN commands, which is possible when using MonteCarlo simulation methods. The MonteCarlo simulation is set to run the nominal case only, and it sweeps through a list of parameter values for the LET. The output for each LET simulation is recorded to the output file. Demonstration output files are included in Tables 21 and 23.

Table 20: Layout aware netlist for a DFF [54]. The netlist shows the setup for the voltage sources, the transistors, and the commands to extract the results from the circuit and store them in a text file. The netlist uses the MonteCarlo function (nominal devices only) to achieve the parameter sweep capability. The models are based on those presented in Table 18.

```
//************************************************************
// Example DFF Layout Aware Netlist
// Automatically Generated Netlist
// X,Y Location (3750,400)
// Jeff Kauppila, Copyright (c) 2015, All Rights Reserved
// Generated for: spectre
simulator lang=spectre
parameters LET=0
include "nmosfet_see.scs"
```

```
include "pmosfet_see.scs"
//Start the voltage sources
V2 (D 0) vsource type=dc dc=0.9
V3 (CLK 0) vsource type=pulse val0=0 val1=0.9 delay=0.5n rise=10p \
  fall=10p width=0.5n period=1
V1 (VDD 0) vsource dc=0.9 type=dc
V0 (VSS 0) vsource dc=0 type=dc
//End Voltage Sources

//Begin CIRCUIT
XM0 (1 CLK VSS 63) nmos l=4e-08 w=1.55e-07 ad=3.465e-14 \
  as=1.705e-14 pd=5.3e-07 ps=1.36e-06 nrd=0.70968 \
  nrs=4.6902 sd=1.4e-07 sa=2.9e-07 sb=1.1e-07
XM3 (5 D 19 63) nmos l=4e-08 w=3.1e-07 ad=2.17e-14 \
  as=2.17e-14 pd=7.6e-07 ps=7.6e-07 nrd=0.22581 \
  nrs=0.22581 sd=1.4e-07 sa=2.9e-07 sb=6.5e-07

<OTHER TRANSISTORS IN THE CIRCUIT>

//SEE Enabled NMOSFET Devices in Charge Sharing Region
XM5 (21 7 20 63) nmosfet_see l=4e-08 w=1.2e-07 ad=8.4e-15 \
  as=8.4e-15 pd=3.8e-07 ps=3.8e-07 nrd=0.58333 \
  nrs=0.58333 sd=1.4e-07 sa=6.5e-07 sb=2.9e-07 \
  dist=470.0 let=LET tau1=0.5e-12 tau2=70e-12 \
  duration=2E-12
XM6 (21 12 VSS 63) nmosfet_see l=4e-08 w=1.2e-07 ad=4.64e-14 \
  as=8.4e-15 pd=3.8e-07 ps=1.45e-06 nrd=0.58333 \
  nrs=3.1619 sd=1.4e-07 sa=1.1e-07 sb=8.3e-07 \
  dist=320.0 let=LET tau1=0.5e-12 tau2=70e-12 \
  duration=2E-12
XM7 (7 5 VSS 63) nmosfet_see l=4e-08 w=1.5e-07 ad=1.65e-14 \
  as=4.97e-14 pd=5.2e-07 ps=1.51e-06 nrd=0.73333 \
  nrs=2.9785 sd=1.4e-07 sa=1.1e-07 sb=1.1e-07 \
  dist=80.0 let=LET tau1=0.5e-12 tau2=70e-12 \
  duration=2E-12
XM8 (8 4 7 63) nmosfet_see l=4e-08 w=1.5e-07 ad=1.05e-14 \
  as=1.65e-14 pd=4.4e-07 ps=5.2e-07 nrd=0.46667 \
  nrs=0.73333 sd=1.4e-07 sa=1.1e-07 sb=4.7e-07 \
  dist=40.0 let=LET tau1=0.5e-12 tau2=70e-12 \
  duration=2E-12
XM9 (22 1 8 63) nmosfet_see l=4e-08 w=1.2e-07 ad=8.4e-15 \
  as=8.4e-15 pd=3.8e-07 ps=3.8e-07 nrd=0.58333 \
  nrs=0.58333 sd=1.4e-07 sa=2.9e-07 sb=2.9e-07 \
  dist=230.0 let=LET tau1=0.5e-12 tau2=70e-12 \
```

```
  duration=2E-12
XM10 (22 9 VSS 63) nmosfet_see l=4e-08 w=1.2e-07 ad=4.64e-14 \
  as=8.4e-15 pd=3.8e-07 ps=1.45e-06 nrd=0.58333 \
  nrs=3.1619 sd=1.4e-07 sa=1.1e-07 sb=4.7e-07 \
  dist=410.0 let=LET tau1=0.5e-12 tau2=70e-12 \
  duration=2E-12

//PMOS DEVICES
XM15 (1 CLK VDD 64) pmos l=4e-08 w=2.05e-07 ad=3.815e-14 \
  as=2.255e-14 pd=6.3e-07 ps=1.46e-06 nrd=0.53659 \
  nrs=4.5801 sd=1.4e-07 sa=2.9e-07 sb=1.1e-07
XM18 (5 D 17 64) pmos l=4e-08 w=3.4e-07 ad=2.38e-14 \
  as=2.38e-14 pd=8.2e-07 ps=8.2e-07 nrd=0.20588 \
  nrs=0.20588 sd=1.4e-07 sa=2.9e-07 sb=4.7e-07

<OTHER TRANSISTORS IN THE CIRCUIT>

//SEE Enabled PMOSFET Devices in Charge Sharing Region
XM21 (6 12 VDD 64) pmosfet_see l=4e-08 w=1.2e-07 ad=4.64e-14 \
  as=1.32e-14 pd=4.6e-07 ps=1.45e-06 nrd=0.91667 \
  nrs=3.1619 sd=1.4e-07 sa=1.1e-07 sb=1.1e-07 \
  dist=500.0 let=LET tau1=0.5e-12 tau2=70e-12 \
  duration=2E-12
XM22 (7 5 VDD 64) pmosfet_see l=4e-08 w=1.8e-07 ad=1.98e-14 \
  as=5.3e-14 pd=5.8e-07 ps=1.57e-06 nrd=0.61111 \
  nrs=2.8563 sd=1.4e-07 sa=1.1e-07 sb=1.1e-07 \
  dist=460.0 let=LET tau1=0.5e-12 tau2=70e-12 \
  duration=2E-12
XM23 (8 1 7 64) pmosfet_see l=4e-08 w=1.8e-07 ad=1.26e-14 \
  as=1.98e-14 pd=5e-07 ps=5.8e-07 nrd=0.38889 \
  nrs=0.61111 sd=1.4e-07 sa=1.1e-07 sb=4.7e-07 \
  dist=497.0 let=LET tau1=0.5e-12 tau2=70e-12 \
  duration=2E-12

<REMAINING TRANSISTORS>

//End CIRCUIT
//Setup Well Resistances
//Based on 30um contact worst case
RNwell (64 VDD) resistor r=5k
RPwell (63 0) resistor r=500
//Start output file designation sources
VX (x 0) vsource type=dc dc=3570 //Value passed from script
VY (y 0) vsource type=dc dc=400 //Value passed from script
```

```
VLET (swlet 0) vsource type=dc dc=LET
//End sources
//Start Simulation Control Options
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 \
  temp=27 tnom=25 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
  maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
  checklimitdest=psf
mc1 montecarlo numruns=1 donominal=no scalarfile="output.txt" {
sweep1 sweep param=LET values=[0.5 0.6 0.7 0.8 1 3 6 11 20 28] {
  tran tran stop=10n \
  annotate=status maxiters=5
  export LET=oceanEval("value(v(\"swlet\" ?result \"tran\" ) \
        1e-9)")
  export FLIP=oceanEval("int(abs(value(v(\"Q\" ?result \"tran\" ) \
        1e-9)-value(v(\"Q\" ?result \"tran\" ) 3E-9))+0.5)")
  export X=oceanEval("value(v(\"x\" ?result \"tran\" ) 1e-9)")
  export Y=oceanEval("value(v(\"y\" ?result \"tran\" ) 1e-9)")
  }
}
save Q swlet x y
```

Table 21: Example output file, output.txt, from the layout-aware netlist shown in Table 20 [54]. The table header is for reference, the actual file contains no headers to ease parsing of results. A zero in the FLIP column is no-upset and a one is an upset.

LET (MeV-cm^2/mg)	FLIP	X Location	Y Location
0.5	0	3750	400
0.6	1	3750	400
0.7	1	3750	400
0.8	1	3750	400
1	1	3750	400
3	1	3750	400
6	1	3750	400
9	1	3750	400
11	1	3750	400
13	1	3750	400
16	1	3750	400
20	1	3750	400
28	1	3750	400

Table 22: Layout aware netlist for the operational amplifier shown in Fig. 69, specifically the PMOSFET input devices [51], [52]. The netlist shows the setup for the voltage sources, the transistors, and the commands to extract the results from the circuit and store them in a text file. The netlist uses the MonteCarlo function (nominal devices only) to achieve the parameter sweep capability. The models are based on the methods presented in Table 18.

```
//************************************************************
// Example OpAmp Layout Aware Netlist
// Automatically Generated Netlist
// X,Y Location (-250,280)
// Jeff Kauppila, Copyright (c) 2015, All Rights Reserved
// Generated for: spectre
simulator lang=spectre
parameters LET=0
include "nmosfet_see.scs"
include "pmosfet_see.scs"
//************************************************************
//Bias Circuit
<BIAS CIRCUIT MOSFETS >
//************************************************************
//Input Pair N
TN4 (ndp inp ns subt) nmos l=500n w=2.25u nf=1 ad=1.04p \
  as=1.04p pd=5.42u ps=5.42u nrd=0.1156 nrs=0.1156 gcon=1 \
  lstis=1 sa=460.00n sb=460.00n sd=0 rsx=50 dtemp=0
TN7 (ndm inm ns subt) nmos l=500n w=2.25u nf=1 ad=1.04p \
  as=1.04p pd=5.42u ps=5.42u nrd=0.1156 nrs=0.1156 gcon=1 \
  lstis=1 sa=460.00n sb=460.00n sd=0 rsx=50 dtemp=0
<ADDITIONAL INPUT NMOSFETS >
//************************************************************
//Input Pair P
XM9 (ps inm pdm see_nwell) pmos l=5e-07 w=8.5e-06 ad=3.91e-12 \
  as=3.91e-12 pd=1.792e-05 ps=1.792e-05 nrd=0.054118 \
  nrs=0.054118 sd=0 sa=4.6e-07 sb=4.6e-07
XM10 (ps inp pdp see_nwell) pmos l=5e-07 w=8.5e-06 ad=3.91e-12 \
  as=3.91e-12 pd=1.792e-05 ps=1.792e-05 nrd=0.054118 \
  nrs=0.054118 sd=0 sa=4.6e-07 sb=4.6e-07
<ADDITIONAL INPUT PMOSFETS >

// Single-Event Impacted PMOSFETS
XM17 (pdp inp ps see_nwell) pmos_see l=5e-07 w=8.5e-06 ad=3.91e-12 \
  as=3.91e-12 pd=1.792e-05 ps=1.792e-05 nrd=0.054118 \
  nrs=0.054118 sd=0 sa=4.6e-07 sb=4.6e-07 \
```

```
  dist=85.0 let=LET tau1=1.5e-12 tau2=100e-12 \
  duration=4.5E-12
XM23 (ps inp pdp see_nwell) pmos_see l=5e-07 w=8.5e-06 ad=3.91e-12 \
  as=3.91e-12 pd=1.792e-05 ps=1.792e-05 nrd=0.054118 \
  nrs=0.054118 sd=0 sa=4.6e-07 sb=4.6e-07 \
  dist=445.0 let=LET tau1=1.5e-12 tau2=100e-12 \
  duration=4.5E-12

// Resistor Modeling NWell Contact Resistance
RNWell (see_nwell vdd) resistor r=300
//***************************************************************
<Remaining OpAmp Devices >
//***************************************************************
C34 (vss vss) capacitor c=2.5p
C33 (ref vss) capacitor c=2.5p
C32 (in vss) capacitor c=2.5p
C31 (vdd vss) capacitor c=2.5p
C30 (rinm vss) capacitor c=2.5p
RR1M (ref rinm) resistor r=1M
RR100K (in rinm) resistor r=100k
CRSC (ref vss) capacitor c=13p
R1 (ref vss) resistor r=1M
C29 (vss vss) capacitor c=2.5p
C28 (vdd vss) capacitor c=2.5p
C26 (inm vss) capacitor c=2.5p
C25 (inp vss) capacitor c=2.5p
C5 (out vss) capacitor c=2.5p
RT1M (out inm) resistor r=1M
RT100K (inp inm) resistor r=100k
CTSC (out vss) capacitor c=13p
R0 (out vss) resistor r=1M
//***************************************************************
V2 (in vss) vsource dc=900.0m type=dc
V1 (vss 0) vsource dc=0 type=dc
V0 (vdd vss) vsource dc=1.8 type=dc
E1 (inp vss in vss) vcvs gain=1.0
//***************************************************************
I14 (ref in ref vdd vss subr) buffered_opamp_v3
//***************************************************************
//Start output file designation sources
VX (x 0) vsource type=dc dc=-250
VY (y 0) vsource type=dc dc=280
VLET (swlet 0) vsource type=dc dc=LET
//End sources
```

```
//************************************************************
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 \
  temp=27 tnom=25 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
  maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
  checklimitdest=psf
mc1 montecarlo numruns=1 donominal=no scalarfile="output.txt" {
sweep1 sweep param=LET values=[10 20 30 40 60] {
  tran tran stop=10u \
  annotate=status maxiters=5
  export LET=oceanEval("value(v(\"swlet\" ?result \"tran\" ) \
    1e-9)")
  export OUTE=oceanEval("integ(abs(v(\"out\" ?result \"tran\" ) \
    -v(\"ref\" ?result \"tran\" ) - (value(v(\"out\" \
    ?result \"tran\" ) 40n ) - value(v(\"ref\" \
    ?result \"tran\" ) 40n )))**2)*1E9")
  export PEAK=oceanEval("value(v(\"out\" ?result \"tran\" ) \
    -v(\"ref\" ?result \"tran\" ) xmax(abs(v(\"out\" \
    ?result \"tran\" )-v(\"ref\" ?result \"tran\" )) 1 ))")
  export TWOP=oceanEval("ymax(cross(abs(v(\"out\" \
    ?result \"tran\" )-v(\"ref\" ?result \"tran\" )) \
    0.018 1 \"either\" t \"time\"))-ymin(cross(abs(v(\"out\" \
    ?result \"tran\" )-v(\"ref\" ?result \"tran\" )) \
    0.018 1 \"either\" t \"time\"))")
  export FWHM=oceanEval("ymax(cross(abs(v(\"out\" \
    ?result \"tran\" )-v(\"ref\" ?result \"tran\" )) \
    ymax(abs(v(\"out\" ?result \"tran\" )-v(\"ref\" \
    ?result \"tran\" )))/2 1 \"either\" t \"time\")) \
    -ymin(cross(abs(v(\"out\" ?result \"tran\" ) \
    -v(\"ref\" ?result \"tran\" )) ymax(abs(v(\"out\" \
    ?result \"tran\" )-v(\"ref\" ?result \"tran\" )))/2
    1 \"either\" t \"time\"))")
  export X=oceanEval("value(v(\"x\" ?result \"tran\" ) 1e-9)")
  export Y=oceanEval("value(v(\"y\" ?result \"tran\" ) 1e-9)")
  }
}
save out ref swlet x y
```

Table 23: Example output file, output.txt, from the layout-aware netlist shown in Table 22. The table header is for reference, the actual file contains no headers to ease parsing of results.

LET	OUTE	PEAK	TWOP	FWHM	X Location	Y Location
10	1.54706	-0.0801286	1.01815e-06	1.54713e-07	-250	280
20	2.2415	-0.0972754	1.3783e-06	1.55391e-07	-250	280
30	2.38915	-0.101333	1.39699e-06	3.76471e-07	-250	280
40	2.31663	-0.100713	1.37318e-06	1.5382e-07	-250	280
60	2.2996	-0.0999503	1.38328e-06	1.54757e-07	-250	280

Cadence Tool Flow Integration

Integration with the Cadence GUI tools requires modifications to the user's cdsinit and cdsenv files as well as customized Skill routines and menu files for Analog Design Environment (ADE). Table 24 contains modifications to the user cdsinit file that loads the routines for a GUI interface to use the single-event models in the Cadence Virtuoso Schematic Editor and ADE. The cdsinit modification expects an environment variable, RAD_INSTALL_DIR, which points to the top level of the models directory, e.g. /opt/SEE_Models/Spectre_SEE. The installation directory should have a Skill directory that contains the code to be loaded. Table 25 shows the additional line required to trigger the loading of the GUI menu when ADE is started. The custom menu for ADE is included in a "menus" directory contained in the user's working directory or home directory. The custom menu file for ADE is called simui.menus and is shown in Table 26. A picture of the Cadence Analog Design Environment window with the custom radiation-enabled menu is shown in Fig. 80.

This section contains the Skill routines utilized in the integration of the radiation-enabled models with the Cadence design tools GUI. Tables 27-30 show the Skill routines for the Single-Event Simulation Form, as well as the routines for error checking and single-event simulation initiation. These routines are included in the

radSEE.il file loaded by the cdsinit modifications in Table 24. A picture of the Single-Event Simulation Form window is shown in Fig. 81.

Table 24: Modifications to user cdsinit file that loads routines for GUI integration of single-event models

```
;#########################################
;# LOAD RADIATION MODELING SKILL CODE
;#########################################
;
;The path to the skill code will need to be modified based
;on the site’s selected install method. Suggested install
;locations include $RAD_INSTALL_DIR/Skill or
; /Skill as shown in the if statements below. If another
;installation location is selected, the if statements
;must be modified to reflect the path to the skill code.
;
printf( ”BEGIN LOADING RADIATION MODELING SKILL CODE...\n” )

rad_home=getShellEnvVar(”RAD_INSTALL_DIR”)

if( isFile( strcat( rad_home ”/Skill/radSEE.il” ) ) then
   printf( ”Loading radSEE.il from $RAD_INSTALL_DIR/Skill\n” )
   loadi( strcat( rad_home ”/Skill/radSEE.il” ) )
else
   if( isFile( ” /Skill/radSEE.il” ) then
      printf( ”Loading radSEE.il from  /Skill\n” )
      loadi( ” /Skill/radSEE.il” )
   else
      printf( ”ERROR: radSEE.il skill code not found!\n” )
      )
   )
printf( ”END OF LOADING RADIATION MODELING SKILL CODE\n” )
```

Table 25: The cdsenv line that triggers the GUI menu when Cadence Analog Design Environment is started.

```
asimenv.startup sessInitTrigFunc string ”radMenuPostInstallTrigger”
```

Table 26: The simui.menus file contains a customized ADE menu, which enables the addition of a Radiation pull-down menu in the ADE interface.

```
/****************************************************************
* This file contains material that is developed and maintained by the
* Institute for Space and Defense Electronics (ISDE) at
* Vanderbilt University
*
* Copyright (c) 2015 Jeff Kauppila, Institute for Space and
* Defense Electronics, All Rights Reserved
*
* File: simui.menus
*
* Description: Skill functions used to implement forms and routines for
* the simulation of single event effects in CMOS transistors.
* The generated form compiles the netlist and runs the SEE sim.
****************************************************************/
;------------------------------------------------------------
; Load the standard menus file
;------------------------------------------------------------
load(prependInstallPath("etc/tools/menus/simui.menus"))
;------------------------------------------------------------
; Identical to the IC614/IC615 menus files, but with "Custom" added.
; Note that the & in the names indicates the following char is the
; accelerator key
;------------------------------------------------------------
(sevSetMainWindowPulldownMenus
  (let (menu)
   menu = `(
            "S&ession"
            "Set&up"
            "&Analyses"
            "&Variables"
            "&Outputs"
            "&Simulation"
            "&Results"
            "&Tools"
            "R&adiation"
            "&Help"
   )
   when( envGetVal("adexl.launchFromTest" "showMenu")
      menu = cons("&Launch" menu)
   )
```

```
    menu
   )
  )
;——————————————————————————————
; Add to the existing menus, rather than "setting". Better than making
; this a copy of the built-in default menus and then hacking - much
; more likely to stay in sync this way.
;——————————————————————————————
(sevAddMenuItemLists
  (lambda
    (session name)
    (case
     name
     ;—————————————————————————-
     ; Define Custom menu
     ;—————————————————————————-
     ("R&adiation"
       `(
         ("&Single Event" ?callback (radSEESetupSim ',session))
       ))
    )
  )
)
```

Table 27: Skill routines to create the Single-Event Simulation Form.

```
/**************************************************************
* radSEE.il
**************************************************************
* This file contains material that is developed and maintained by the
* Institute for Space and Defense Electronics (ISDE) at
* Vanderbilt University
*
* Copyright (c) 2015 Jeff Kauppila, Institute for Space and
* Defense Electronics, All Rights Reserved
**************************************************************
* Description: Skill functions used to implement forms and routines
* for the simulation of single event effects in CMOS
* transistors. The generated form compiles the netlist
* and runs the SEE sim.
```

```
*************************************************************/
/*************************************************************
* Function: radSEESetupSim
* This function gets the current simulation sessions, calls for
* the creation of the SEE simulation setup form, and displays
* the form on screen.
*
* Input Parameters: session
* The session parameter is the current sevSession(). It is
* passed to the function from the simui.menus file in the
* Radiation->Single Events... pulldown menu.
*
* Return Parameters: NONE
*************************************************************/
procedure( radSEESetupSim(session)
  asiSession=asiGetCurrentSession()
  rexPat="Spectre_SEE"
  modFlag=when( or( ( length( asiGetModelLibSelectionList(asiSession))<1)
        ( length( rexMatchAssocList( rexPat
        asiGetModelLibSelectionList( asiSession ) ) )!=1 ) )
      hiDisplayUserDBox(
        ?name 'modFlagDBox
        ?dboxBanner "Model Selection Warning"
        ?dboxText strcat( "The model library selection "
          "list does not have single event "
          "models enabled or selected.\n"
          "Please select and enable the single "
          "event models and press <Fixed>.\n"
          "You may use the Model Selection "
          "button on this form or Setup->"
          "Model Libraries... in Analog Design "
          "Environment." )
        ?dialogStyle 'modeless ?buttons list( "Fixed" )
        ?callbacks list( "radSEECkModList(
                asiSession seeForm rexPat)" )
          )
      )
  tranFlag=when( !asiIsAnalysisEnabled(
                asiGetAnalysis( asiSession 'tran ) )
      ;If tran Analysis is not enabled we want a modeless dialog
      ;box that will check the tran in Ok callback and call
      ;itself again if tran is not set, but it will need to be
      ;called
      hiDisplayUserDBox(
```

```
      ?name 'tranFlagDBox ?dboxBanner "Tran. Enable Warning"
      ?dboxText strcat( "The transient analysis option is not "
        "enabled.\nPlease select a transient analysis "
        "and press <Fixed >." )
      ?dialogStyle 'modeless ?buttons list( "Fixed" )
      ?callbacks list( "radSEETranFlagCB( asiSession seeForm )" )
      )
    )
  seeForm=radSEECreateForm( session asiSession modFlag tranFlag rexPat)
  hiDisplayForm( seeForm )
  ) ; end procedure radSEESetupSim
/***************************************************************
* Function: radSEECreateForm
* This function creates the SEE simualtion setup form
*
* Input Parameters: session, asiSession
* The session parameter is the current sevSession() output.
* The asiSession parameter is the asiGetCurrentSession() output
* These parameters are passed to the call backs for accessing
* Simualtion environment information.
*
* Return Parameters: s_form_handle
* The handle to the form is passed back.
***************************************************************/
procedure( radSEECreateForm( session asiSession tranFlag modFlag rexPat)
  letFloat=hiCreateFloatField( ?name 'letFloat ?prompt "LET [0->100]"
     ?defValue 0.0 ?range list( 0.0 100.0 )
     )
  t0Float=hiCreateFloatField( ?name 't0Float ?prompt "see_start_time"
     ?defValue 0.00
     ?callback "radSEET0CB( asiSession hiGetCurrentForm() )"
     ?range list( 0.0 1E12 )
     )
  tau1Float=hiCreateFloatField( ?name 'tau1Float ?prompt "see_tau1"
     ?defValue 1e-13 ?range list( 0.0 1.0 )
     )
  tau2Float=hiCreateFloatField( ?name 'tau2Float ?prompt "see_tau2"
     ?defValue 5e-12 ?range list( 0.0 1.0 )
     )
  durFloat=hiCreateFloatField( ?name 'durFloat ?prompt "see_duration"
     ?defValue 4e-13 ?range list( 0.0 1.0 )
     )
  tiltFloat=hiCreateFloatField( ?name 'tiltFloat ?prompt "see_tilt"
     ?defValue 0.00 ?range list( 0.0 90.0 )
```

```
    )
rollRadio=hiCreateRadioField( ?name 'rollRadio ?choices list("0" "90")
    ?prompt "see_roll" ?defValue "0" ?itemsPerRow 2
    )
seeInst=hiCreateStringField( ?name 'seeInst
    ?prompt "SEE Device Instance:"
    ?defValue "nil"
    ?callback "radseeInstValueCB( session asiSession hiGetCurrentForm() )"
    )
seeInstButton=hiCreateButton( ?name 'seeInstButton
    ?buttonText "Select FinFET from Schematic..."
    ?callback "radseeInstButtonCB( session asiSession hiGetCurrentForm() )"
    )
seeEditModelButton=hiCreateButton( ?name 'seeEditModelButton
    ?buttonText "Model Selection"
    ?callback "sevEditModels(session)"
    )
seeNlRun=hiCreateButton( ?name 'seeNlRun
    ?buttonText "SEE Netlist and Run"
    ?callback "radSEENlRun( session asiSession hiGetCurrentForm() rexPat)"
    ?enabled !or( tranFlag modFlag )
    )
seeAnalysis=hiCreateButton( ?name 'seeAnalysis
    ?buttonText "SEE Analysis"
    ?callback "t" ?enabled nil )
hiCreateAppForm( ?name 'seeForm
    ?formTitle "Single Event Effects Simulation Setup"
    ?fields list(
      list( letFloat 5:15 195:30 80 )
      list( t0Float 5:50 195:30 80 )
      list( durFloat 205:50 195:30 80 )
      list( tau1Float 5:85 195:30 80 )
      list( tau2Float 205:85 195:30 80 )
      list( tiltFloat 5:120 195:30 80 )
      list( rollRadio 205:120 195:30 80 )
      list( seeInst 5:155 395:30 135 )
      list( seeInstButton 5:190 395:30 )
      list( seeEditModelButton 5:225 118:30 )
      list( seeNlRun 128:225 149:30 )
      list( seeAnalysis 282:225 118:30 )
      )
    ?buttonLayout 'Close
    ?attachmentList list(
      hicTopPositionSet|hicLeftPositionSet|hicRightPercentSet
```

```
    hicTopPositionSet|hicLeftPositionSet|hicRightPercentSet
    hicTopPositionSet|hicLeftPositionSet|hicRightPercentSet
    hicTopPositionSet|hicLeftPositionSet|hicRightPercentSet
    hicTopPositionSet|hicLeftPositionSet|hicRightPercentSet
    hicTopPositionSet|hicLeftPercentSet|hicRightPercentSet
    hicTopPositionSet|hicLeftPercentSet|hicRightPercentSet )
   ?initialSize list( 405 290 )
   ?minSize list( 405 290 )
   )
)
```

Table 28: Skill routines to check the model list and ensure that a transient simulation is setup.

```
/***************************************************************
* Function: radSEECkModList
* Checks to make SEE models are in the model list.
*
* Input Parameters: asiSession, theForm, rexPat
* The asiSession parameter is the asiGetCurrentSession() output.
* The theForm parameter is the handle to the displayed form.
* The rexPat is the regular expression pattern to check
* These parameters are used to access the model list.
*
* Return Parameters: NONE
***************************************************************/
procedure( radSEECkModList(asiSession theForm rexPat)
 prog(
    (libList matchList)
    libList=asiGetModelLibSelectionList( asiSession )
    matchList=rexMatchAssocList( rexPat libList )
    if( or( ( length( libList )<1 ) ( length( matchList )!=1 ) )
     then hiDisplayUserDBox(
      ?name 'modFlagDBox
      ?dboxBanner "Model Selection Warning"
      ?dboxText strcat( "The model library selection "
       "list does not have single event "
       "models enabled or selected.\n"
       "Please select and enable the single "
       "event models and press <Fixed>.\n"
       "You may use the Model Selection "
```

```
        "button on this form or Setup->"
        "Model Libraries... in Analog Design "
        "Environment." )
      ?dialogStyle 'modeless ?buttons list( "Fixed" )
      ?callbacks list( "radSEECkModList(
           asiSession seeForm rexPat )" )
      )
      modFlag=t
      return(nil)
    else
      modFlag=nil
      theForm->seeNlRun->enabled=!or(tranFlag modFlag)
      return(t)
    )
  )
)
/*************************************************************
* Function: radSEETranFlagCB
* Checks to make sure T0 is within the simulation time bounds.
*
* Input Parameters: asiSession, theForm
* The asiSession parameter is the asiGetCurrentSession() output.
* The theForm parameter is the handle to the displayed form.
* These parameters are used to access the tran analysis time
* bounds.
*
* Return Parameters: NONE
*************************************************************/
procedure( radSEETranFlagCB(asiSession theForm)
   if( !asiIsAnalysisEnabled( asiGetAnalysis( asiSession 'tran ) )
    then hiDisplayUserDBox(
      ?name 'tranFlagDBox ?dboxBanner "Tran. Enable Warning"
      ?dboxText strcat( "The transient analysis option is not "
        "enabled.\nPlease select a transient analysis "
        "and press <Fixed>." )
      ?dialogStyle 'modeless ?buttons list( "Fixed" )
      ?callbacks list( "radSEETranFlagCB( asiSession seeForm )" )
      )
      tranFlag=t
      nil
    else
      tranFlag=nil
      theForm->seeNlRun->enabled=!or(tranFlag modFlag)
      t
```

```
    )
  )
```

Table 29: Skill routines to check the single-event start time and the selected instance in the schematic.

```
/****************************************************************
* Function: radSEET0CB
* Checks to make sure T0 is within the simulation time bounds.
*
* Input Parameters: asiSession, theForm
* The asiSession parameter is the asiGetCurrentSession() output.
* The theForm parameter is the handle to the displayed form.
* These parameters are used to access the tran analysis time
* bounds.
*
* Return Parameters: NONE
****************************************************************/
procedure( radSEET0CB(asiSession theForm)
; Check the value and compare it to the from and to values in the tran
; analysis. If it is greater than the bound, show a dialog box warning
; the user about the value, but do not change it
 prog(
    (t0 stoptime scaleTable len strHead strTail)
    scaleTable=makeTable("atable1" "")
    scaleTable["Y"]="E24"
    scaleTable["Z"]="E21"
    scaleTable["E"]="E18"
    scaleTable["P"]="E15"
    scaleTable["T"]="E12"
    scaleTable["G"]="E9"
    scaleTable["M"]="E6"
    scaleTable["k"]="E3"
    scaleTable["K"]="E3"
    scaleTable["%"]="E-2"
    scaleTable["m"]="E-3"
    scaleTable["u"]="E-6"
    scaleTable["n"]="E-9"
    scaleTable["p"]="E-12"
    scaleTable["f"]="E-15"
    scaleTable["a"]="E-18"
```

```
      scaleTable["z"]="E-21"
      scaleTable["y"]="E-24"
      t0=sprintf( nil "%g" theForm->t0Float->value )
      stoptime=asiGetAnalysisFieldVal( asiGetAnalysis(
          asiSession 'tran ) 'stop )
      len=strlen( stoptime )
      strTail=scaleTable[ get_pname( getchar( stoptime len ) ) ]
      when( strcmp( strTail scaleTable[ nil ] )!=0
        len=len-1
        strHead=substring( stoptime 1 len )
        stoptime=strcat(strHead strTail)
        )
      when( alphaNumCmp( stoptime t0 t)!=1
        hiDisplayUserDBox(
          ?name 't0DBox ?dboxBanner "Strike Time After Sim End Time"
          ?dboxText strcat( "The given strike time (" t0 ") occurs "
            "after the given transient simulation stop time "
            "(" stoptime ").\n Please correct the strike "
            "time unless you desire a simulation without a "
            "single event pulse." )
          ?dialogStyle 'modeless ?buttons list( "Ok" )
          )
        )
      )
  )
/***************************************************************
* Function: radseeInstValueCB
* Sets up the terminal selection if the previous selection was
* not a valid terminal selection.
*
* Input Parameters: session asiSession theForm
*
* Return Parameters: NONE
***************************************************************/
procedure( radseeInstValueCB(session asiSession theForm)
  prog(
      (schStrn schFlag winID)
      if( !rexMatchp( "/[MT][0-9]+$" seeForm->seeInst->value)
      then
        hiDisplayUserDBox(
          ?name 'seeInstDBox
          ?dboxBanner "Invalid Device Instance Selection"
          ?dboxText strcat("You have selected the instance: "
            seeForm->seeInst->value " "
```

```
            "instead of a MOSFET device in the design.\n"
            "Please select a MOSFET instance from the schematic."
            )
          ?dialogStyle 'modeless ?buttons list("Ok")
          ?callbacks list( "radseeInstButtonCB( session asiSession seeForm )" )
          )
        seeForm->seeNlRun->enabled=and(nil !or(tranFlag modFlag))
      else
        hiDisplayUserDBox(
          ?name 'seeInstOkDBox
          ?dboxBanner "Valid MOSFET Selection"
          ?dboxText strcat("You have selected the instance: "
            seeForm->seeInst->value " "
            "which is a valid MOSFET device selection.\n"
            "The selected MOSFET device will be used in the "
            "single event simulation."
            )
          ?dialogStyle 'modeless ?buttons list("Ok")
          ?dialogType hicMessageDialog
          )
        seeForm->seeNlRun->enabled=and(t !or(tranFlag modFlag))
        )
      )
  )
```

Table 30: Skill routines to initiate device selection from schematic and trigger netlist creation and simulation.

```
/***************************************************************
* Function: radseeInstButtonCB
* Sets up the terminal selection from schematic and check the
* selected terminal to make sure it is a source or a drain. If
* it is not a valid selection, pop a dialog box and set the
* value back to the default value.
*
* Input Parameters: session asiSession theForm
*
* Return Parameters: NONE
***************************************************************/
procedure( radseeInstButtonCB(session asiSession theForm)
  prog(
```

```
    (schStrn schFlag winID)
    theForm->asiSession=asiSession
    schStrn=strcat(asiGetDesignLibName(asiSession) " "
      asiGetDesignCellName(asiSession) " "
      asiGetDesignViewName(asiSession)
      )
    schFlag=nil
    foreach( winID hiGetWindowList()
      when( rexMatchp(schStrn hiGetWindowName(winID)) schFlag=t)
      )
    unless(schFlag sevOpenSchematic(session))
    asiSelectInst( 'seeInst ?prompt "Select a FinFET instance..."
      ?form theForm )
    )
  )
/*************************************************************
* Function: radSEENlRun
* Performs the initial netlisting, netlist modification and
* simulation run function calls. There is also some error
* checking that will be used to make sure we have the right
* models, parameter bounds, etc.
*
* Input Parameters: session asiSession theForm
*
* Return Parameters: NONE
*************************************************************/
procedure( radSEENlRun(session asiSession theForm rexPat)
  prog(
    (perlPath parsePath simDir netlist LET T0 INST TAU1 TAU2 DUR TILT ROLL)
    if( and( radSEECkModList(asiSession theForm rexPat)
        radSEETranFlagCB(asiSession theForm) )
      then
        perlPath=strcat( car(getInstallPath()) "/../perl/bin/perl" )
        parsePath=strcat( getShellEnvVar("RAD_INSTALL_DIR") "/scripts/" )
        simDir=asiGetNetlistDir( asiSession )
        netlist=asiGetSimInputFileName( asiSession )
        LET=sprintf( nil " -let %g" theForm->letFloat->value )
        T0=sprintf( nil " -start %g" theForm->t0Float->value )
        DUR=sprintf( nil " -duration %g" theForm->durFloat->value )
        TAU1=sprintf( nil " -tau1 %g" theForm->tau1Float->value )
        TAU2=sprintf( nil " -tau2 %g" theForm->tau2Float->value )
        TILT=sprintf( nil " -tilt %g" theForm->tiltFloat->value )
        ROLL=strcat( " -roll " theForm->rollRadio->value )
        INST=theForm->seeInst->value
```

```
      sevNetlistFile(session 'recreate)
      println( strcat( "Adding SEE Model to " simDir "/" netlist ) )
      modCall=strcat( perlPath " " parsePath "see_insert_GUI.pl "
        LET T0 DUR TAU1 TAU2 TILT ROLL " " INST " " simDir "/" netlist
        )
      println( strcat( "Call: " modCall ) )
      if(sh( modCall )
        then
            /*Add the calls to the netlist modification program*/
            println( "Modification Complete... Running Simulation..." )
            sevRun(session)
        else
            println( "Modification exited with an error" )
        )
    else
      theForm->seeNlRun->enabled=!or(tranFlag modFlag)
    )
  )
)
```

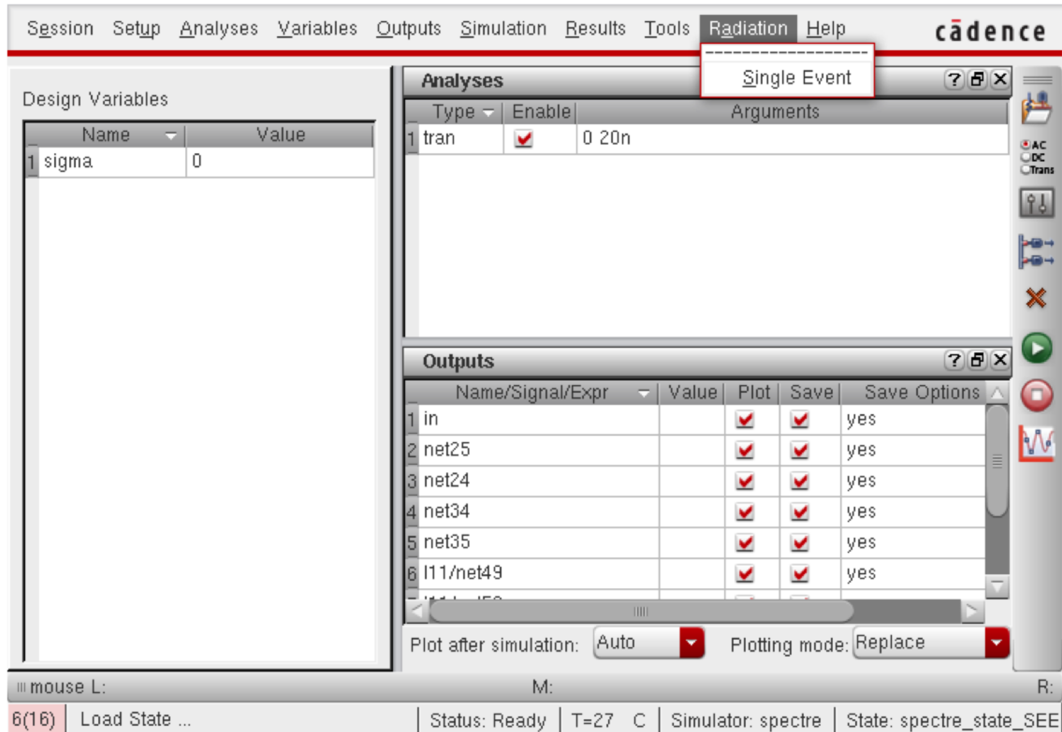

Figure 80: Cadence Analog Design Environment window with the custom radiation-enabled menu.

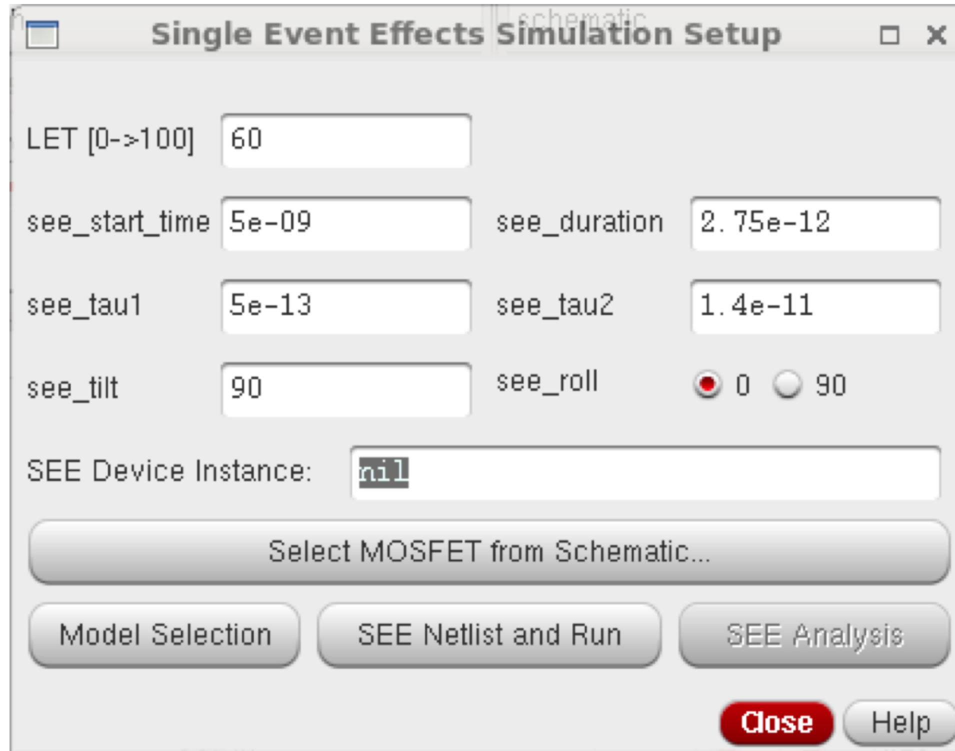

Figure 81: The Single-Event Simulation Form created with the skill code from Tables 27-30.