RADIATION EFFECTS AND LOW FREQUENCY NOISE IN BLACK PHOSPHORUS TRANSISTORS

By

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Table of Contents

LIST OF TABLES

LIST OF FIGURES

Chapter 1 . Introduction

The integrated circuit (IC) industry has benefitted for over five decades from “Moore’s law,” which states that the number of transistors on a chip doubles every 18 months [1]. The key to sustain Moore’s law is the scaling of single transistors. As the transistors scale in dimension, more transistors are integrated on a single chip, yielding an exponential increase in the device density and therefore the functionality of the chip. In addition, the device miniaturization itself boosts the performance of individual transistors by lowering the supply voltage and decreasing the intrinsic delay.

As the feature sizes (or channel lengths) of conventional Silicon-based Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) scale into the nanometer regime, it is becoming more and more challenging to sustain Moore’s law. Several significant changes have been implemented to enable continuous scaling, as shown in Fig. 1.1 [2]. For example, strain engineering was introduced in the 90 nm node to increase the carrier mobility [3]. Metal-gate/high-k gate stacks were implemented in the 45 nm node to limit the gate leakage and eliminate poly-silicon depletion [4]. The device structure transitioned from planar transistors to FinFETs in the 22 nm node to enhance the gate control during device scaling [5]. For 7 nm technology, III-V/Ge materials are promising NMOS/PMOS channel materials due to the high carrier mobility and injection velocity [6].

One obstacle for scaling is that the transistor becomes more difficult to “turn off” due to the exacerbation of short channel effects with the continuous scaling down of the channel length.

According to the classic MOSFET scaling theory, off-state leakage control of a planar MOSFET maintains if the channel length is larger than the characteristic length λ [7]:

$$\lambda = t_{OX} + (\varepsilon_{OX}/\varepsilon_{ch})t_{ch}, \tag{1.1}$$

where t_{OX} and t_{ch} are the oxide thickness and channel material thickness, and ε_{OX} and ε_{ch} are the relative permittivities of the oxide and channel materials.

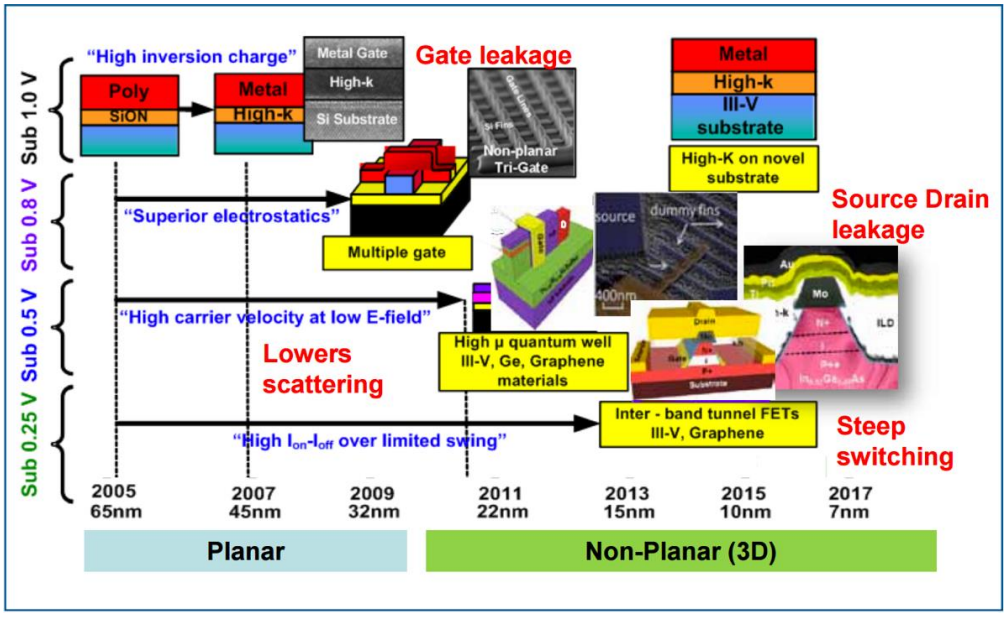


Fig. 1.1. Development of state-of-the-art high performance (HP) CMOS transistors [2].

Thus, scaling of the channel material thickness enables the continuous scaling of the channel length with off-state leakage control. However, the mobility of the conventional bulk materials such as Si, InGaAs and InAs decreases significantly when the thickness is reduced below 7 nm [6], [8]–[10]. Therefore, alternative high-performance logic devices are currently being investigated to maintain the scaling trends [5].

In fact, global research efforts have been devoted, with an emphasis on novel channel materials to develop thin materials with high mobility for electronics applications. Two-dimensional (2D) semiconductors possess atomically thin body thickness while maintaining the mobility, making them promising channel material candidates for further channel length scaling [11]–[17]. Recent advances in material integration have even allowed for the possibility of 2D material integration into Si-based fabrication processes [18]–[20].

1.1 Two-Dimensional Materials and Black Phosphorus

In 2004, the success of isolated graphene by the mechanical exfoliation method inspired research on related 2D atomic layers worldwide. To date, graphene is one of the most widely studied (and thinnest) 2D materials. To realize the high-performance transistors for future beyond-silicon CMOS logic technology, it requires channel materials with non-zero band gap and reasonably high carrier mobility. While graphene offers high carrier mobility, its lack of a band gap makes it unsuitable for most transistor applications. Although researchers make efforts to create a bandgap in pristine graphene, the low on/off current ratio is still an open issue for graphene-based transistors [21]–[23]. Recently, a wide range of 2D semiconductor materials has emerged with band gaps in the 1-2 eV range, with the most common among these being the transition metal dichalcogenides (TMDs) such as Molybdenum Disulfide (MoS_2) and Tungsten Diselenide (WSe_2) [24], [25]. However, TMDs have the difficulty that they have relatively low mobility due to the heavy effective mass of carriers, making them questionable for high-performance transistors. Novel materials with the properties of good mobility and a non-zero

bandgap are in great need to fill in the “gap” between Graphene and TMDs.

In 2014, black phosphorus (BP), a thermodynamical allotrope of the element phosphorus, emerged as a promising 2D semiconductor with a moderate band gap for nanoelectronics and nanophotonics applications [12], [14], [26], [27]. Similar to graphene, single-layered or few-layered black phosphorus can be obtained by mechanical exfoliation. Due to the strong electronic state coupling among layers in BP, its direct bandgap is tunable from 0.3 eV in bulk to 2 eV in monolayer form, covering the visible to the mid-infrared range for photonics application [28]. Also, BP offers mobility as high as 1000 cm^2/Vs (600 cm^2/Vs) for holes (electrons) at room temperature, while maintaining on/off current ratio up to 10^5, making it a promising candidate for future transistor applications [29]. The comparison between these 2D materials is shown in Fig.1.2.

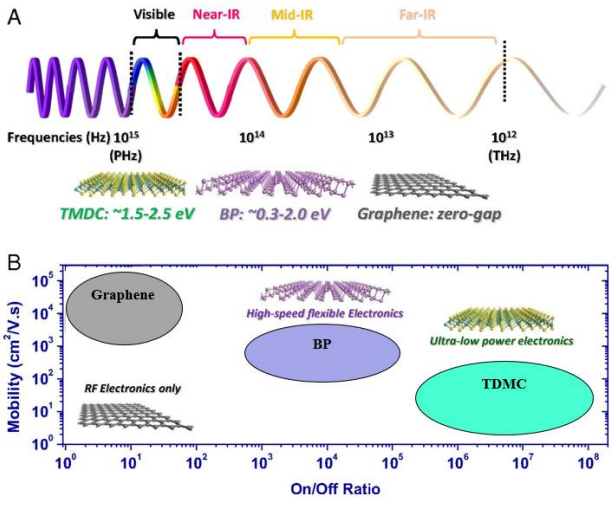


Fig.1.2. Electromagnetic wave spectrum and mobility/on–off ratio spectrum. (A) The electromagnetic wave spectrum and the band gap range of various types of 2D materials. The frequency ranges corresponding to the band gaps of 2D materials and their applications in optoelectronics are also indicated. (B) The shaded regions are the approximate possible ranges of performance reported for the respective materials in the literature [29].

The thermodynamically stable crystal structure of black phosphorus consists of multiple layers, and these layers are stacked together by van der Waals interactions. Within a layer, each phosphorus atom covalently bonds to three adjacent atoms and the structure is a puckered honeycomb. The covalent bonds take up all three valence electrons of phosphorus by sp^3 hybridization, so monolayer black phosphorus is a semiconductor with a bandgap [13].

For the monolayer BP, the armchair (AM) and the zigzag (ZZ) direction are shown respectively in Fig. 1.3. Because of the high carrier mobility, BP is suitable for complementary metal oxide semiconductor (CMOS) applications [29]. However, the dominant conduction type in BP is hole transport, which can be ascribed to the higher degree of anisotropy of the hole effective mass [13]. Also, distinct anisotropy phenomena are observed in carrier transport. Researchers reported that the hole mobility along the ZZ direction of monolayer BP is 16–38 times larger than that along the AM direction, and they attributed it to the higher elastic modulus along the ZZ direction as relatively stiffer 2D materials exhibit higher carrier mobility [13].

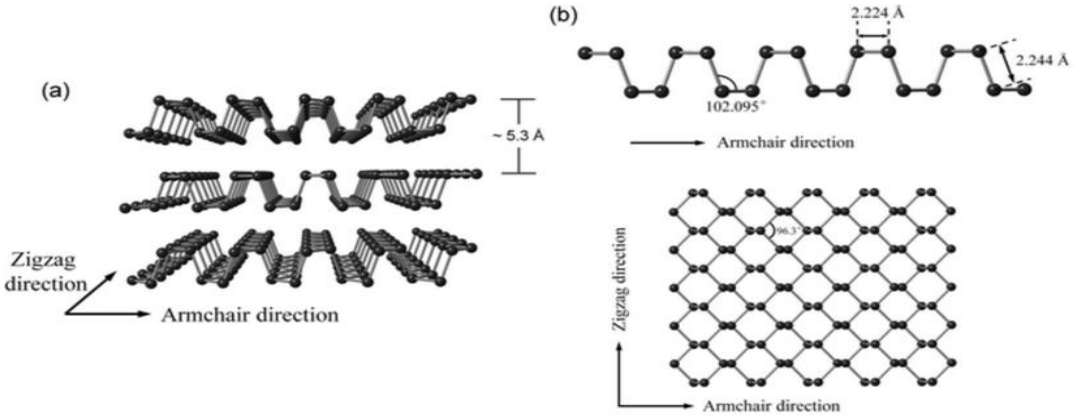


Fig. 1.3. (a) Atomic structure of multi-layer black phosphorus and (b) monolayer phosphorene [13].

One important property of BP is that its bandgap is thickness dependent. With increasing number of layers, the bandgap decreases due to interlayer interactions. The bandgap decreases from 2 eV in a monolayer to 0.3 eV in bulk BP, with a direct gap for all the thicknesses, as shown in the band structure plots in Fig. 1.4 [16].

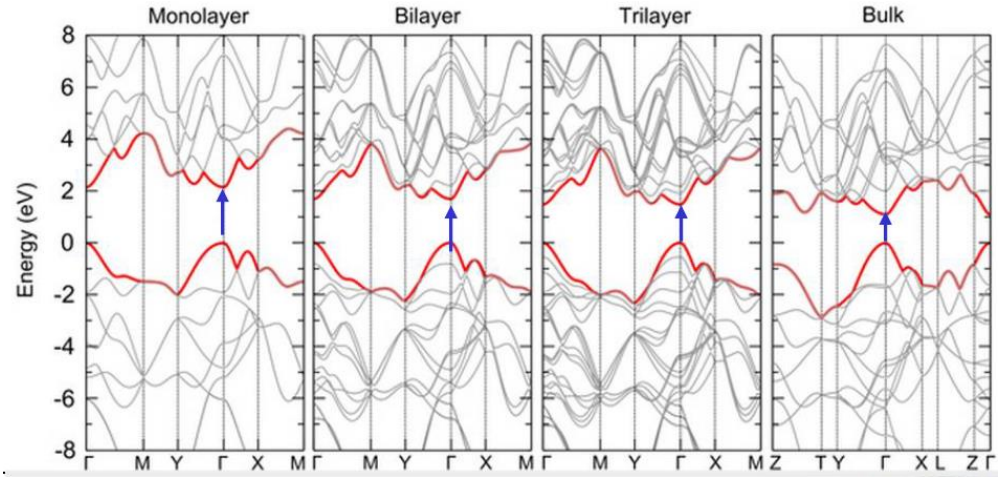


Fig. 1.4. The band structure of BP with different number of layers [16].

1.2 High-K materials and HfO_2

Generally, the gate oxide thickness of the transistor scales with the channel length, which results in increasing gate leakage current. The thickness of conventional bulk SiO_2 gate dielectrics has reached its physical limitations due to the constraints on the gate leakage current [16]. Thus, high-permittivity (high-K) materials such as hafnium-based, zirconium, and aluminum oxides are introduced as alternative gate dielectrics for SiO_2. High-K materials allow a further increase of the physical thickness of the gate stack to suppress the leakage current while keeping the equivalent oxide thickness (EOT) constant:

$$EOT = \frac{\varepsilon_{high-K}}{\varepsilon_{SiO_2}} d_{high-K}, \tag{1.2}$$

where ε_{SiO_2} and ε_{high-K} are the dielectric constants of silicon dioxide and high-K material, respectively. d_{high-K} is the physical thickness of the high-K dielectric.

Hafnium oxide (HfO_2), alumina (Al_2O_3), and zirconium oxide (ZrO_2) are the materials with greatest potential to replace SiO_2 in MOS devices, mainly due to their relatively high dielectric constants compared to other high-K materials and better band offsets than most other high-K dielectrics [30]. Both the conduction and valence band offsets between monolayer/bulk BP and HfO_2 are larger than 1 eV, which is large enough to stop the leakage current for gate oxide [31].

Unlike the thermal oxidation techniques used to fabricate gate SiO_2 in Si MOSFETs, atomic layer deposition (ALD) techniques are used for depositing thin high-K gate oxides in MOSFETs. However, to grow an extremely uniform layer-by-layer ALD film, which is needed to ensure uniform electrical performance across the entire gate oxide, the nucleation of ALD precursors with the initial surface species needs to be efficient on the very first ALD cycle. In this respect, 2D materials are inadequate nucleation templates for enabling reaction with the ALD precursors because of the intrinsic lack of dangling bonds on the exposed surface, which may lead to a non-conformal growth of high-k dielectric films [31]. For example, AFM and TEM images of the cross-section reveal that HfO_2 deposited using ALD on MoS_2 surfaces shows a non-uniform, island-like morphology, as shown in Fig. 1.5. This type of structure exhibits poor electrical properties due to the high defect densities. During device operation, these traps could

capture carriers tunneling from the channel, resulting in performance degradation of the device.

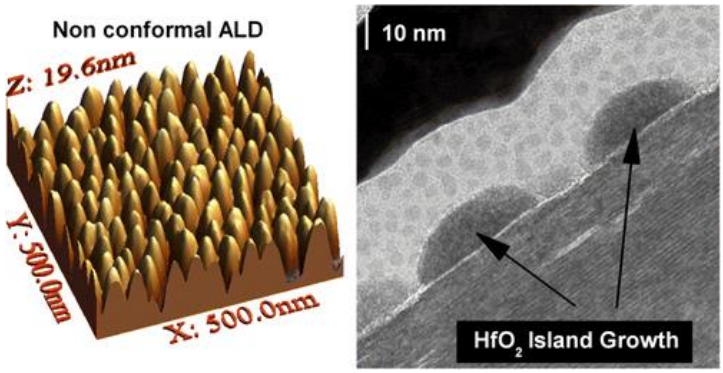


Fig. 1.5. AFM and TEM images of a HfO_2 ALD film deposited on MoS_2 thin layers [31].

1.3 Overview of Dissertation

It is necessary to evaluate the charge trapping characteristics and reliability of BP/high-k structure devices, as well as single event transient charge collection for potential space-exploration applications. In this thesis, total ionizing dose radiation effects, low frequency $1/f$ noise and single event effects on BP/high-k structure are explored. This thesis is organized as follows: Chapter 2 describes the background of this work. Defects, reliability and radiation-effects mechanisms are introduced; radiation reports on relevant 2D-material-based transistors are summarized. Chapter 3 describes the technology for BP MOSFET structure and fabrication. Device operation mechanisms are analyzed, and one unique stability issue of BP MOSFETs is discussed. Chapter 4 covers the TID responses of BP MOSFETs with passivation layer to 10 keV X-ray and proton irradiation. DC electrical characterizations are conducted before and after irradiation to evaluate the impact of TID effects. Switched-bias annealing after irradiation is used to explore the mechanisms of the TID-induced trapping effects. Chapter 5 presents and discusses

the low frequency $1/f$ noise in MOSFET transistors. Experimental results on the temperature dependence of the $1/f$ noise on BP MOSFETs before and after X-ray irradiation. DFT calculation is also performed to study the origin of the irradiation-induced defects. Chapter 6 reports the single event transients in BP MOSFETs induced by single-photon-absorption (SPA) laser irradiation. The last chapter provides conclusions of this work.

Chapter 2 . Defects and Radiation Reliability Mechanisms

Defects in MOS impact the reliability of the electronic devices. Also, they play an important part in the radiation effect for space applications. The first part of this chapter contains background information about the defects impacting the reliability performance of MOS devices. The second part of this chapter describes the mechanisms of radiation effects in MOS devices.

2.1 Defects and Reliability

Depending on the locations of the defects, the traps in the silicon MOSFETs are categorized into interface traps, border traps, and oxide traps. Interface traps are located at the Si/SiO_2 interface and in electrical communication with the underlying Si. Border traps are near-interfacial oxide traps that exchange charge with the underlying Si on the time scale of the measurements. Oxide-trapped charges are located within the oxide and are not in electrical communication with the underlying Si. The location and the electrical properties of the defects are shown in Fig. 2.1.

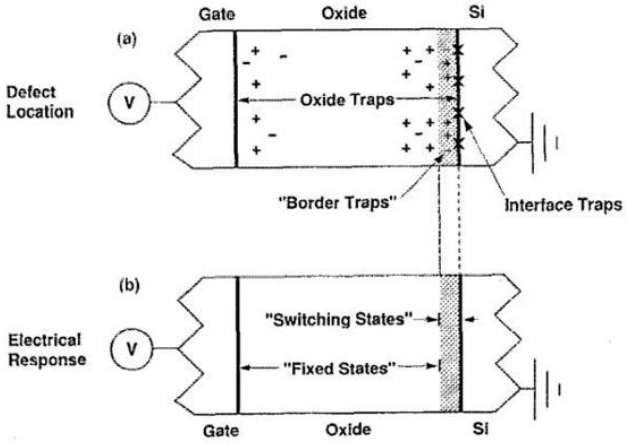


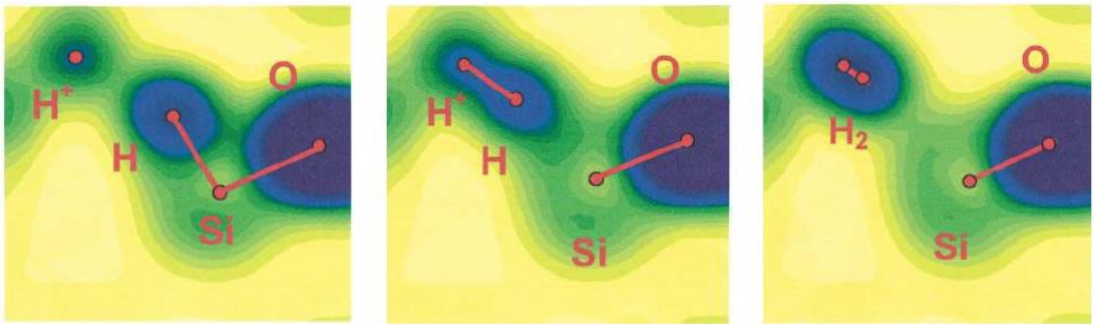
Fig. 2.1. Schematic representation of (a) the physical location of oxide, interface, and border traps and (b) their electrical response [32].

Interface traps:

At the interface between the oxide and the channel silicon, some of the Si atoms are bonded to another three Si atoms, with a dangling bond extending into the oxide. This configuration is called a P_b center. During device fabrication, most of the dangling bonds are passivated with hydrogen to form P_b-H precursor sites. Density functional theory calculations by Rashkeev et al. [33] strongly suggest that protons interact directly and break the Si-H bonds at the Si/SiO_2 interface via the simple reaction:

$$H^+ + \text{Si-H} = Si^+ + H_2 \qquad (2\text{-}1)$$

This suggests that two electrons leave the Si-H through a Si-H-H^+ bridge, forming a neutral H_2 molecule and leaving a dangling bond positively charged. The process is shown in Fig. 2.2.



(a) (b) (c)

Fig. 2.2. Electronic density at different stages of the reaction between H^+ and a Si-H bond: (a) a proton approaches a Si-H bond; (b) a Si-H-H^+ bridge is created; (c) an H_2 molecule and a defect are formed [33].

Oxide traps:

There are a large number of oxygen vacancies close to the interface where oxidation is not complete. The oxygen vacancy can be activated into the paramagnetic state by irradiation or

electric field stress. The model is shown in Fig. 2.3. The radiation-induced or stress-induced paramagnetic center is termed an E’ defect, which is identified as a "trivalent silicon” back-bonded to three oxygen atoms in the oxide. There is one oxygen atom missing from the usual Si-O-Si lattice configuration, leaving a weak Si-Si bond. E’ centers or oxygen vacancies are primarily responsible for hole traps in pMOS devices during TID tests [34], [35]. After the hole is trapped in the precursor bridging-oxygen vacancy, the weak and strained Si-Si bond configuration is broken. One of the Si atoms then relaxes back into a planar configuration, leaving it positively charged. The other Si remains neutral, with a dangling orbital containing one unpaired electron.

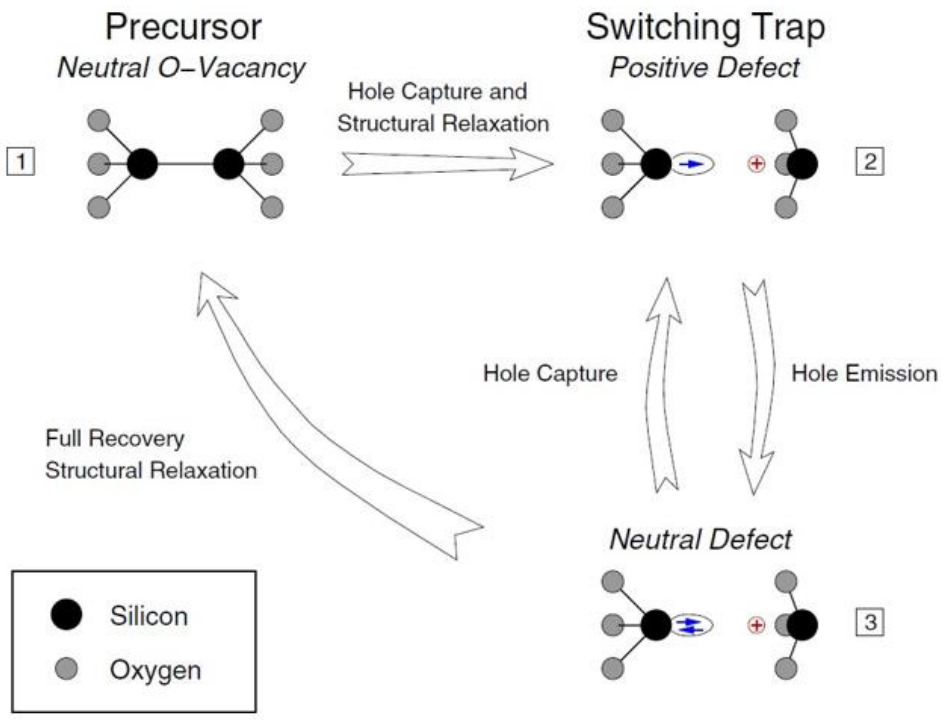


Fig. 2.3. Switching oxide trap model [36].

Border traps:

A standard name for near-interfacial oxide traps that communicate with the Si was proposed as “border traps” by D. M. Fleetwood in 1992 [32]. Border traps are defined as near-interfacial oxide traps that can rapidly or slowly exchange charge with the underlying Si substrate over a very wide range of timescales. There is growing evidence that a large percentage of these defects are likely associated with E’ centers [32], [37], [38]. Border traps typically are located within a certain distance (less than ~2 or 3 nm) in the oxide from the interface.

2.2 Radiation Effects on 2D Material MOSFETs

The potential high performance of 2D materials makes 2D MOSFETs important candidates for space applications. However, to operate in the harsh space environment, they must be able to withstand radiation, including high energy particles, protons, electrons, heavy solar ions and galactic cosmic rays. Radiation can have different effects on devices or ICs. In this thesis, two types of the radiation effects, total ionizing dose (TID) effects and single event effects (SEE), are studied.

2.2.1 Total Ionizing Dose (TID) Effect

TID effects refer to parametric degradation and functional failures in electronic devices caused by ionizing radiation. It is a significant concern for the long-term reliability of MOS devices. Fig. 2.4 shows the physical processes that occur in silicon MOS systems under positive

gate bias following ionizing radiation. Usually, insulators are the most sensitive parts in the MOS system.

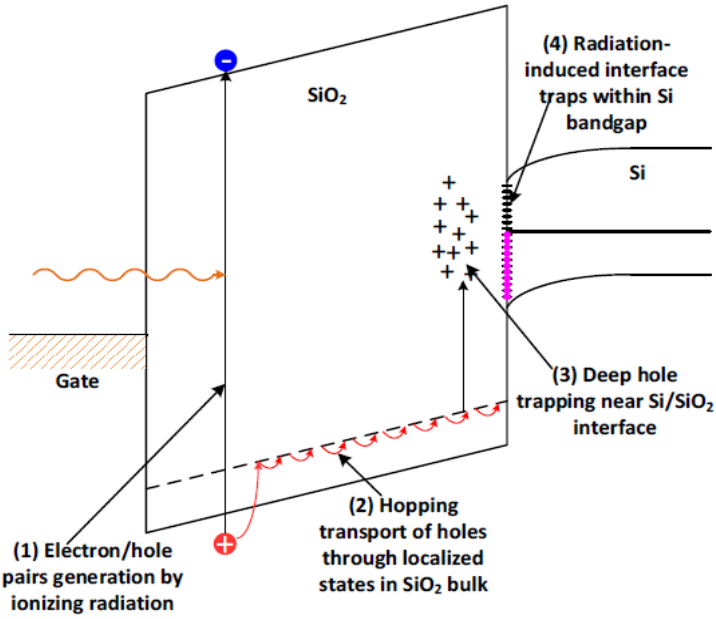


Fig. 2.4. Schematic diagram illustrating physical processes in MOS system after ionizing radiation [35].

When radiation passes through an oxide, electron and hole pairs are created by the deposited energy (process 1). Electrons are quickly swept out of the oxide due to high mobility (20 $cm^2/V{\cdot}s$ at 300 K in fused quartz), while holes with low mobility (~4×10^{-9} $cm^2/V{\cdot}s$ at 300 K) survive initial recombination and remain in the oxide. The fraction of electron-hole pairs that escape recombination is called the charge yield. The fraction depends greatly on the strength of the electric field in the oxide and the energy of the incident particle. The generation and recombination of electron-hole pairs are the first processes shown in Fig. 2.4. When the electric field is higher than 4 MV/cm, more than 80% of radiation-induced holes escape initial recombination.

The accumulated holes may be trapped in microstructural defects and pre-existing traps in the oxide. These holes may further transport to the oxide/semiconductor interface by hopping via localized states in the oxide (process 2 in Fig. 2.4) This process typically takes less than a second but may occur over many decades of time.

As the holes approach the SiO_2/Si interface, some of the holes can be neutralized by electron tunneling from the silicon, and others will be trapped at relatively deep states, forming positive oxide trap charges (process 3 in Fig. 2.4). These oxide-trapped charges can cause a shift in the threshold voltage and an increase of radiation-induced leakage current (RILC) in these devices. RILC involves an inelastic tunneling process assisted by neutral traps in the oxide. The oxide traps and interface traps cause parametric degradation and reliability issues in conventional MOS. The neutral electron trap likely originates as radiation-induced holes trapped at E' centers (oxygen vacancy) in the oxide. Electron Spin Resonance (ESR) measurements performed by P. M. Lenahan et al. have shown a link between E' centers and RILC [35].

The charges trapped in the gate oxide cause threshold voltage shifts. The positive charge reduces threshold voltage while the negative charge increases the threshold voltage. The relationship is given by [35]:

$$\Delta V_{TH} = -\frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}}\int_0^{x_0} x \cdot \rho_{ox}(x)dx, \tag{2.2}$$

where Q_i is the interface charge, ρ_{ox} is the volumetric oxide charge density, x_0 is the oxide

thickness and ε_{ox} is the oxide dielectric constant. TID effects on gate oxides are becoming less significant for advanced technology nodes with thinner gate oxide.

During process 3, protons can be released in the oxide as holes transport to the SiO_2/Si interface. The protons can drift to the Si/SiO_2 interface under positive gate bias where they may react with Si-H to form H_2, leaving silicon dangling bonds at the interface (process 4 in Fig. 2.4). These dangling bonds can act as interface traps, which are localized states in the Si band-gap. Their occupancy is determined by the Fermi level, leading to a change of threshold voltage and a decrease of carrier mobility.

For 2D material devices, the TID radiation responses have been reported recently, mainly on Graphene FETs and MoS_2 FETs [23], [39]–[42]. When the devices are capped with passivation layers, significant negative shifts in threshold voltage and degradation in mobility are observed, which is consistent with oxide hole trapping theory in conventional MOSFETs. On the other hand, for the Graphene and MoS_2 materials that are unencapsulated, positive threshold voltage shifts and carrier-mobility degradation occur. If there is no passivation layer to isolate the channel materials from the ambient environment, graphene and MoS_2 can adsorb O atoms resulting from the decomposition of ozone during X-ray irradiation. The charge of these ozone-induced electrons may dominate over hole trapping in the oxide for 2D materials.

2.2.2 Single Event Effect (SEEs)

The physical origin of SEEs is from the charge deposition and collection when high

energy particles pass through the sensitive regions of devices. Heavy charged particles (protons, alpha particles, ions) are the main SEE sources for space applications. Based on the failure type, SEEs can be classified into two categories: hard error (non-recoverable) and soft error (recoverable). Hard errors include single event gate rupture (SEGR), single event burnout (SEB) and single-event latch-up (SEL) in MOS devices [43]–[45]. Soft errors include single event upset (SEU) in a memory cell where the memory cell flips [46]. When an ion hits a device, charge is generated, which can be transported and collected, resulting in single event transient (SET) pulses at the device terminals. These sudden voltage spikes can be propagated in a circuit and cause SEUs occur in memory cells when a state '1' flips to the state '0' or vice versa. High radiation-field applications usually require radiation-hardened device [47]. Fig. 2.5 (A) shows the charge deposition by the ion and subsequent charge collection by drift and diffusion [47]. Electron/hole pairs generated in the depletion region are separated and collected efficiently, a process known as drift collection. Carriers generated close to the depletion region can diffuse to the depletion region, where they are collected by the drift process. This process is known as the diffusion process since the carriers generated outside the high-field region diffuse to the depletion region. A representative current pulse, shown in Fig. 2.5 (B), illustrates a prompt drift and a slow diffusion component.

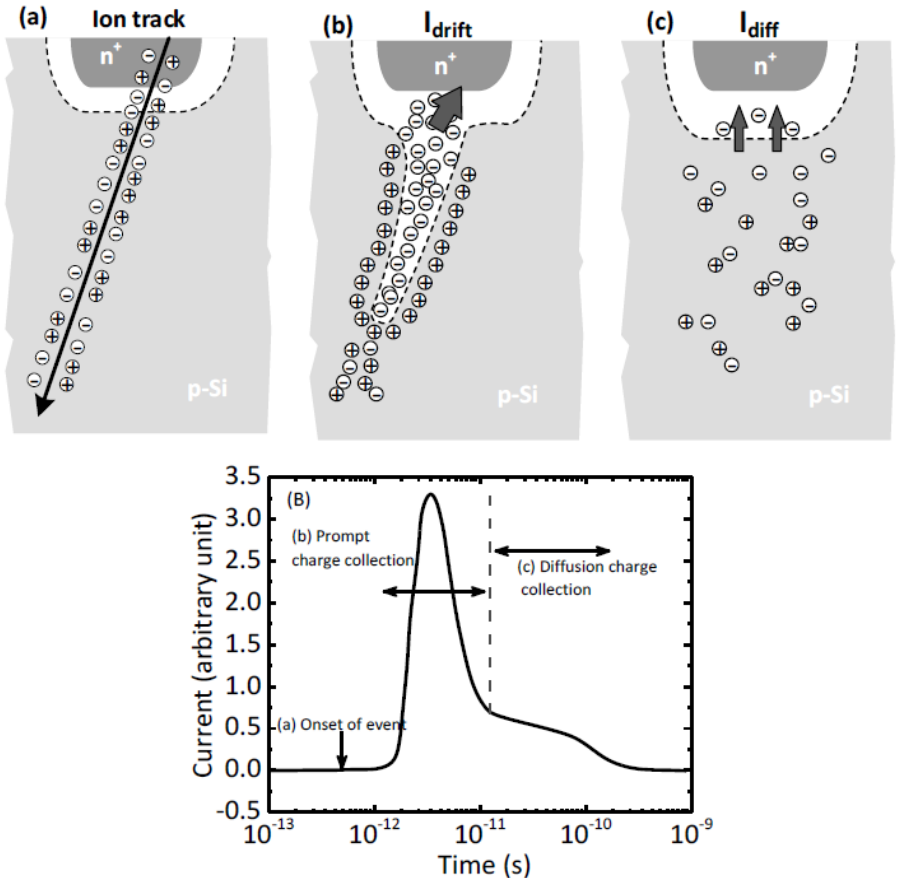


Fig. 2.5. (A) Charge generation and collection processes in a reverse biased PN junction and (B) the resultant current transient caused by the passage of a high-energy ion [47].

SEEs in traditional silicon-based electronic devices have been well-studied for decades. However, the response of 2D materials-based devices to a single event has not been fully explored. Current studies of ion beam interactions with 2D materials focus on lattice structure damage. Table 1.1 lists the impact of ions on 2D materials and related devices. To date, there have been no reports on the effects of heavy ions on BP-based devices.

Table 1.1 Reports on the impact of ions on 2D materials and related devices.

ion type	**material**	**energy**	**fluence (ions· cm^{-2})**	**impact**
proton	graphene	2 MeV	10^{15} to 6×10^{18}	vacancy and interstitial generation; surface desorption; increase in defect density [48], [49]
proton	MoS_2	10 MeV	10^{12} to 10^{14}	conductivity loss; threshold voltage shift; interface traps [50]
helium	graphene	35 keV	10^{16} to 10^{17}	graphene etching, cutting, and patterning [51]–[53]
argon	graphene, WSe_2	90 eV, 5 keV, 100 keV	10^{11} to 10^{15}	isolated defects at lower fluence and defect coalescence at higher fluence [54]
xenon	graphene	5 keV	$\sim 10^{11}$ to $\sim 10^{14}$	vacancy chain generation if angled; nanomesh generation [55]
swift heavy ion	graphene	~100 MeV	$\sim 10^{9}$	graphene folding, forming of surface tracks and hillocks [56], [57]
uranium (U28+)	graphene, MoS_2	1.14 GeV	4×10^{10} to 4×10^{11}	significant changes of structural properties; conductivity gain at low fluence and conductivity loss at high fluence [41]

Chapter 3 . BP MOSFETs

3.1 BP MOSFETs Structure and Fabrication

The back-gate BP MOSFETs used in this work are shown in Fig. 3.1 and Fig. 3.2. Back-gate MOSFETs consist of three electrodes (drain, gate and source) with a dielectric layer separating the gate electrode from the channel materials. When the device is turned on by the gate voltage, carriers flow between the source and drain electrodes through the channel. The channel material is BP which takes the place of silicon in conventional MOSFETs.

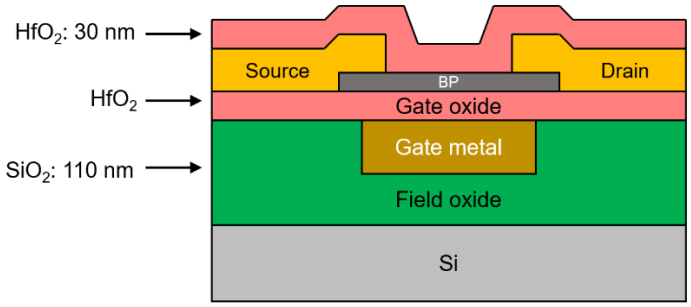


Fig. 3.1. Schematic cross-section of a BP based transistor (not drawn to scale). Current flows in the BP layer, and gate control is provided by the lower Ti/Pd electrode. Gate edges are not fully flush with the surrounding SiO_2, and small (~ 5 nm) non-planarity may exist between the gate metal and SiO_2 field oxide.

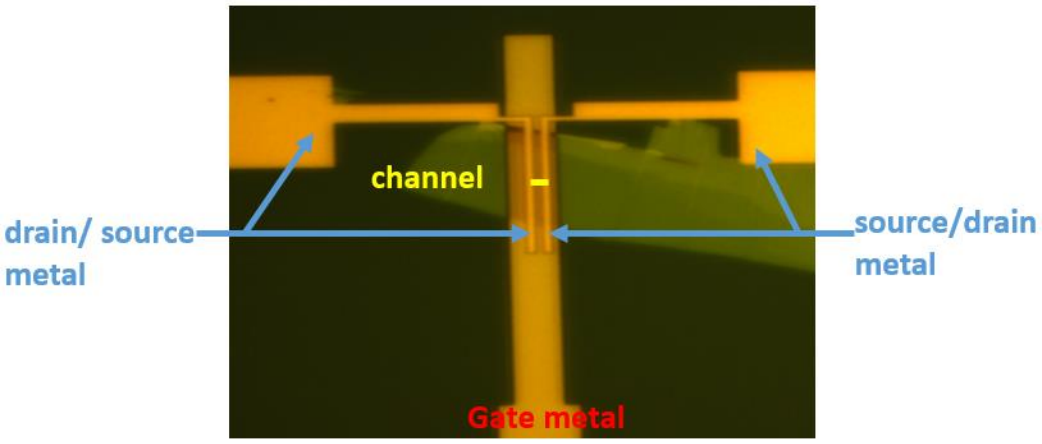


Fig. 3.2. Top view of the BP MOSFETs used in this work

Compared to silicon, BP can achieve thinner channel thickness and higher mobility at the same time, which may enable transistor scaling to sub-nm dimensions. For a transistor with thicker BP materials (more layers), the charged impurity scattering at the interface can be effectively reduced due to the screening effect [13]. Also, more layers indicate more conduction layers between the source and drain when the device is turned on. Thus, compared to thin BP, more drive current can be gained in MOSFETs with thicker BP layers when the overdrive voltage is the same. However, since the thicker BP has a smaller bandgap, the off-current is larger. Thus, a tradeoff exists between achieving large mobility and large current on/off ratio when choosing the number of BP layers [13].

The gate insulator selections vary from conventional SiO_2 to 2D insulators like hexagonal boron nitride (h-BN). Also, ambient-stable insulator materials must be applied as passivation layers around the channel BP materials as the performance of unpassivated BP transistors degrades when exposed to the atmosphere [15], [16].

Since there is no stable and reliable doping method for BP, the typical drain/source regions of BP MOSFETs are constructed with metals directly contacting the channel BP material, which induces a Schottky barrier. Compared to conventional MOSFETs with p-n junction source/drain regions, this Schottky barrier contact between the semiconducting channel and metal electrodes increases the channel resistance. Thus, achieving low contact resistivity at the source and drain regions is among the key challenges, since it is highly dependent on the metal/BP semiconductor contact interface [17]. Also, unlike other metal/2D material contacts,

the metal/BP interface is not strongly affected by the Fermi level pinning effect, and the choice of the contact metal can effectively tune the Schottky barrier heights at the interface [58]. Thus, it is possible to switch between p-type and n-type conduction through the control of the gate and drain bias, which allows ambipolar operation and the potential for CMOS integration [13].

In our work, the device is constructed on a bulk Si wafer with 110-nm thermally-grown SiO_2. A Ti/Pd metal layer is incorporated as a gate contact below the active device layers. The gate metal is almost flush with the top of the oxide, though there is a narrow "trench" at the edge of the gate. The gate dielectric consists of HfO_2 deposited using atomic layer deposition (ALD). The gate-oxide thicknesses considered are 6.8 nm and 20 nm. Few-layer BP flakes with a thickness of 8-10 nm were aligned and transferred onto the gate fingers. Ti was deposited on top of the BP flakes in the source and drain regions to form the electrodes. As Ti could easily peel off if the thickness is high, Au is deposited to avoid this issue. Finally, a passivation layer of 30 nm of HfO_2 was deposited using ALD to provide stability in the ambient atmosphere; other options for passivation materials include h-BN and Al_2O_3 to suppress the diffusion of oxidizing species. The devices have a source/drain spacing of 500 nm and device widths ranging from 3 μm to 18 μm. These fabrication steps are shown in Fig. 3.3.

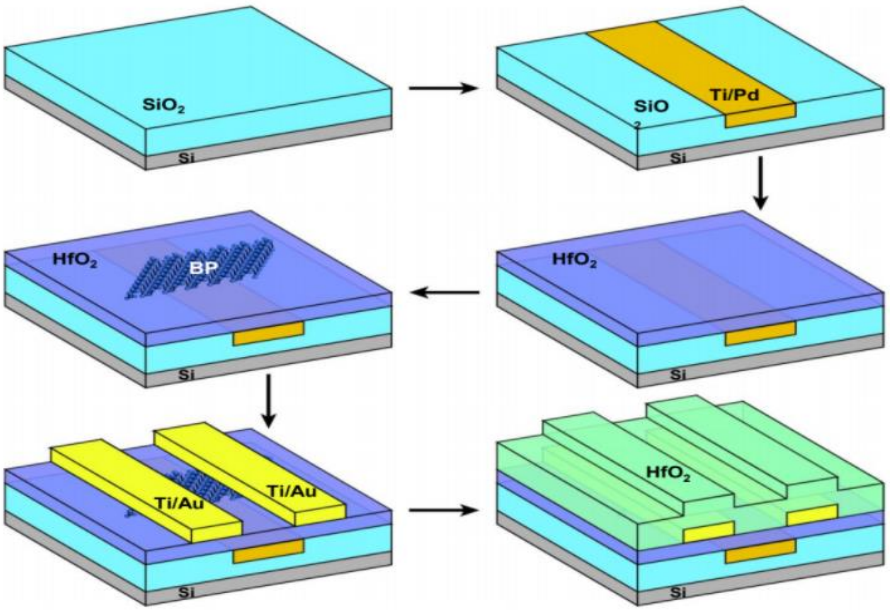


Fig. 3.3. Fabrication of the BP MOSFETs used in this work

3.2 The DC Characteristics of BP MOSFETs

3.2.1 Device Operation Mechanisms

A Schottky barrier (SB-)FET is a MOSFET in which the doped semiconductor source and drain regions are replaced with a metallic source and drain, with the actual SB junction formed at the metal-semiconductor (MS) interface. Because the SB may drastically limit the drain on-state current, BP MOSFETs typically perform more like “Schottky-Barrier Source/Drain MOSFETs” which operate fundamentally differently from conventional MOSFETs.

In the BP MOSFETs, injection of the carriers involves transport at an abrupt metal-semiconductor SB interface. Carrier injection at the interface of the source and the channel plays a more important role than carrier transport in the channel [17], [58], [59]. Two major mechanisms contribute to the carrier injection to overcome the SB: field emission (tunneling)

and thermionic emission [59]. The bias conditions control these two carrier injection mechanisms. The principle of device operation is summarized here, with an example of I_D-V_G characteristics and band diagrams.

Fig. 3.4 is an example showing the typical I_D-V_G characteristics of the BP MOSFETs. The thickness of the gate oxide is 6.8 nm, the channel length is 0.5 μm and the channel width is about 3 μm. V_{DS} is -0.1 V, and V_G is swept from 0.2 V to -1.2 V with the step = 20 mV. The DC characteristics are measured with HP 4156B and Agilent B1505 parameter analyzers.

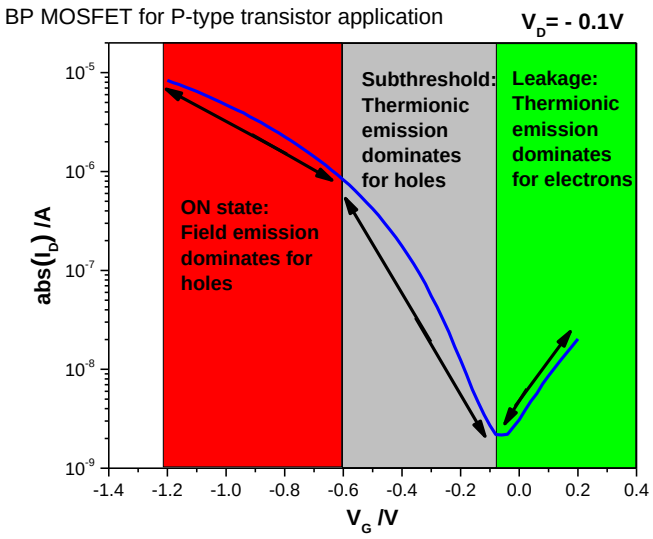


Fig. 3.4. Typical I_D-V_G characteristics of the BP MOSFETs for p-type FET applications.

Reverse leakage region for P-type application:

At gate voltages more positive than –0.1 V, the channel is in accumulation, and the reverse leakage is dominated by electrons tunneling from drain to channel through the Schottky barrier. This effect becomes more significant when the quasi-Fermi level of the drain is biased above the conduction band in the channel, as the field emission current component increases, as

shown in Fig. 3.5(b). When the electrons are in the channel, they drift under the lateral electrical field to the source/channel interface where the other Schottky barrier exists. Since this barrier is comparably small, the leakage current is controlled by the field emission from the drain to the channel.

Subthreshold region for P-type application:

When the voltage is between –0.1 V and –0.6 V, the subthreshold regime corresponding to the band diagram, the drain current is entirely induced by thermionic emission of holes over the source-channel hole Schottky barrier. In this regime, the valence band in the channel is below the tip of the Schottky contact and therefore no tunneling occurs, as shown in Fig. 3.5(c).

On region for P-type application:

With the increase of the absolute V_G value, the valence band at the source/channel interface rises and when the flatband condition occurs, the thermionic emission current reaches its maximum. Raising the valence band beyond this point will not increase thermionic emission anymore. However, the field and thermionic-field emission begin to increase, as shown in Fig. 3.5(d).

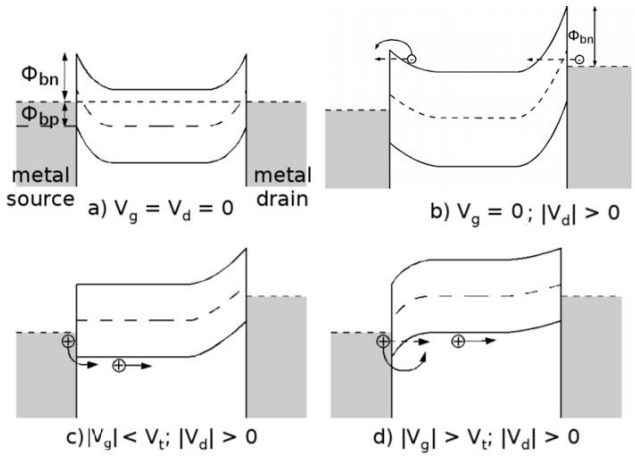


Fig. 3.5. The band diagram when the device at different biases. The solid line with arrows are the thermionic emission currents, and the dashed line with arrows are the field emission currents.

3.2.2 Temperature Dependence

Fig. 3.6 shows the I_D-V_G characteristics of the BP MOSFETs at different temperatures. The temperature range used in this work is from 90 K to 300 K. When the device is off, the leakage current increases with increasing temperature. This is because in this region, the drain current is dominated by the thermionic injection of the holes from the source. At the fixed bias condition, it is easier for the holes to climb over the barriers with higher energy (temperature). When the device is on, the dominant current is from holes tunneling from the source, so the dependence on temperature is weaker than in the off state. The data show that the temperature affects the threshold voltage and the subthreshold swing. These results are consistent with the results from other 2D material-based SB MOSFETs [58], [60].

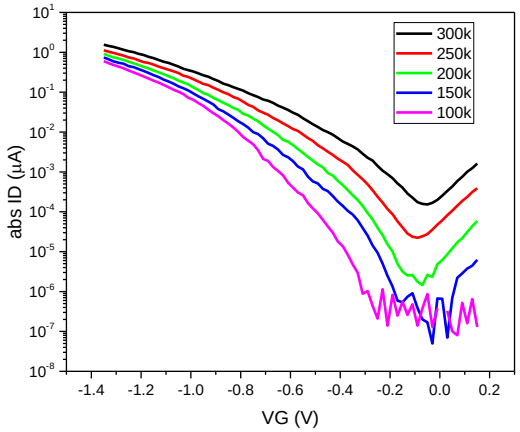


Fig. 3.6. The BP transfer characteristic dependence on temperature.

3.3 BP MOSFET Stability Issues

For BP flakes formed by mechanical exfoliation, O_2 and H_2O in the environment irreversibly react with BP to form phosphoric acid or oxidized phosphorous compounds through rapid surface oxidation. The exfoliated surface becomes rough after one hour, and it becomes obvious when the exfoliated BP crystals are exposed for 24 hours [15]. This degradation not only increases the surface roughness but also results in the formation of chemisorbed species, which can result in physical changes such as volume expansion and cleated surface, chemical changes that degrade mobility, as well as large Schottky barrier heights due to the metal-induced gap states. Meanwhile, the oxygen defects (e.g., dangling oxygen) are another reason for degradation because oxygen defects are low energy metastable forms that may introduce deep donor and/or acceptor levels in the band gap and the dangling oxygen atom can be a starting point for forming more complex defects [61]. Thus, the device performance is influenced significantly by surface degradation. The exposure of unencapsulated BP FETs in to atmosphere induces an increase in

threshold voltage, and decrease in on/off ratio and mobility, as shown in Fig. 3.7(A).

To avoid the undesired effects, passivation is needed to act as a barrier against ambient moisture. The materials that could be used as passivation layers for BP transistors includes AlO_x, HfO_2 and h-BN. The effects of AlO_x layers are shown here as an example. Positive fixed charges induce band bending, changing the polarity of the transistors from P-type to ambipolar [53], as shown in Fig. 3.7 (B). The on/off ratio of the unencapsulated device degraded rapidly upon ambient exposure while the AlO_x encapsulated device shows an on/off ratio ranging between 180 and 300 after 175 hours. Because of encapsulation and passivation of both the edge and top surface by AlO_x, a high on/off ratio of $\sim 3 \times 10^3$ and mobility of ~ 53 $cm^2V^{-1}s^{-1}$ were maintained for over two weeks under ambient conditions, as shown in Fig. 3.7 (C)-(F).

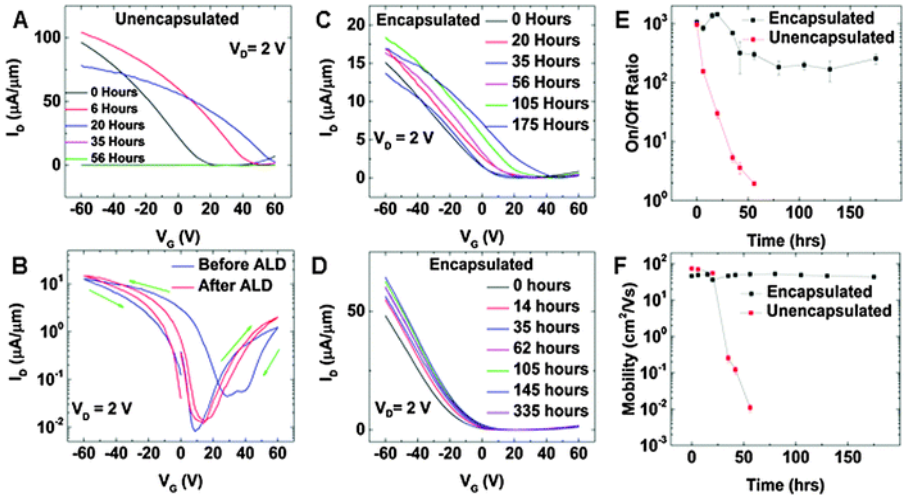


Fig. 3.7. Time dependence of few-layer BP FET device characteristics. (A) Transfer curves for an unencapsulated BP FET with Ti/Au contacts, measured as a function of ambient exposure time. (B) Transfer curves for a BP FET measured immediately before and after encapsulation. (C) Transfer curves for a ~30 nm thick ALD AlO_x encapsulated BP FET with Ti/Au contacts, measured as a function of ambient exposure time. (D) Transfer curves for a ~30 nm thick ALD AlO_x encapsulated BP FET with Ni/Au contacts, measured against the ambient exposure time. Comparison of the (E) I_{on}/I_{off} ratio and (F) hole mobility for encapsulated and unencapsulated Ti/Au BP FETs *versus* ambient exposure time [15].

In this work, 30 nm thick HfO_2 is deposited using ALD as a passivation layer. The transfer characteristics of these passivated BP MOSFETs are stable in the ambient environment for weeks [58], [59]. However, the devices show degradation after storage in ambient conditions for months, as shown in Fig. 3.8. The hysteresis window increases from 0.5 V to 2.5 V after storage, due most likely to an increase in density of border traps. Also, the on current decrease significantly after storage, which is consistent with the results reported in [15].

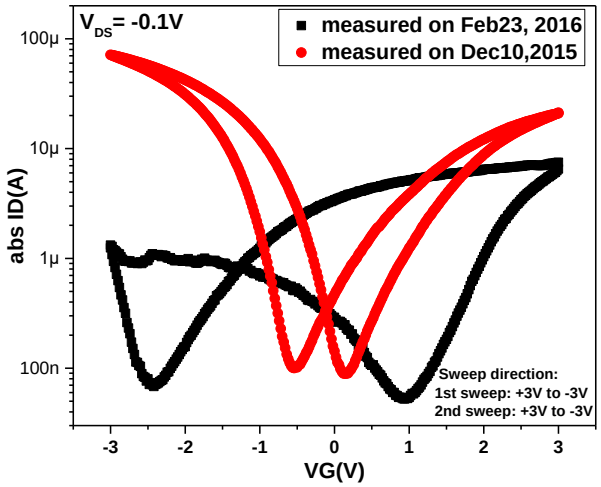


Fig. 3.8. The transfer curves of BP MOSFETs passivated with 30 nm thick HfO_2. Measured before and after 73-day storage in ambient environment.

Chapter 4 . Radiation-induced Degradations on BP MOSFETs

In this chapter, changes in the device characteristics due to electrical stress, 10-keV x-ray irradiation, proton irradiation, and annealing are evaluated for HfO_2-passivated black phosphorous (BP) MOSFETs with HfO_2 gate dielectrics. Device performance is evaluated before radiation testing to determine the stability. Threshold, mobility, and subthreshold swing are characterized during both positive and negative bias irradiation. Switched-bias annealing after irradiation is evaluated to study the charge trapping mechanisms.

4.1 Experiment Setup

4.1.1 DC characterization of the samples

The detailed device structure and fabrication process are described in Chapter 3.1. The wafers were first diced to individual dies. Then each die, containing the isolated BP MOSFETs, was mounted on a high-speed package. After packaging, an HP 4156A Semiconductor Parameter Analyzer is used for characterizing the packaged devices. A grounded wrist strap was always used while handling the devices. We evaluated two types of BP MOSFETs with different gate oxide thickness (20 nm and 6.8 nm). The data shown are representative of at least two samples for each experimental condition, which exhibited similar responses.

Fig. 4.1 shows typical device characteristics with 20 nm thick gate oxide. Fig. 4.1.(a) shows drain current as a function of gate voltage for drain voltages from 0 V to -1.5 V, with a 0.1 V step, and Fig. 4.1.(b) shows output characteristics for drain voltages ranging from 0 V to -1.5

V and gate voltages from -1.5 V to 3 V with a step of 0.1 V. The results are similar to those of other BP FETs in the literature [61], [62], demonstrating ON/OFF ratios of greater than 100 and current drive capability above 100 μA.

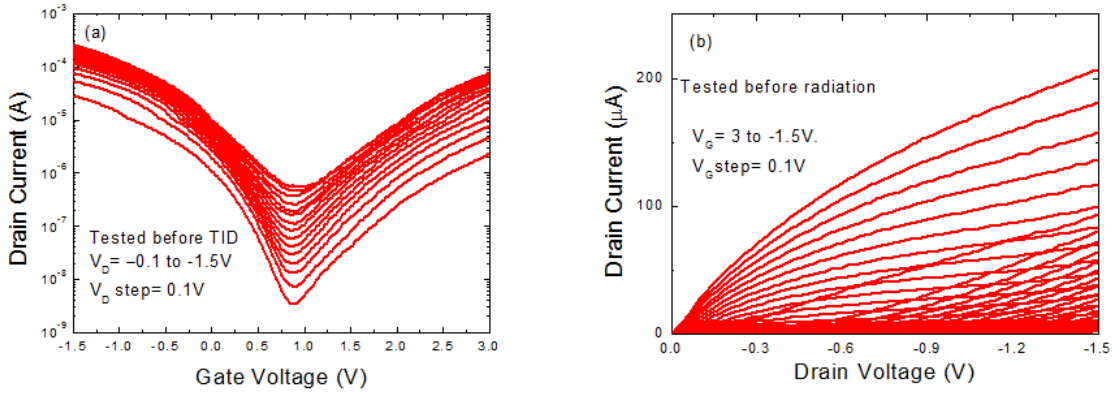


Fig. 4.1. Typical characteristics of the devices with 20 nm gate oxide: (a) I_D-V_G curves for drain voltages from 0 V to -1.5 V with a step of 0.1 V, and (b) I_D-V_D curves at gate voltages from -1.5 V to 3 V with a step of 0.1 V.

Fig. 4.2 shows typical device characteristics with 6.8 nm thick gate oxide. Fig. 4.2 (a) shows drain current as a function of gate voltage for drain voltages from 0 V to -1 V, with a -0.1 V step, and Fig. 4.2 (b) shows output characteristics for drain voltages ranging from 0 V to -1 V and gate voltages from 0.4V to -1.4 V with a step of -0.1 V.

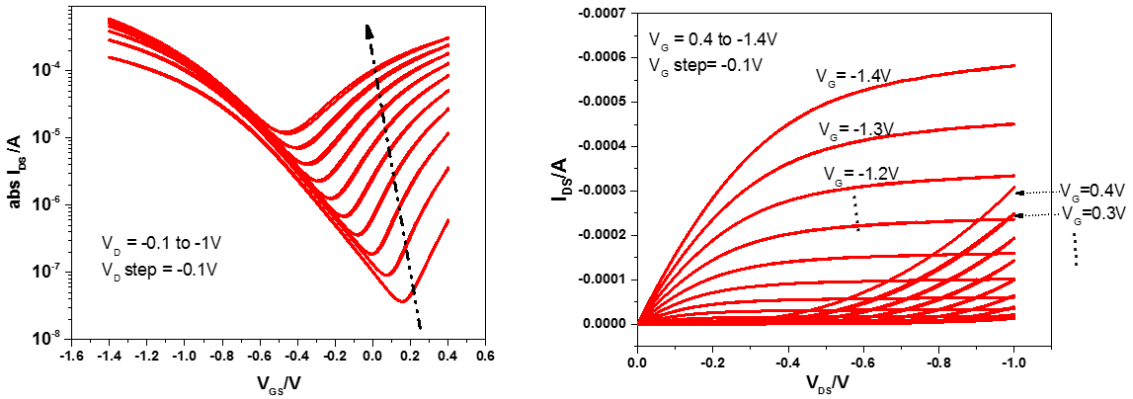


Fig. 4.2. Typical characteristics of the devices with 6.8 nm gate oxide: (a) I_D-V_G curves for drain voltages from -0.1 V to -1V with a step of 0.1 V, and (b) I_D-V_G curves at gate voltages from 0.4 V to -1.4 V with a step of 0.1 V.

4.1.2 X-ray Irradiation

The BP transistors were irradiated with a 10-keV ARACOR x-ray source at a dose rate of 30.3 krad(SiO_2)/min at room temperature in air with applied gate bias, with drain and source grounded. Device responses after radiation exposure were evaluated in-situ at room temperature. The DC electrical measurements were performed with a HP 4156A Semiconductor Parameter Analyzer.

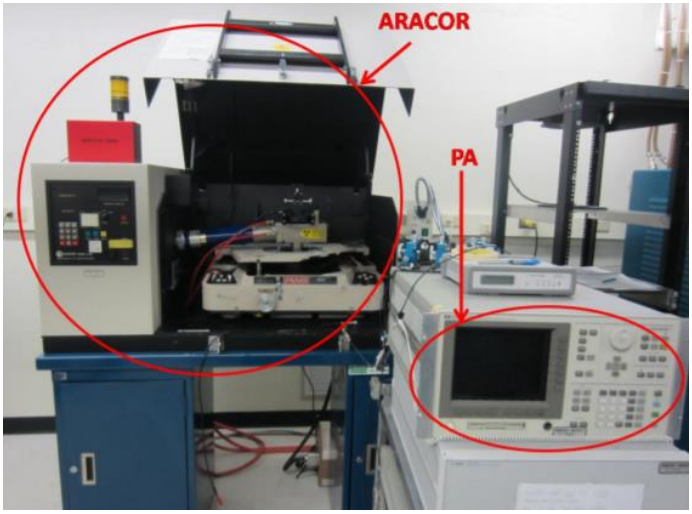


Fig. 4.3. X-ray irradiation setup.

4.1.3 Proton Irradiation

The BP transistors were irradiated in the Vanderbilt Accelerator Laboratory using a Pelletron. 1.8 MeV proton irradiation is used in this work. The fluences considered range from 1×10^{11} cm^{-2} to 1×10^{14} cm^{-2}, which is a very high particle fluence relative to typical space applications. The voltage bias conditions on the devices are the same as those for the X-ray irradiation. DC measurements are taken right after the proton beam is turned off at each fluence step using the Parameter Analyzer.

Fig. 4.4. Vanderbilt Pelletron Test Setup.

4.2 DC Characterization of X-ray Irradiation on BP MOSFETs

4.2.1 X-ray Irradiation for BP MOSFETs with 20 nm Gate Oxide

The stability of the BP MOSFETs with 20 nm gate oxide with applied bias is illustrated in Fig. 4.5, which plots the drain current vs. the gate voltage. The left-hand branch of the curve corresponds to hole conduction and the right-hand branch to electron conduction. The drain current is measured when the gate voltage is swept from 3 V to -1.5 V in air at room temperature. During electrical stress, the devices were kept at a constant gate voltage of +1 V or -1 V with all other terminals grounded. Measurements were taken after the accumulated stress times shown in the legend of Fig. 4.5. Each measurement takes less than 10 s, so stressing effects are negligible during *IV* sweeping. Fig. 4.5(a) shows the drain current I_D at V_{SD} = 100 mV vs. gate voltage V_G

as a function of time for +1 V bias-stress. A small positive shift in the $I_D - V_G$ characteristics occurs, most likely due to electron trapping at or near the interface of the gate-HfO_2/BP layer. Similar effects of charge transfer occur in other 2D semi-conductor MOSFETs with similar device structures [28], [29], [40], [63]. For -1 V bias-stress in Fig. 4.5(b), even less shift is observed. These results demonstrate the stability of these HfO_2-passivated BP transistors with HfO_2 gate oxides.

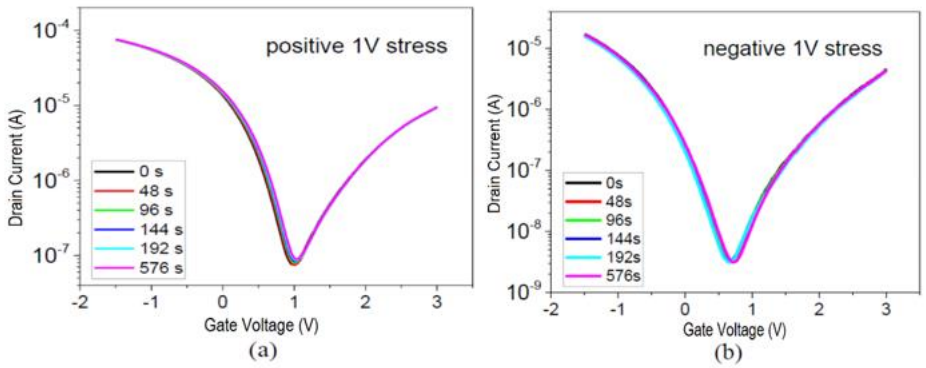


Fig. 4.5. Drain current I_D as a function of stress time with applied gate bias of (a) + 1 V and (b) − 1 V. V_{SD} = 100 mV during the measurement of the *IV* characteristics.

Fig. 4.6 shows the drain current I_D at V_{SD} = 100 mV vs. gate voltage V_G as a function of total dose and annealing time at room temperature. The devices were irradiated up to 1 Mrad(SiO_2) at a gate bias of ±1 V, with all other terminals grounded. For the negatively biased devices, there is an initial, small positive shift in the curves, which is evidence either of a small amount of electron trapping, or passivation of a small amount of process induced charge. The $I_D - V_G$ characteristics under both biases shift negatively at higher doses, however, and the

slopes of the $I_D - V_G$ curves increase in magnitude with increasing dose. The significant negative voltage shifts in Fig. 4.6 (a) and (b) are due primarily to net radiation-induced hole trapping in the relatively thick HfO_2 gate oxide layers, where the applied electric field is much higher than the fringing field in the upper (ungated) HfO_2 passivation layer. After irradiation, the same gate bias is applied to the devices for 0.5 h to check for room-temperature annealing. Fig. 4.6 (a) and (b) show that very little $I_D - V_G$ recovery is observed. After annealing in air for 20 days, the $I_D - V_G$ characteristics recover approximately to the values observed at 500 krad(SiO_2), as shown in Fig. 4.6 (a), as a result of significant trapped-hole annealing. The slight reduction in subthreshold slope after this long-term, unbiased anneal is most likely due to a decrease in charge lateral non-uniformities (LNUs) [64] or to a reduction in border-trap density [65]. Biased annealing effects are discussed further below.

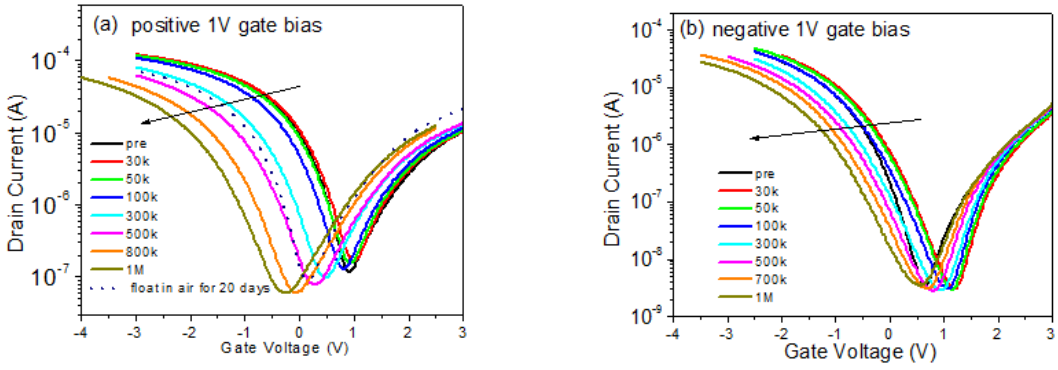


Fig. 4.6. Drain current I_D as a function of total dose with applied gate bias of (a) + 1 V and (b) − 1 V. V_{SD} = 100 mV during the measurement of the *IV* characteristics.

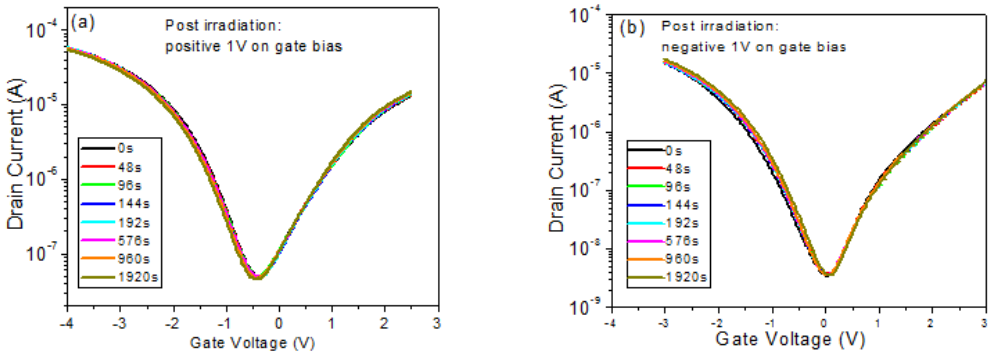


Fig. 4.7. Drain current I_D as a function of annealing time with applied gate bias of (a) + 1 V and (b) − 1 V. V_{SD} = 100 mV during the measurement of the IV characteristics.

Fig. 4.8, Fig. 4.9, and Fig. 4.10 show threshold voltage shifts ΔV_{th}, changes in field-effect mobility and subthreshold swing ($SS = dV_G/d(logI_D)$) as functions of total ionizing dose at gate biases of ±1 V. The application of positive gate bias during irradiation results in more charge trapping than negative bias, attributable to (1) the much higher electric field in the region between the gate Ti/Pd electrode and the BP than the field in the upper passivation layer, and (2) the greater effects of hole trapping in the gate HfO_2 layer on ΔV_{th} for positive bias irradiation than under negative bias irradiation, similar to what is observed in typical Si-based MOS transistors.

The field effect mobility is extracted within the linear range of transistor response using $\mu = g_m \times (\frac{L}{W C_{ox} V_{DS}})$ where C_{ox} is the oxide capacitance and g_m is the peak of the device transconductance. Before irradiation, the field effect mobility is about 30 $cm^2/V{\cdot}s$. After irradiation, the mobility degrades to about 60% of the pre-irradiation value. Such large degradation in mobility is consistent with the generation of positively charged defects at/near the

interface. These defects act as Coulomb scattering centers and degrade the carrier mobility. Values of *SS* as a function of dose are also extracted and normalized by the pre-irradiation value, as shown in Fig. 4.10. The value of *SS* increases by ~ 65% for both positive and negative bias irradiations. The *SS* value is degraded primarily by radiation-induced defects at the interfaces between the BP and surrounding HfO_2 layers. The increase of the subthreshold swing indicates that interface traps are created by irradiation. Under positive gate bias, it is likely that these interface traps form at the lower BP/HfO_2 (gate) interface, while under negative gate bias, it is quite possible that interface traps also are formed at the upper BP/HfO_2 (passivation) interface, consistent with the directions of H^+ transport in surrounding dielectric layers. The resulting degradation in mobility is similar to that observed in irradiated graphene and MoS_2 devices in previous work [39], [42].

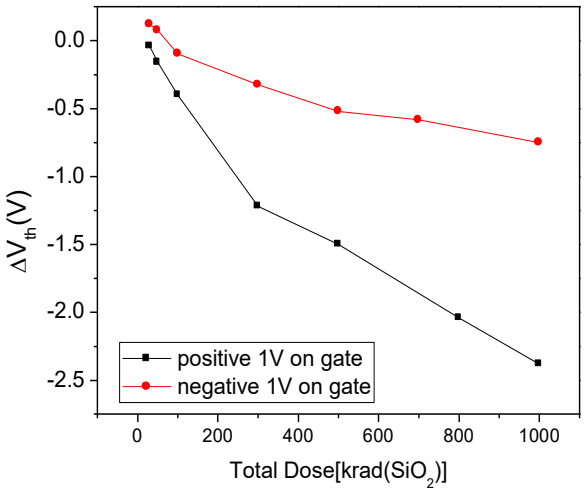


Fig. 4.8. Threshold voltage shift ΔV_{th} as a function of total dose for devices irradiated to 1.0 Mrad(SiO_2) with an applied gate bias of ± 1 V.

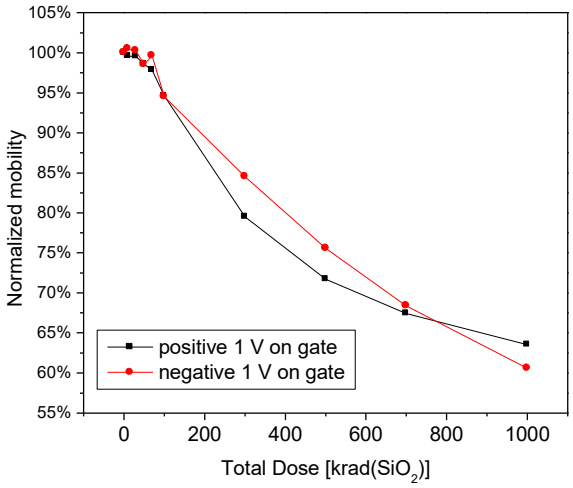


Fig. 4.9. Field-effective mobility as a function of total dose for the devices and irradiation conditions of Fig. 4.8.

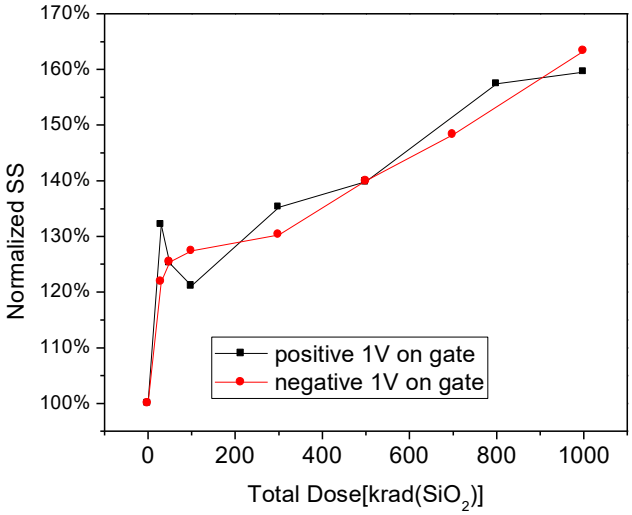


Fig. 4.10. Subthreshold swing as a function of total dose as a function of total dose for the devices and irradiation conditions of Fig. 4.8

4.2.2 X-ray Irradiation for BP MOSFETs with 6.8 nm Gate Oxide

Thinner oxide is preferred from the perspective of device scaling and low power performance. In this section, the TID response of the BP MOSFETs with the oxide thickness of 6.8 nm is reported. From the experimental results of the previous section, positive gate bias

during the X-ray irradiation induces larger device characteristic shifts. As a result, we use the positive gate bias condition to study the X-ray irradiation effect on the transistor with 6.8 nm gate oxide and compare the results to those with the gate oxide thickness of 20 nm. The applied voltage also scales to +0.34 V with the scaling of the gate oxide to ensure the electrical field within the gate oxide is approximately the same for these two types of transistors.

The stability and TID responses of these devices are shown in Fig. 4.11. V_{th} = -0.03 V for the device before stress. Fig. 4.11 (a) shows the drain current at V_{SD} = 100 mV vs. gate voltage before and after +0.34 V gate bias stress for 30 minutes at room temperature in air. A small negative shift in the I_{SD}-V_{GS} characteristics is found, most likely as a result of hole trapping and/or passivation of a small amount of process-induced charge [40],[66] at or near the interface of the gate HfO_2/BP layer. Fig. 4.11 (b) shows the drain current at V_{SD} = 100 mV vs. gate voltage as a function of dose at room temperature. The devices were irradiated to 500 krad(SiO_2) at a gate bias of +0.34 V, with all other terminals grounded. The I_{SD}-V_{GS} characteristics shift negatively. Two curves are shown for each dose, corresponding to forward and reverse voltage sweeps. The negative voltage shifts in Fig. 4.11 (b) are due to net radiation-induced trapped-positive charge trapping in the HfO_2 gate oxide [65],[67] for which the applied electric field is much higher than the fringing field in the upper (ungated) HfO_2 passivation layer. The hysteresis window increases slightly from 0.02 V before irradiation to 0.05 V after 500 krad(SiO_2), indicating that border traps are activated during irradiation [65]. After irradiation, the same gate bias is applied to the devices for 30 minutes to check for room-temperature annealing. Very little

I_{SD}-V_{GS} recovery is observed.

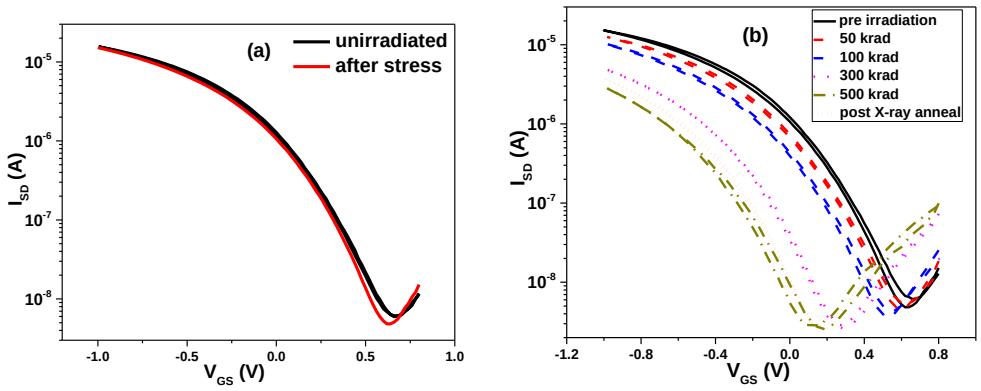


Fig. 4.11. (a) Drain current before and after gate bias of + 0.34 V stress for 30 mins in room ambient. (b) Drain current I_{SD} as a function of total dose with applied gate bias of +0.34 V. V_{SD} = 100 mV during the measurements of the *I-V* characteristics in (a) and (b).

Fig. 4.12(a) and (b) show threshold voltage shifts ΔV_{th} and mobility degradation as functions of dose at gate biases of +0.34 V during irradiation. Net trapped positive charge causes the I_{SD}-V_{GS} characteristics to shift negatively [16]. A V_{th} shift of -0.16 V is observed for 6.8 nm gate oxide transistors at 100 krad(SiO_2), in contrast with a -0.43 V V_{th} shift for 20 nm HfO_2 gate oxides. If these shifts were caused entirely by hole trapping, and if the defect densities were otherwise identical in the thicker and thinner oxides, one would expect a $1/t_{ox}^2$ dependence, due to geometry and moment arm effects [65]. However, the oxides were formed during different deposition runs, and HfO_2 gate dielectrics trap both electrons and holes [65],[68],[69], so it is quite likely, based on this result and the low-frequency noise results presented below, that the relative percentages of trapped positive and negative charge [70] in these 6.8 nm oxides differ substantially from percentages in the 20 nm oxides. This difference in defect densities almost certainly accounts for the deviation from a purely geometric $1/t_{ox}^2$ dependence between the 6.8

nm oxides and the 20 nm oxides.

Fig. 4.12 (b) shows field effect mobility normalized by the pre-irradiation value as a function of dose. This large degradation in mobility is consistent with the generation of a high density of interface and/or border traps. These defects act as Coulomb scattering centers and degrade carrier mobility. Under positive gate bias, interface/border traps likely form at the lower BP/HfO_2 (gate) interface, consistent with the direction of H^+ transport in surrounding dielectrics [21]. The resulting degradation in mobility is qualitatively similar to that observed in other irradiated 2D-material transistors [40], and with BP devices with 20 nm HfO_2 gate oxide.

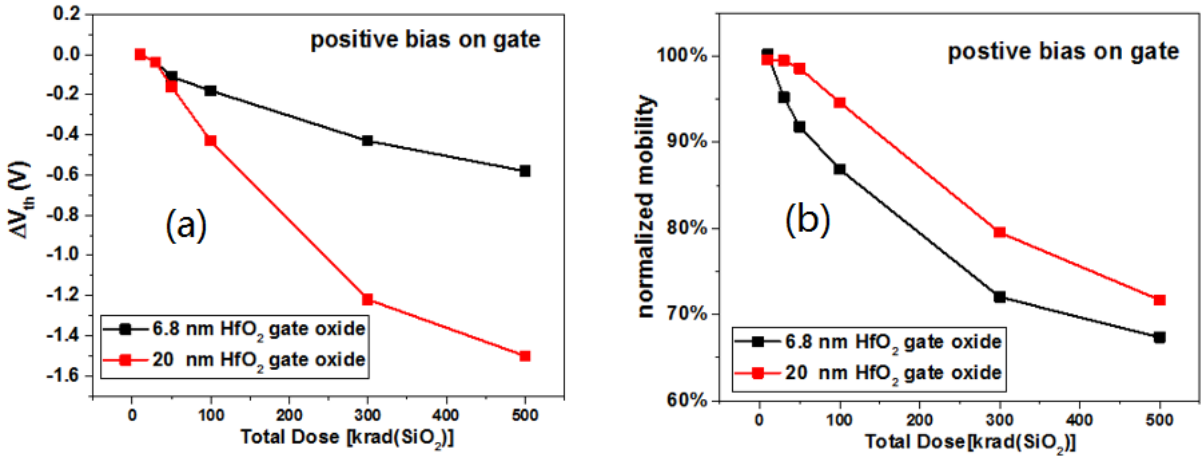


Fig. 4.12. (a) Threshold voltage shift ΔV_{th} and (b) normalized field effect mobility as functions of total dose for devices with 6.8 nm and 20 nm HfO_2.

4.2.3 Switched Bias Annealing after X-ray Irradiation

The charge trapping characteristics of these devices are further investigated by considering switched-bias annealing after irradiation for the BP MOSFETs with the 20 nm gate oxide [71], [72]. The test sequence is shown in Fig. 4.13.

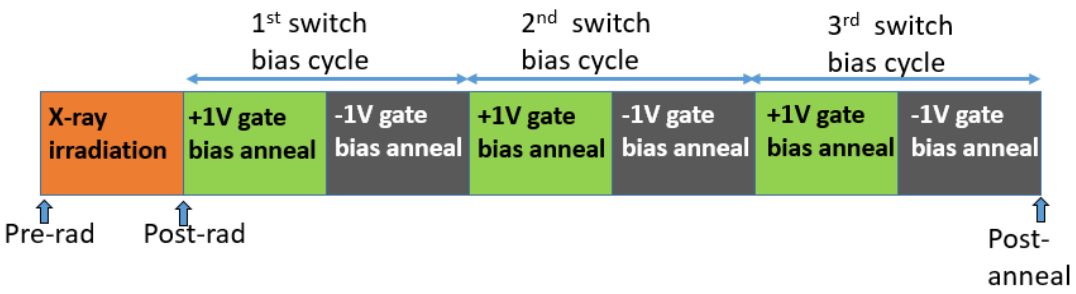


Fig. 4.13. Radiation and switch bias test sequence.

Fig. 4.14 shows the reversible threshold voltage change under alternating ±1 V switched bias annealing after devices were irradiated to 1.0 Mrad(SiO_2). The devices were annealed at room temperature for 2290 s for each ±1 V cycle shown in Fig. 4.14. The net oxide-trapped charge inside the gate HfO_2 layer increases in magnitude during negative-bias annealing and decreases in magnitude during positive-bias annealing. This is a classic pattern observed many times in both SiO_2 and HfO_2 gate dielectrics [73]–[75], which is caused by the trapping of predominantly positive charge in the HfO_2 layer, followed by the tunneling of electrons into compensating defects in the near-interfacial HfO_2 during positive-bias anneal and emission of electrons from compensating traps during negative-bias anneal [73]–[75]. Fig. 4.15 shows that mobility increases (decreases) and SS decreases (increases) during negative (positive)-bias annealing. These reversible shifts indicate that both interface and border traps contribute to carrier scattering and *IV* stretch out in these devices, again consistent with the responses of typical Si-based MOS devices to similar irradiation and annealing sequences [72]–[74], [76].

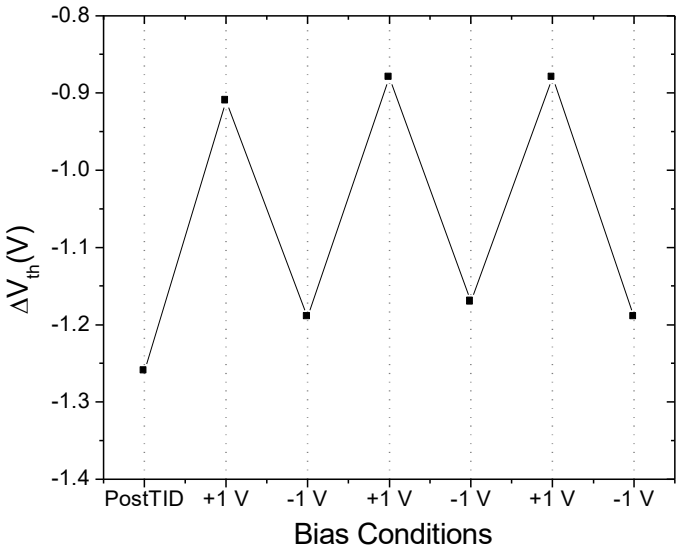


Fig. 4.14. V_{th} shifts as a function of switched bias annealing. Devices were irradiated to 1.0 Mrad(SiO_2) at 1 V, and then annealed at room temperature for 2290 s for each ± 1 V cycle.

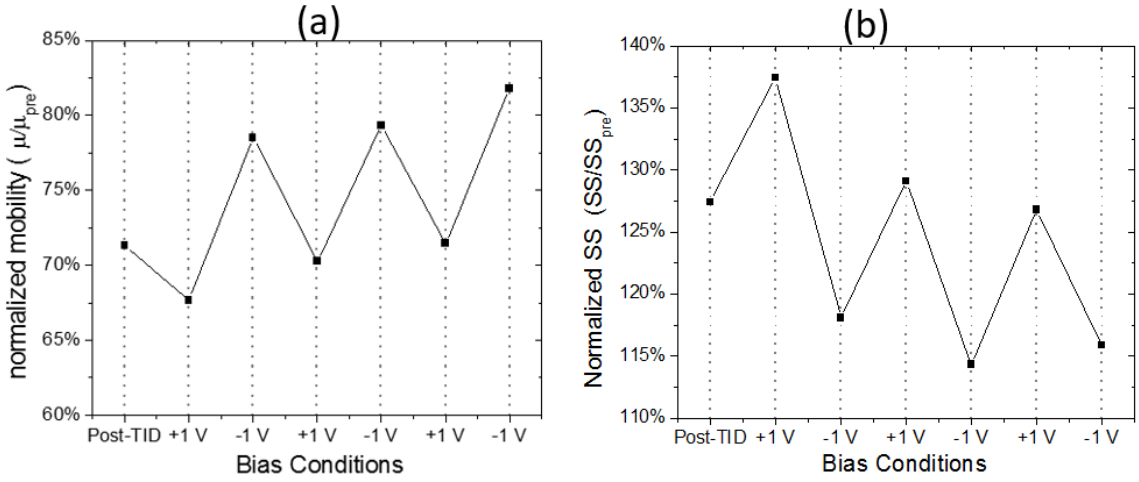


Fig. 4.15. Normalized (a)mobility (b) SS for the devices, irradiation, and annealing conditions of Fig. 4.13.

4.3 DC Characterization of Proton Irradiation on BP MOSFETs

Proton radiation testing of devices with 20 nm-thick gate oxides was performed. The gate is biased at +1V with source and drain grounded during irradiation. Fig. 4.16 (a) shows the transfer characteristic shift with the increase of the proton fluence. Two curves are shown for each fluence, corresponding to forward and reverse voltage sweeps. The first sweep is the

reverse sweep and the second sweep is the forward sweep. At first the $I_D - V_G$ curves did not change substantially following the proton irradiation to a small fluence of 3×10^{11} cm^{-2}. However, the performance was influenced noticeably when devices were irradiated to higher proton fluences. The current decreased dramatically at high fluences. The current decreased from ~10 μA (before proton irradiation) to ~0.1 μA (after proton irradiation) when devices were measured at V_{DS} = 0.1 V and V_G = -2 V, as shown in Fig. 4.16. The subthreshold slope of the device after proton irradiation to 10^{14} cm^{-2} became worse. Such degradation of the subthreshold slope after high-fluence proton beam irradiation is attributed to the proton beam-induced trap states at or near the interface. This degradation is much larger than that during X-ray irradiation, which suggests more interface/border traps are activated. Also, a negative $I_D - V_G$ curve shift occurs after proton irradiation. This results from the net positive charge trapped in the gate oxide, which is similar to the X-ray induced net positive charge discussed in Chapter 4.2.1 and 4.2.2. Also, there is an increase of the hysteresis window from 0 V in the pre-irradiation state to 1 V after a proton fluence of 10^{14} cm^{-2}. The increase of the hysteresis suggests the increase of the density of trapped charges accumulated near the interface.

When high-energy particles are incident on materials, they lose the majority of their energy near the stopping region. The energy-loss depth profiles of the protons was calculated using Stopping and Range of Ions in Matter (SRIM 2008) software [77]. From the simulation

results, 1.8 MeV protons could penetrate and stop ~42 μm from the top surface of the device, which exceeds the device channel region of our BP MOSFETs. Thus, the majority of protons could simply penetrate through the entire structure, generating electron and hole pairs along the path of the proton beam. When high-energy particles such as electrons and protons are incident on silicon-based FETs, they can ionize atoms and generate electron and hole pairs in the gate oxide layer, which is the layer that is most sensitive to ionizing irradiation. The generated electrons are quickly swept out of the bulk HfO_2 and the remaining holes are trapped at localized trap sites in the bulk HfO_2, leading to positive oxide-trapped charges. Similarly, the radiation-induced holes and protons in the HfO_2 can transport to the HfO_2/BP interface, leading to the formation of interface traps, which are positively charged for p-channel transistors [78]. Also, carrier mobility is reduced from the trapped charges at the interface due to Coulomb scattering.

The annealing of the BP MOSFETs after proton irradiation was examined. The bias condition is the same as that during irradiation. The measurement is conducted in vacuum at room temperature. Fig. 4.16 (b) shows the recovery of the subthreshold swing and threshold voltage. After annealing for 170 h, the $I_D - V_G$ curves and subthreshold swing partially recover. The recovery of the current indicates that a large portion of the radiation-induced traps is recoverable. During the irradiation and annealing processes, the gate currrent is monitored and no changes are observed through the whole process.

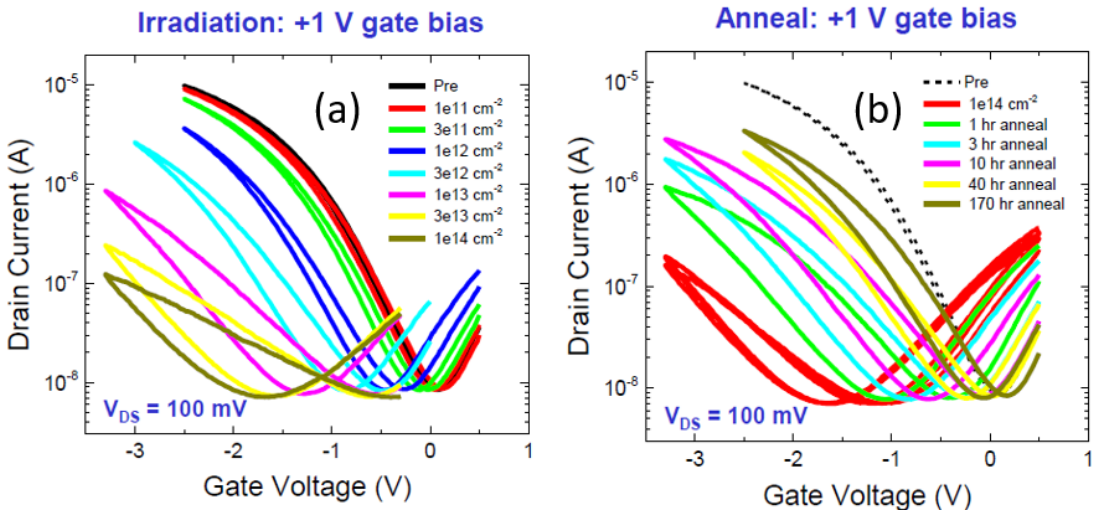


Fig. 4.16. (a) Drain current I_D as a function of total fluence with an applied gate bias of + 1 V. V_{DS} = 100 mV during the measurement of the *IV* characteristics. (b) Drain current I_D as a function of total fluence with an applied gate bias of + 1 V for annealing.

4.4 Conclusions

The total-ionizing-dose radiation response of HfO_2-passivated BP transistors with different HfO_2 gate dielectrics at X-ray doses up to 500 krad(SiO_2) was examined. Excellent stability of these structures is observed under bias stress before irradiation. Net positive oxide-trap charge buildup is observed in the HfO_2 gate dielectric layer; mobility and subthreshold swing degrades after radiation exposure, with shifts similar to those expected for Si MOS transistors with similar dielectric/passivation layer. Relatively large oxide and interface-trap charge densities are observed, owing to the gate oxide. Net positive oxide-trap charge buildup decreases approximately as $1/t_{ox}$ when the HfO_2 dielectric layer thickness decreases from 20 nm to 6.8 nm. The reversibility of these DC parameters during post-irradiation switched-bias annealing is similar to that observed in MOS transistors with SiO_2 gate dielectrics, and is associated with trapping of compensating electrons during positive-bias annealing, and

detrapping of electrons during negative-bias annealing. In the proton irradiation, we observed similar threshold voltage shift compared to x-ray radiation. These results confirm that, with continuing process improvement, it should be possible to develop stable, radiation-tolerant BP-based transistors for use in space environments.

Chapter 5 . Low Frequency Noise of BP MOSFETs

5.1 Low Frequency Noise Theory

Any resistive system exhibits noise. It is often found that in addition to the well understood thermal noise and shot noise, there is an "excess noise" with magnitude S_V, and the frequency exponent $0.7 < \alpha < 1.3$ where:

$$\alpha = -\partial ln(S_V)/\partial ln(f) \tag{5-1}$$

Here S_V is the excess noise after the thermal noise is subtracted. This excess noise is called low frequency noise, $1/f$ noise or flicker noise. Fig. 5.1 shows a typical drain voltage noise power spectral density (S_V) versus frequency of CMOS. At low frequency, the noise is dominated by the flicker noise; when the frequency is higher, the dominant noise is thermal noise.

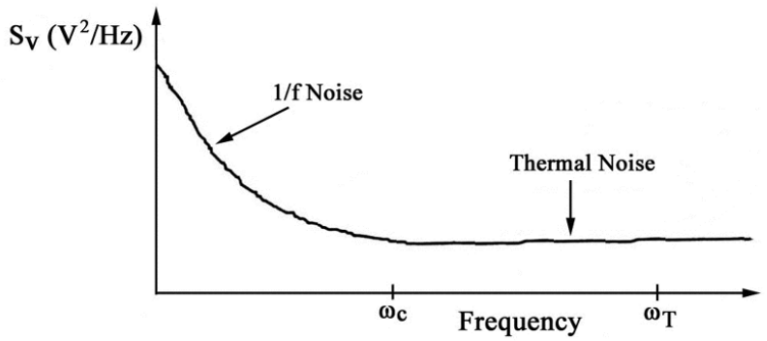


Fig. 5.1. Schematic variation of S_V with frequency, showing the dominant $1/f$ noise at low frequencies, and dominant thermal noise at high frequencies[79].

Since low frequency noise increases when the dimension of devices decreases, it could be a problem for nanoscale devices. The origins of flicker noise have been investigated and the noise spectrum in MOSFET is attributed to the defects within the device. As a result, low frequency noise measurements can be used to obtain insight into the densities, energies, and microstructures of defects in microelectronic devices [80]].

5.1.1 The McWhorter Model (Number Fluctuations)

The carrier number fluctuation model is also called the trapping and detrapping model, proposed by McWhorter [67], in which the low frequency noise is attributed to carrier number fluctuations in the channel. McWhorter obtained the $1/f$ spectrum by assuming that the time constant τ of the surface states varied with a $1/\tau$ distribution. That is, $1/f$ characteristics superpose many different spectra of random telegraph signal (RTS) noise, where free carriers are randomly trapped and detrapped by trap centers in the gate oxide with different lifetimes [81]]. This is because carrier tunneling to trap centers decreases exponentially with the distance from the surface. For an MOS structure, the traps exchange carriers with the channel, giving rise to fluctuations in the inversion charge density, which in turn causes the noise in the drain current.

In experiments the excess drain voltage noise power spectral density (PSD) of the devices operated in the linear region in strong inversion can be measured. In strong inversion, if an MOS

device is operated in its linear region at constant drain current and gate bias, the $1/f$ noise can be described by

$$S_V(f, V_D, V_G) = \frac{K}{f^\alpha} \frac{V_D^2}{(V_G - V_{th})^\beta}, \quad (5\text{-}2)$$

where S_V is the excess drain-voltage noise power spectral density, V_{th}, V_G, and V_D are the threshold, gate, and drain voltages, and f is the frequency.

A strong correlation has been shown between the $1/f$ noise of MOS transistors and oxide-trap charge in SiO_2, whereas no correlation is generally observed between low frequency $1/f$ noise and interface-trap charge [78]]. The $1/f$ noise of n-channel MOS devices increases with increasing oxide-trap charge during irradiation and decreases with decreasing oxide-trap charge during post irradiation annealing. Like hole trapping generated by negative bias-temperature stressing, the radiation-induced-hole trap was also identified as an E' center, as introduced in Section 2.1. Thus, reducing the number of oxygen vacancies in the oxide can significantly reduce the $1/f$ noise of MOS devices.

5.1.2 The Dutta-Horn Model

The magnitude and frequency dependence of the noise of metal films can vary strongly with temperature. Dutta and Horn [82]] proposed that the $1/f$ spectrum in metals is caused by a broad distribution of activation energies. This technique was applied first to analyze the nearly $1/f$ spectrum of noise in thin metal films, and then extended to Si and compound-semiconductor-

based microelectronic devices and materials.

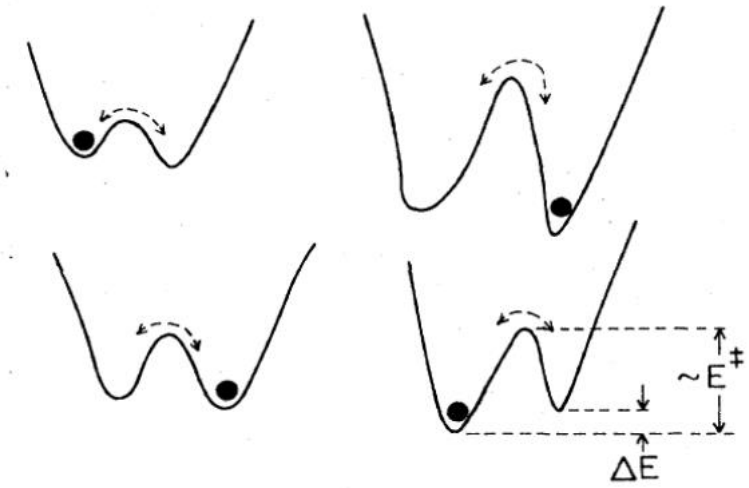


Fig. 5.2. The distinction between the two energies: the energy difference between the states (ΔE) and thermal activation energy ($E^{\pm}$)for a two-level system in the classical regime [82].

The noise is the result of thermally activated processes involving two energy levels separated by an energy barrier of $E^{\pm}$ or E_0 that the system must overcome for the system to move from one configurational state to another, as shown in Fig. 5.2. A single two-state system can be characterized by two energies: the energy difference between the states, ΔE, and the thermal activation energy for making the transition $E^{\pm}$, which is inferred from the temperature dependence of the noise. The defects have an energy distribution $D(E_o)$. The frequency exponent shows a temperature dependence described by:

$$\alpha(\omega,T) = 1 - \frac{1}{\ln(\omega\tau_0)}\left(\frac{\partial \ln S_V(T)}{\partial \ln T} - 1\right). \tag{5-3}$$

Here S_V is the excess voltage-noise power spectral density after the thermal noise is subtracted, and τ_0 is the characteristic time of the process leading to the noise. For noise that is successfully

described by Eq. (5-3), one can infer the shape of the defect-energy distribution $D(E_o)$ over a wide range of energies from noise measurements as a function of temperature T via:

$$D(E_0) \propto \frac{\omega}{kT} S_V(\omega, T) \tag{5-4}$$

where the defect energy barrier is related to the temperature and frequency of the noise measurements through:

$$E_o \approx -kT \ln(\omega \tau_o). \tag{5-5}$$

5.2 Low Frequency Noise Measurement Setup

In this work, low frequency $1/f$ noise is measured for BP MOSFETs, before and after bias/radiation/annealing. The excess noise measurements were performed when the devices were biased in the linear regime. The gate terminal was connected directly to a HP 4140B for constant voltage supply, with the source terminal grounded. A resistor is connected in series between the drain terminal and HP 4140B for protecting and adjusting the drain bias. The drain voltage noise is amplified using a low-noise amplifier SR 560 and the power spectral density is calculated by a SR 760 spectrum analyzer, across a frequency span from 1 Hz to 390 Hz. Preamplifier noise and thermal noise contributes to most of the background noise, and all the low frequency noise data in this thesis are shown after background noise subtraction, if not otherwise pointed out.

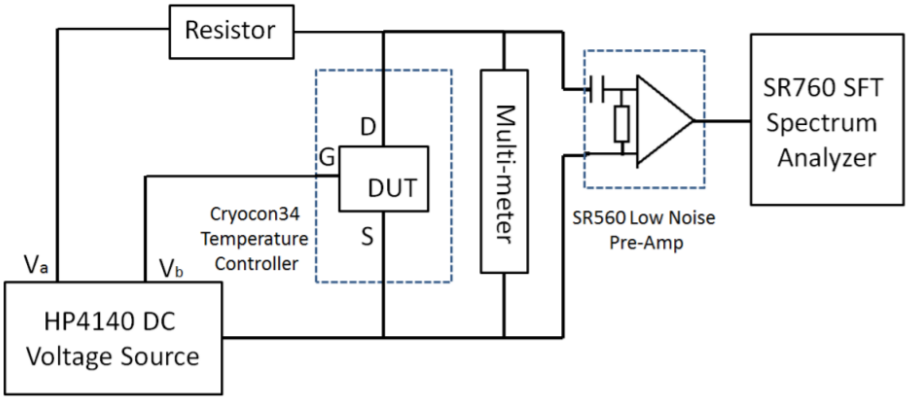


Fig. 5.3. Low frequency noise measurement setup.

5.3 Room Temperature 1/f noise Spectrum Analysis of BP MOSFETs

The gate oxide thickness of the devices under test is 20 nm. The experimental procedure is irradiation under +1V gate bias to 1 Mrad(SiO_2), followed by alternating ±1 V switched bias annealing cycles. Room temperature low frequency noise is measured before and after irradiation and before each alternating switched bias annealing cycle, which has been shown in Fig. 4.13.

Fig. 5.4 shows the excess drain-voltage noise power spectral density S_V (corrected for background noise) as a function of frequency before irradiation, after the devices are irradiated to 1.0 Mrad(SiO_2), and after the conclusion of the switched-bias annealing sequence depicted in Fig. 4.13. For these measurements, the gate voltage was adjusted to maintain a constant $V_G - V_{th}$ of -0.2 V. The noise of these devices increases with irradiation, and decreases at the end of the post-irradiation annealing sequence.

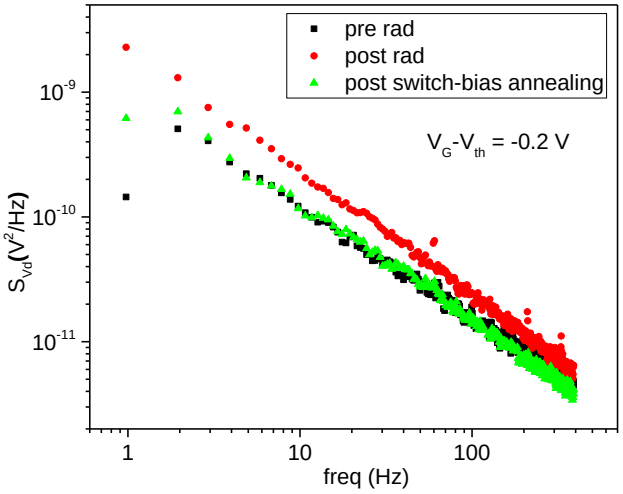


Fig. 5.4. S_{Vd} at room temperature as a function of frequency before irradiation, after irradiation, and after the after the conclusion of the switched-bias annealing sequence depicted in Fig. 4.13. For the noise measurements, V_{SD} = -100 mV, and $V_G - V_{th}$ = -0.2 V.

The noise magnitude was monitored as a function of gate voltage at the various stages of the irradiation and annealing sequence of Fig. 4.13. To assist in the parameterization of the noise, we use the empirical expression discussed in Section 5.1.1:

$$S_V(f, V_D, V_G) = \frac{K}{f^{\alpha}} \frac{V_D^2}{(V_G - V_{th})^{\beta}}. \tag{5-2}$$

Here K is the normalized noise magnitude of the device, α is the frequency dependence, and β is a measure of the gate-voltage dependence, where $S_V \propto (V_G - V_{th})^{-\beta}$ [83]–[85]. The frequency exponent α was determined by the best fit to S_V vs. f over the accessible frequency span. For these devices, α = 1.0 ± 0.1 before irradiation, and throughout the irradiation and annealing sequence.

Fig. 5.5 shows the value of S_V at 10 Hz as a function of alternating bias annealing

for two values of $V_G - V_{th}$ for the irradiation and annealing sequence of Fig. 4.13. The magnitude of the noise consistently increases during positive bias annealing, when the effective net positive oxide-trap charge in the HfO_2 gate dielectric is at a minimum, and decreases during negative-bias annealing, when the effective net positive oxide-trap charge in the HfO_2 gate dielectric is at a maximum. Quite interestingly, such a trend was also observed in previous studies of the low frequency noise of Si-based *p*MOS devices by Meisenheimer et al. [83] and by Ploor et al. in nMOS power transistors [86]. In each of these studies, the noise was attributed to the differences in effects of filled and empty border traps on the observed noise magnitude [83], [86]. Future study is needed to determine whether that is also the case for these BP transistors. Given that other aspects of radiation-induced charge trapping are similar between these devices and Si-based MOSFETs, and that the defects that cause low frequency noise in MOSFETs are quite similar to those responsible for radiation-induced-hole trapping [80],[87]–[89], it is certainly plausible for this to be the case.

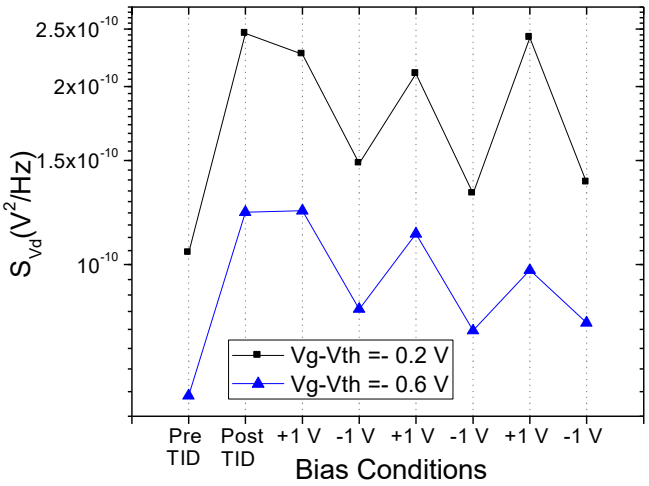


Fig. 5.5. S_V at 10 Hz at two values of $V_G - V_{th}$ for the switched-bias annealing sequence depicted in Fig. 4.13. For the noise measurements, V_{SD} = -100 mV.

Finally, we note that, prior to irradiation, the slope of the S_V versus V_G-V_{th} curve, $\beta = -1.5$; after irradiation, $\beta = -1.8$, and then $\beta = -2.0$ after the last +1 V annealing process in the series. Based on the usual number fluctuation model of the noise of semiconductor devices, this is evidence of a distribution of defect energies that increases from midgap toward the valence band edge before irradiation, and then becomes more uniform in energy after the device is irradiated and then annealed [83], [86]. These results illustrate the utility of low frequency noise measurements in characterizing the evolution of radiation-induced defects in BP transistors.

5.4 Temperature-dependent Low Frequency Noise

Fig. 5.6 shows the normalized low frequency noise magnitude at 10 Hz as a function of temperature for an unirradiated BP transistor with 6.8 nm gate oxide biased at ± 0.34 V in room ambient. The upper x-axis in Fig. 5.6 shows values of E_0 based on Eq. (5-4), from 0.2 eV to 0.7 eV. These energies are associated with defects in the HfO_2 [80]; hence, there is no particular

feature that can be associated with the ~ 0.38 eV BP band gap. For noise described by Eq.(5-3), the shape of the defect-energy distribution $D(E_o)$ from noise measurements versus temperature is inferred via Eq.(5-4). The defect energy is related to the temperature and frequency through Eq.(5-4). The noise of these BP transistors is consistent with carrier number fluctuations [80] in all cases considered in this work.

For the unstressed device, a peak in noise near 0.6 eV is observed, indicating the presence of a significant defect density in as-processed BP devices. After stressing the device for two hours with V_{GS} = +0.34 V and V_D = V_S =0 V, the noise around 0.6 eV decreases slightly. After switching the gate bias polarity and stressing the devices for two more hours, the noise above 0.6 eV decreases again slightly. Although bias-stress induces small changes in the noise distribution, no significant I_{DS}-V_{GS} shifts are observed, as shown in the inset of Fig. 5.6. This shows the relative stability of these devices before irradiation.

The red curve in

Fig. 5.7 shows the measured frequency exponent of the low frequency noise, $\alpha = -\partial \ln(S_V)/\partial \ln(f)$, for the unirradiated BP transistor of Fig. 5.6 in the temperature range 90 K to 300 K, where f is the frequency. When low frequency noise is caused by a random thermally activated process having a broad distribution of energies relative to kT, the frequency and temperature dependences of the noise are correlated via the Dutta-Horn model [80],[82] and Eq. (4-3). The characteristic time of the process $\tau_0 = 1.81\times10^{-15}$s is chosen here to be

consistent with previous MOS studies [80],[87]. The calculated frequency exponent is plot as the black curve in

Fig. 5.7.

The good agreement between the measured value of α and the value calculated via the Dutta-Horn model indicates that the noise of BP transistors is due to a random thermally activated process having a broad distribution of energies and confirms the validity of Eq.(5-4) for these devices.

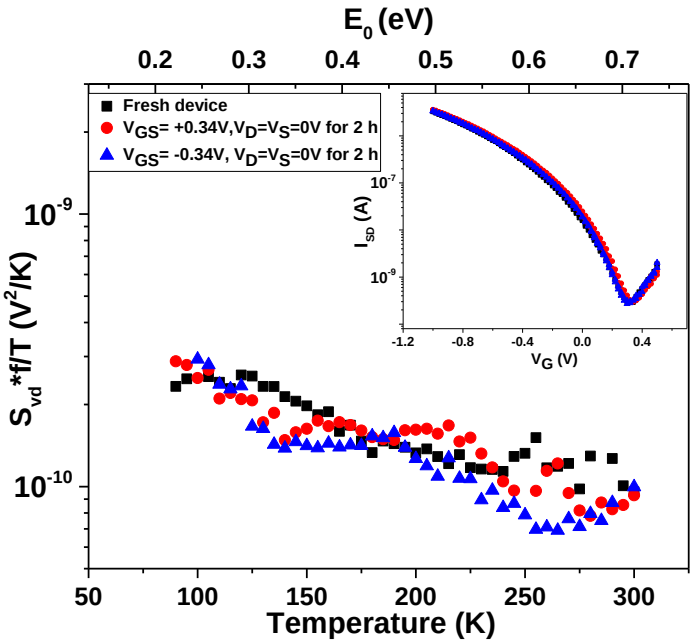


Fig. 5.6. Normalized low frequency noise from 90 K to 300 K at f = 10 Hz for an unirradiated BP transistor before and after bias stress at ± 0.34 V in room ambient. The temperature range corresponds to an activation energy scale ranging from 0.2 eV to 0.7 eV (top x-axis). The inset is the I_{SD}-V_{GS} curve before and after each bias measured at V_{SD} = 100 mV. The narrow band gap of the BP (~ 0.38 eV) limits our noise measurements in this work to room temperature and below.

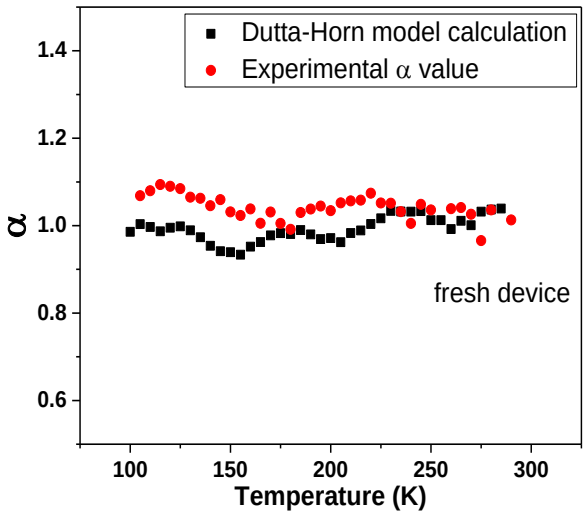


Fig. 5.7. Measured and predicted values of the frequency dependence of the noise, $\alpha = -\partial \ln(S_V)/\partial \ln(f)$, from 90 K to 300 K. The predicted values are based on the temperature dependence of the noise of the unirradiated and unstressed device in Fig. 5.6, using the Dutta-Horn model.

Fig. 5.8 shows a significant increase at energy levels when the device is irradiated with V_{GS} = +0.34 V, which is identified as the worst-case bias in Chapter 4. Significant increases in the post-irradiation noise, relative to pre-irradiation values, are observed at ~ 0.35 eV and ~ 0.65 eV, following 200 krad(SiO_2) irradiation. When the dose increases to 500 krad(SiO_2), the noise increases further, and new post-irradiation noise peaks are observed at ~ 0.2 eV and ~ 0.5 eV. These peaks correspond to local maxima in the defect-energy distribution. Before irradiation and at all doses, the 0.2 eV defects remain the dominant trapping centers in these devices. In previous studies on MOSFETs with HfO_2 dielectrics, the noise has been attributed primarily to O vacancies [80], a conclusion reinforced by the density functional calculations presented below, and a potentially new role for hydrogen in the noise process will be identified.

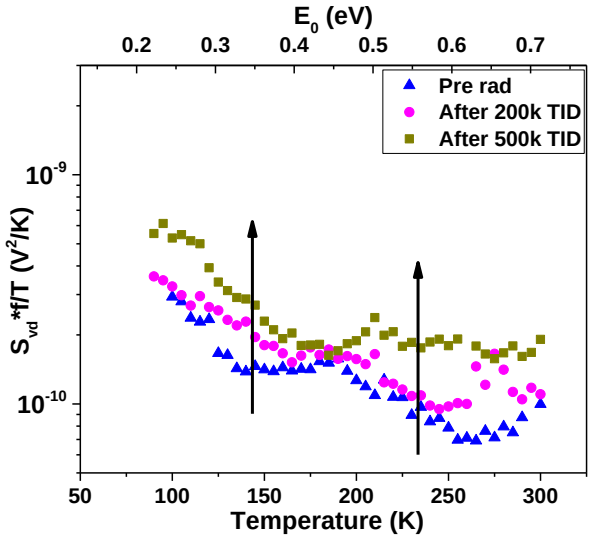


Fig. 5.8. Normalized low frequency noise from 90 K to 300 K at f = 10 Hz for the BP transistors as a function of the total dose. Devices were biased at V_{GS} = 0.34 V and $V_D = V_S$ = 0 V during irradiation.

The charge trapping characteristics of these devices are further investigated via post-irradiation switched-bias annealing, at room temperature in the vacuum cryostat of Fig. 5.3. These kinds of switched-bias annealing measurements are often helpful in understanding the roles of defects and impurities on MOS radiation response and low-frequency noise [32], [75], [87], [90]. Fig. 5.9 shows results for devices annealed with V_{GS} = ± 0.34 V for 2 h. After positive bias annealing, the *I-V* curve in Fig. 5.9 (a) shifts positively by ~ 50 mV, and the noise in Fig. 5.9 (b) increases significantly in the range 0.3 eV to 0.5 eV. After negative bias annealing, the *I-V* curve shifts negligibly, and the noise peak moves to a lower energy level of ~ 0.3 eV. The *I-V* shifts during switched-bias annealing in Fig. 5.9 (a) are much smaller than the ± 0.3-0.4 V shifts observed in the devices with thicker dielectrics during shorter anneals at comparable electric fields.

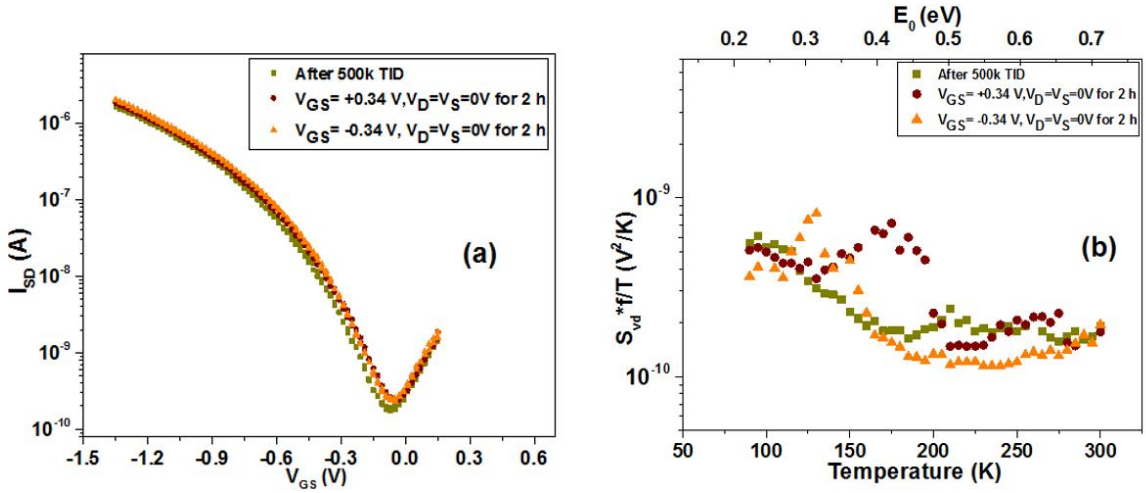


Fig. 5.9. (a) I_{SD}-V_{GS} characteristics of a BP transistor before and after switched-bias annealing. After positive bias annealing, there is a +50 mV I_{SD}-V_{GS} shift. After negative bias annealing, no I_{SD}-V_{GS} shift is observed. (b) Normalized low frequency noise from 90 K to 300 K at f = 10 Hz for the irradiated BP transistors for one switched-bias annealing cycle.

After the switched-bias annealing cycle of Fig. 5.9, the device was transferred to a vacuum chamber at a pressure of 1.2 Torr and allowed to sit under floating bias conditions for two weeks at room temperature. Fig. 5.10 shows (a) I_{SD}-V_{GS} curves and (b) changes in the low frequency noise after this vacuum storage. However, the low frequency noise shows a significant change after storage. Fig. 5.10(b) shows the noise in the range of 0.38 eV to 0.5 eV increases significantly, and the noise decreases slightly for the energy level below 0.38 eV.

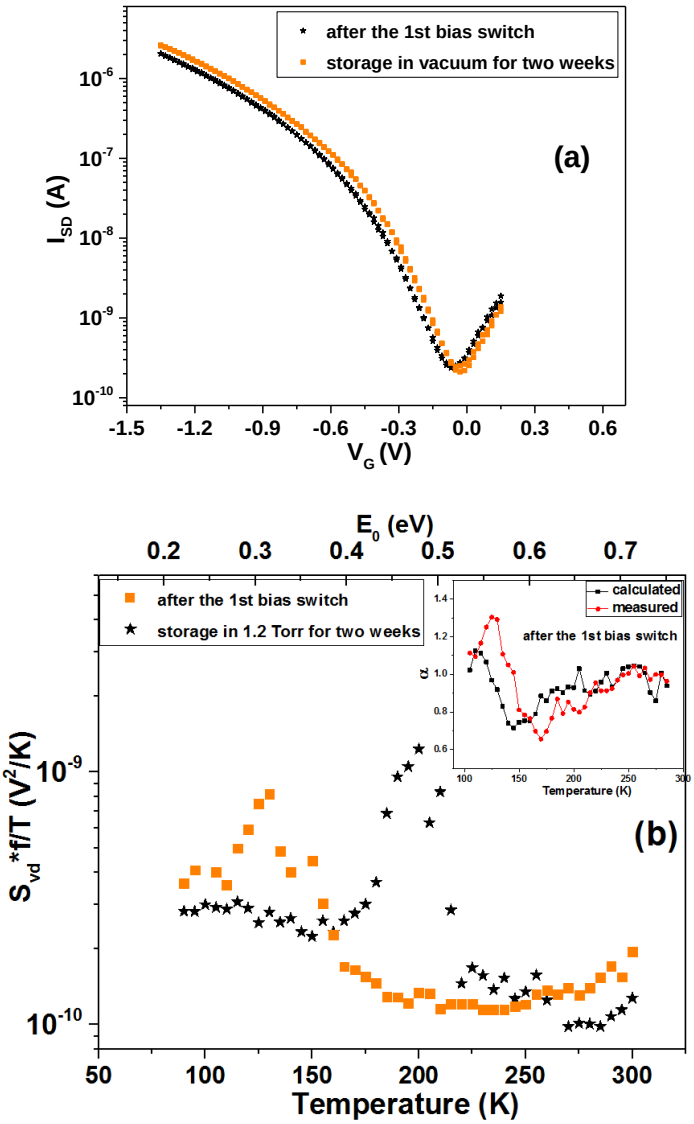


Fig. 5.10. I_{SD}-V_{GS} characteristics for the BP transistor of Fig. 5.9 before and after two weeks of storage in a vacuum chamber (dark environment with air pressure of 1.2 Torr) with floating bias. There is a positive 50 mV I_{SD}-V_{GS} shift after storage. (b) Normalized low frequency noise from 90 K to 300 K at f = 10 Hz before and after storage. The inset in (b) shows that the noise continues to follow the Dutta-Horn model, as consistently observed in this study.

A control experiment was conducted on an unirradiated BP MOSFET to see whether similar aging effects might produce quantitatively or qualitatively similar effects to those observed in Fig. 5.9 and Fig. 5.10 on unirradiated devices in the same storage environment. This test was performed because the performance of BP transistors can degrade with time in air, when

the moisture and oxygen react with BP [13], [28], [66]. A passivation layer reduces these effects, but degradation may still occur [28]. Fig. 5.11(a) shows that there is a -10 mV shift of the I_{SD}-V_{GS} curve for the unirradiated device after storage. This shift is smaller and oppositely directed to the shift in the irradiated device under storage in Fig. 5.10(a). Fig. 5.11(b) again shows a noise peak in the range of 0.35 eV to 0.5 eV for the unirradiated device during vacuum storage, but both the initial noise and the peak that appears after aging are approximately a factor of 10 less than the noise of the device that was first irradiated and then aged. Hence, the same factors appear to contribute to the noise peaks in both the irradiated and unirradiated devices, but effects are much larger after the device is irradiated.

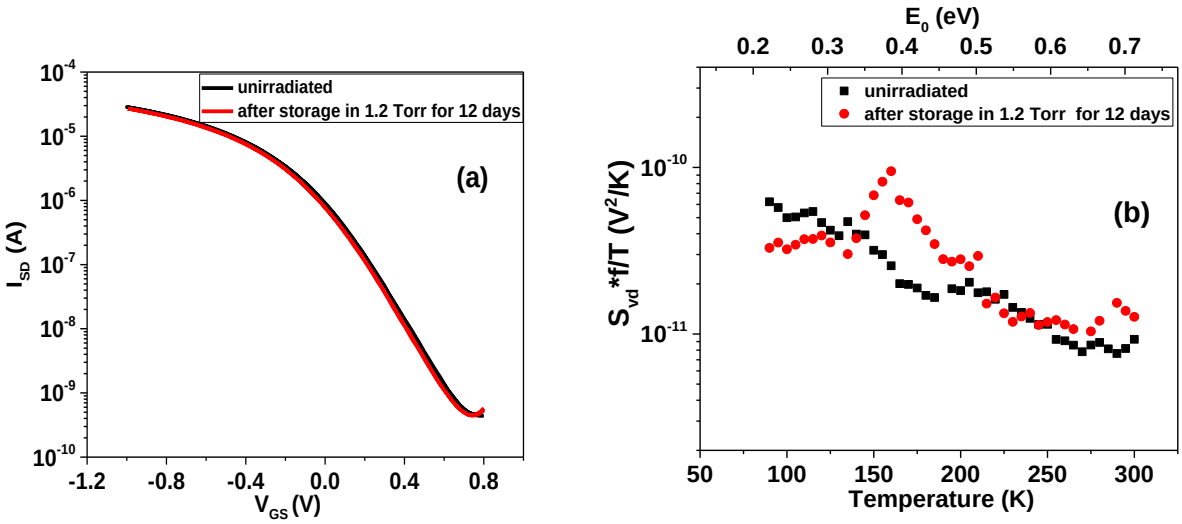


Fig. 5.11. (a) The I_{SD}-V_{GS} characteristics of an unirradiated BP transistor before and after 12 days of storage in a vacuum chamber (dark environment with air pressure of 1.2 Torr) with floating bias. There is a negative 10 mV I_{SD}-V_{GS} shift after storage. (b) Normalized low frequency noise from 90 K to 300 K at f = 10 Hz for the unirradiated BP transistors before and after storage.

Having confirmed that the results in Fig. 5.9 and Fig. 5.10 are due primarily to the evolution of radiation-induced defects and/or impurities (e.g., hydrogen), and not just a result of

environmental and/or aging effect, we performed a second series of switched-bias anneals and noise measurements, as shown in Fig. 5.12 to see whether the reversibility in response is repeatable, or diminishes with time, as often observed in Si MOS devices [75]. This second series of positive-bias annealing leads to a +30 mV shift in the *I-V* curves and increased growth and broadening of the 0.4-0.5 eV noise peak. The noise magnitude is now significantly increased over the peak observed during the first switched-bias annealing cycle in Fig. 5.9. Performing a second negative-bias anneal shifts the noise peak to lower energies, and further broadens the peak.

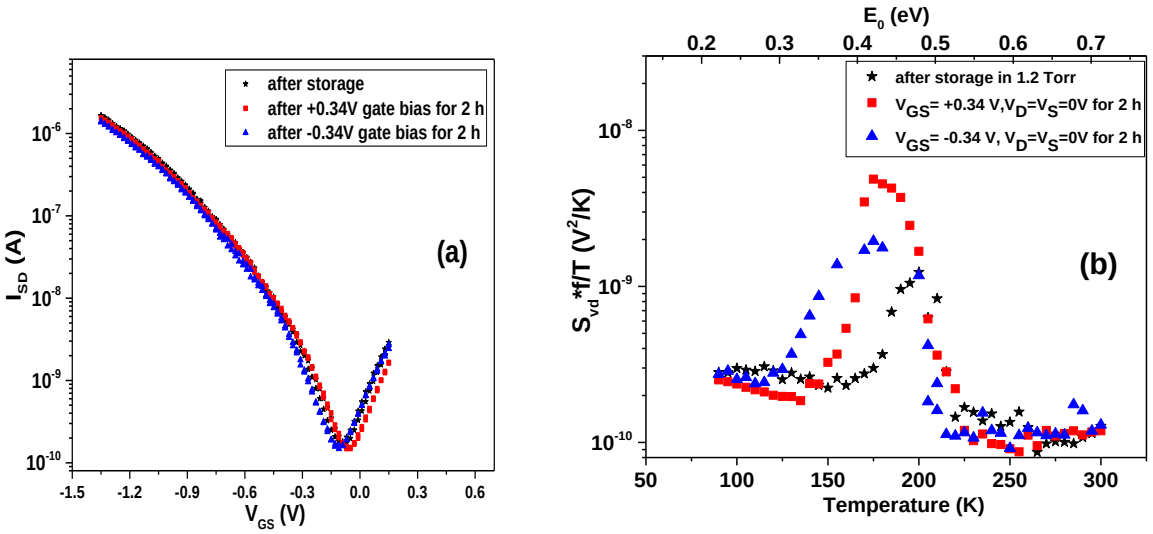


Fig. 5.12. (a) I_{SD}-V_{GS} characteristics of the irradiated and stored BP transistor of Fig. 5.9 and Fig. 5.10 before and after a second series of similar switched-bias anneals. After positive bias annealing, there is a +30 mV I_{SD}-V_{GS} shift. After negative bias annealing, there is a -50 mV I_{SD}-V_{GS} shift. (b) Normalized low frequency noise from 90 K to 300 K at f = 10 Hz for these irradiated and aged BP transistors through this second switched-bias annealing cycle.

Importantly, the most significant changes in noise that occur during post-irradiation annealing and/or storage in Fig. 5.9, Fig. 5.10 and Fig. 5.12 are simply unobservable in room temperature noise measurements. Through this full annealing and storage cycle, the noise at

room temperature changes by less than a factor of 2, consistent with observations in a previous study in Section 5.3, during a similar switched-bias annealing sequence. These results emphasize the utility of temperature-dependent noise measurements in understanding the effects of defects and/or impurities on the performance, reliability, and radiation response of MOS devices [80].

5.5 DFT Calculations for Defect Identification

Density functional theory calculations (DFT) provide an efficient and reliable methodology to gain insight into the atomistic nature of radiation-induced phenomena in microelectronic devices [91]. Therefore, density functional theory (DFT) calculations are performed on a model BP/HfO_2 system. In MOS devices with HfO_2 dielectric layers on Si and/or SiGe substrates, oxygen vacancies have been identified as important defects in studies of both the radiation response and low frequency noise [65], [69], [80]. Electron exchange with dipolar defects associated with O vacancies and the “shuttling” of protons between the near-interfacial oxide and interface have both been found to contribute to post-irradiation switched-bias annealing in HfO_2 oxides on Si [80], [92], [93]. The calculations in this work are on oxygen- and hydrogen-related defects and impurities that are expected to be relevant to BP/HfO_2 devices at all stages of device maturity.

DFT calculations were performed by Andrew O'Hara from Vanderbilt University using the VASP code [91], [94] with projector-augmented plane wave pseudopotentials [95], [96] and a 400 eV plane wave cutoff energy. For calculation of defect energy level alignments, the HSE06 range-separated hybrid functional is used for the exchange correlation potential [97] using

experimental lattice constants [98], [99], and utilized local electrostatic potential alignments to account for charged impurities in finite supercells [100]. A $3\times2\times1$ supercell of the primitive cell of BP and a $2\times2\times2$ of the primitive cell of HfO_2 were utilized with k-point point grids of $3\times3\times2$ and $2\times2\times2$, respectively. Using this parameterization, a band gap of 5.60 eV is calculated for HfO_2, in good agreement with experimental reports [101], as shown in Fig. 5.13(a). The band gap of BP is calculated as 0.38 eV (Fig. 5.13 (a)), slightly larger than the reported values for truly bulk BP, but similar to that expected for few nanometer thick BP [102] as in the current devices. For calculations of interfacial hydrogen shuttling related to switched-bias annealing (Fig. 5.13 (b))[90], the Perdew, Burke, and Ernzerhof parameterization of the generalized gradient approximation was employed to calculate the exchange-correlation potential [103] with Van der Waals interaction correction [104] due to the lower computational cost for structural properties.

Using the $\varepsilon_H(+/-)$ energy level crossing point for interstitial hydrogen as an estimate for the charge neutrality level in each material, the band alignment between BP and HfO_2 was calculated, as shown in Fig. 5.13 (a). This alignment results in a valence band offset of 3.68 eV and a conduction band offset of 1.53 eV. Using the $\varepsilon_H(+/-)$ level for BP to set the valence band position relative to the vacuum energy level [105] gives a value of 4.80 eV for the ionization energy, in agreement with the value calculated using surface slab models of BP [106]. For p-type BP, hydrogen in either the HfO_2 or BP regions will act as a donor. The +/0 transition energy level relative to the BP valence band is 0.23 eV for hydrogen in BP; while for hydrogen in HfO_2, the

level is 1.61 eV above the BP valence band.

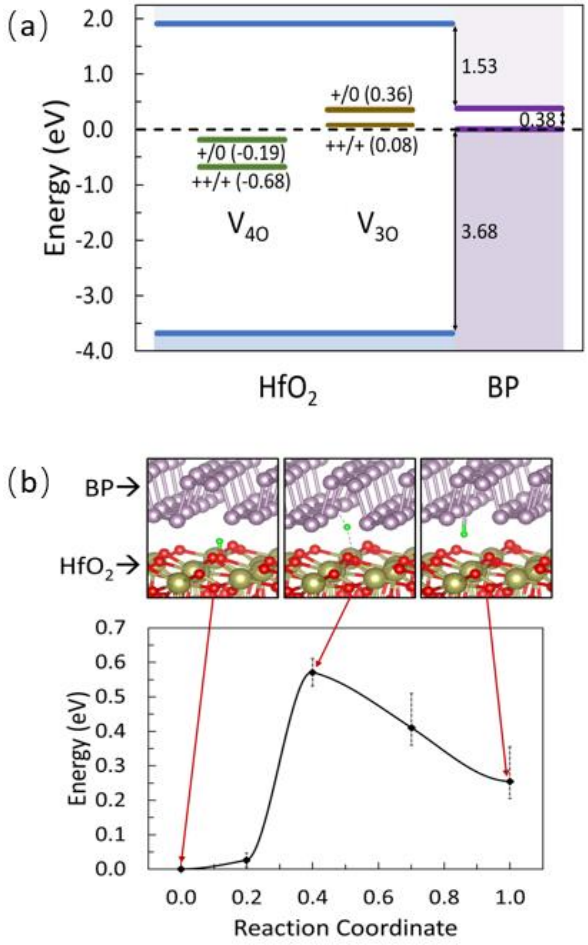


Fig. 5.13. (a) Energy band alignment of HfO_2 and BP showing the calculated defect levels for 4-fold and 3-fold based oxygen vacancies, the most likely to contribute to the low-frequency noise. The dashed line is set equal to the BP valence band maximum to guide the eye. All numbers are in eV. (b) Atomic structure and energy barrier calculation for H^+ migration at the inter-face between HfO2 and BP, illustrating bonding to the HfO_2 surface, detach-ment from both surfaces, and bonding to the BP surface.

5.6 Discussion

To investigate whether O vacancies in HfO_2 play a significant role in determining the radiation response and low-frequency noise of these BP/HfO_2-based devices, transition levels for the fully depassivated 3-fold and 4-fold coordinated oxygen vacancies in HfO_2 are calculated

using DFT. Each of these types of defects requires two hydrogen atoms for full passivation. During X-ray irradiation, mobile hydrogen can depassivate either one or both of these hydrogen atoms by forming H_2 molecules, leading to the trapping of either one or two holes at the defect site, similar to what is observed in SiO_2 [107]. To investigate whether O vacancies in HfO_2 play a similar role in the current devices and, in particular, whether they contribute to the low frequency noise measurements of the irradiated devices in Fig. 5.8, transition levels for the fully depassivated 3-fold and 4-fold coordinated oxygen vacancies in HfO_2 are calculated. The ++/+ and +/0 transition energy levels and their values are shown in Fig. 5.13(a), relative to the BP valence band, for both types of fully depassivated O vacancies. Each is found to have levels that are easily accessible to the BP during noise measurements, making them strong candidates for the defects responsible for at least a portion of the radiation-induced increase in low frequency noise in these devices. In amorphous HfO_2, which is the case for these devices there will not be single-value energy levels; instead, each level will be broadly distributed in energy around its peak [70], making these devices ideal candidates for the multiply-peaked, broad increase in the noise spectrum that is observed when the devices are irradiated (Fig. 5.8). Half-passivated vacancies, while still contributing to overall hole trapping, have transition energies of 1.41 eV (3-fold coordinated) and 1.16 eV (4-fold coordinated) above the valence band of BP, and thus are not expected to contribute to the low frequency noise spectra in the region measured. Moreover, electron-trap levels are also found in HfO_2 [108], [109]. These defects also will contribute to the noise before and after irradiation, and are also likely to partially offset radiation-induced hole

trapping in these devices [70], [76].

Since BP is known to oxidize relatively easily under ambient conditions [110], [111], oxide-related defects in BP such as interstitial adsorption and substitution (O_P defects) must also be considered. However, prior work has shown that the adsorption of oxygen on the BP surface leads to an electrically inactive site [112]. We also affirmed the result of [113] that O_P substitution modifies the valence band of BP and introduces a shallow hole trap above the valence band. However, the +/0 transition level of this state is 0.04 eV above the BP valence band, and is therefore too low in energy to substantially impact either the noise or the threshold voltage of the devices over the measured temperature range. On the other hand, oxidation of BP through gettering of oxygen from the HfO_2 layers provides a plausible explanation for the enhancement in 1/*f* noise in Fig. 5.11 after device storage. Not only can BP be easily oxidized, as mentioned above, but the presence of vacancies in BP (a contributor to its *p*-type behavior) increases the oxidation rate [114]. Furthermore, HfO_2 has been exploited for its ability to generate oxygen vacancies when in contact with easily oxidized materials for RRAM applications [115]–[117]. Similar 1/*f* noise enhancements have previously been observed in Si/SiO_2 devices due to diffusion of oxygen from SiO_2 into Si [38], [118], [119]. Hence, interactions of BP with near-interfacial layers of HfO_2 is a likely source of a significant fraction of the O vacancies responsible for the majority of the low-frequency noise and radiation-induced hole trapping in these devices.

Switched-bias-induced reversibility in threshold voltages and low-frequency noise

magnitudes in Si MOS devices are often associated with the motion of electrons into and out of defect sites associated with trapped holes [32], [75], [87]. In contrast, only small changes in the effective threshold voltages are observed for the devices of Fig. 5.9, Fig. 5.10 and Fig. 5.12 during switched-bias post-irradiation annealing for these BP/HfO_2-based devices, but large time and voltage-dependent peaks in the low frequency noise spectrum. These noise peaks are observed at 0.4 to 0.5 eV and increase in magnitude during positive-bias annealing, and decrease in magnitude and shift slightly lower in energy with negative-bias annealing. However, only small changes in the *I-V* measurements are observed. Moreover, peaks similar to those in Fig. 5.9, Fig. 5.10 and Fig. 5.12 are *not* observed in irradiated Si MOS devices under similar switched-bias annealing conditions [32], [75], [87]. Thus, while a small portion of the switched-bias, post-irradiation annealing response in these BP/HfO_2-based devices may be associated with electron motion into and out of the oxide in response to the applied bias, another mechanism is most likely responsible for the large noise peaks at 0.3 to 0.5 eV in Fig. 5.9, Fig. 5.10 and Fig. 5.12.

We now consider whether hydrogen motion may account for the noise peaks that appear during switched-bias, post-irradiation annealing. Hydrogen for *p*-type BP devices is a donor and will serve as a hole trap. Furthermore, H^+ has been shown in general to be field mobile. Thus, we considered the role of hydrogen motion across the van der Waals gap between HfO_2 and BP in Fig. 5.13 (b) as a possible origin for the noise peaks in Fig. 5.9, Fig. 5.10 and Fig. 5.12. As motivation, we note that a similar mechanism has been observed previously in Si-based devices passivated with HfO_2, in which a proton “shuttles” between sides of the dielectric/semiconductor

interface [90], but the energetics of this process has not been investigated in the context of either BP devices or noise spectra. Using the nudged elastic band method [120], [121], the DFT calculations depicted in Fig. 5.13(b) show that, in equilibrium, H^+ preferentially binds to the HfO_2 surface, as opposed to the BP surface, with an energy level difference of 0.26 eV. The barrier for H^+ migration from the HfO_2 side of the interface to the BP side is found to be ~ 0.57 eV, while the reverse barrier is only ~ 0.22 eV. Due to the lattice mismatch between HfO_2 and BP, the calculations include some unavoidable strain. Different ways of handling this strain lead to variations in the calculated values in Fig. 5.13(b) of 0.1 eV to 0.2 eV, which are shown as error bars. The calculated relative stability implies a small preference for hydrogen to be on the HfO_2 side of the interface in ther-modynamic equilibrium. The relatively low barriers imply that hydrogen shuttling across the interface at room tempera-ture is energetically possible no matter which interface the hydrogen is initially located, and likely to be highly bias sensitive, consistent with the observed hysteresis in these structures, before and after irradiation.

The above discussion of the energetics of H^+ binding and motion enables the following understanding of the noise peaks in Fig. 5.9, Fig. 5.10, Fig. 5.11 and Fig. 5.12. When a device is irradiated, hydrogen is released and transports to the near-interfacial region as a proton under positive (worst-case) bias [64], [92]. When bias is removed, a fraction of the H^+ is thermally released and migrates to the HfO_2 interface. The application of positive bias causes the H^+ to return to the BP side of the interface, and negative bias causes H^+ to return to the HfO_2 side of the interface, as long as the temperature is high enough for the H^+ to surmount the relevant

energy barrier. When the H^+ is bound to either the BP or the HfO_2, it contributes to the *I-V* shifts, but not significantly to the noise. When the H^+ is moving, it can contribute strongly to noise [122], leading to the observed peaks.

Fig. 5.13 (b) shows that motion of H^+ under negative bias occurs with a lower barrier than motion under positive bias, consistent with the reduced energy at which the associated noise peak occurs in Fig. 5.9(b) and Fig. 5.10(b) for post-irradiation annealing or aging under negative bias (~ 0.3 eV) than for post-irradiation annealing or aging under positive bias (~ 0.4 eV to ~ 0.5 eV). Hence, the DFT calculations of Fig. 5.13(b) support the idea that the noise peaks observed in BP/HfO_2-based devices during switched-bias, post-irradiation annealing or aging under bias are associated with the reversible motion of H^+ in response to the applied bias. Fig. 5.9 and Fig. 5.10 also show that more mobile protons are present after irradiation than after aging under bias. The density of the H^+ that leads to the observed noise after irradiation and annealing is naturally a function of as-processed defect density and hydrogen concentration, so we expect that the magnitude of the observed peaks should decrease as device processing becomes more mature. However, because HfO_2 is a standard dielectric material in advanced Si-based MOSFETs, it is reasonable that HfO_2 may also be utilized in mature, commercial BP devices. Moreover, bonding configurations at the BP/HfO_2 interface are unlikely to change fundamentally, so significant effects associated with oxygen vacancies and hydrogen transport and reactions within BP/HfO_2 devices are also expected in future devices. Thus, in the same way that early radiation and ozone exposure studies of carbon nanotubes and graphene [23], [119], [123]–[125] provided initial

perspectives on the influence of defects on device performance, reliability, and radiation response that proved to be useful in guiding future technology development in those areas [126], we expect the results of this study to be similarly helpful in the development of future BP-based devices and integrated-circuit technologies.

5.7 Conclusions

We have measured the gate bias dependence and temperature dependence of the low-frequency $1/f$ noise of BP MOSFETs with HfO_2 gate dielectrics. Large increases in noise magnitude are observed after X-ray irradiation test. Reversibility of magnitude of the noise is observed during switched-bias annealing after irradiation. The voltage dependence of the low-frequency noise suggests that the trap distribution of the defects contributing to the noise becomes more uniform in energy after the devices are irradiated and annealed. Temperature dependent low-frequency noise measurements, coupled with DFT calculations, suggest that reducing the density of O vacancies in the HfO_2 gate dielectric layer and the amount of hydrogen in the structure should improve the performance and radiation response of BP/HfO_2-based devices.

Chapter 6 . Laser-induced Single Event Transients in BP MOSFETs

BP MOSFETs are of significant interest for future CMOS logic applications. To date, there have been no reports on the SEE responses of BP MOSFETs. For logic devices working in space environments, SETs are important reliability concerns as they may lead to SEUs and soft errors at the system level. The SEEs discussed in this dissertation are SETs.

This chapter reports results obtained using a pulsed laser to study the SET responses of the BP MOSFETs. The pulsed laser technique has been widely used for SET testing [127]–[129]. High peak power femtosecond laser pulses at above-bandgap optical wavelengths have been used as single-photon excitation to investigate the single event transient response of various devices. Although the charge generation mechanisms and charge profile induced by laser irradiation are different from heavy ion irradiation, laser testing provides a complementary nondestructive, convenient, and low-cost method to identify mechanisms responsible for SETs. To study the charge collection mechanisms, the bias-dependence, position dependence, and laser energy dependence of the measured SETs in BP transistors were examined.

6.1 Experimental Detail of Laser-induced SETs in BP MOSFETs

The device used here has the same geometry as those described in Chapter 3.1. It has a source/drain spacing of 0.5 μm and device width is about 8.6 μm. The top view of the device is shown in Fig. 6.1(a). The center of the channel has an offset of ~1.5 μm to the center of the gate metal finger. The cross section of the device is shown in Fig. 3.1. For transient capture, all the devices are mounted in custom-milled metal packages with microstrip transmission lines and

Precision 2.92 mm K connectors. The packed device is shown in Fig. 6.1(b).

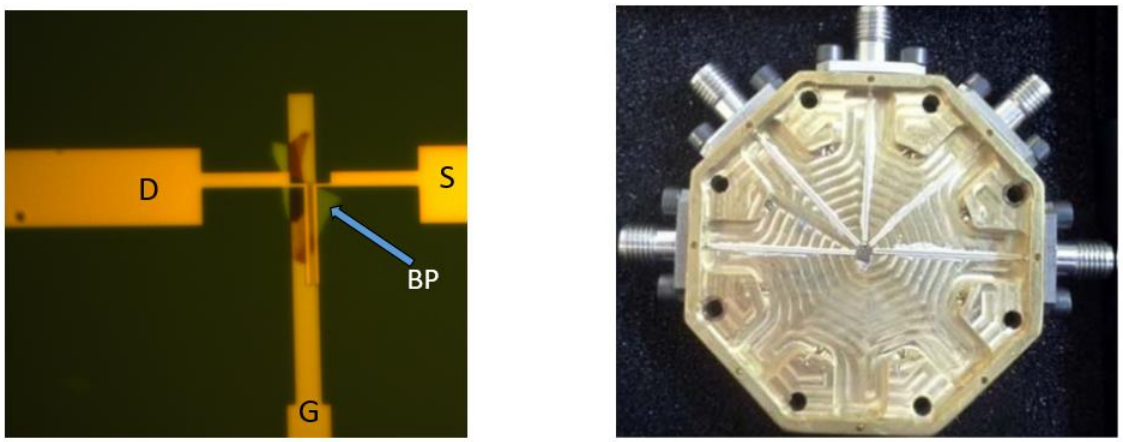


Fig. 6.1. (a) Top view of the BP MOSFETs for laser test (b) High-speed package for SET capture.

The transients were captured using a Teledyne Lecroy LabMaster 10-36Zi-A oscilloscope with 38 GHz front-end bandwidth. Each oscilloscope channel has 50 Ω input impedance, which is used to convert the transient current to a measurable voltage. During these tests, the source was grounded and the DC drain and gate bias were supplied by a HP 4156B through Picosecond Model 5542 bias tees with 50 GHz bandwidth. For all transients, the DC current is filtered out and only AC current transients are shown.

Laser irradiations were performed at Vanderbilt University. The experimental setup is shown in Fig. 6.2(a). The detailed experimental setup is described in [127]. The laser wavelength is 1.26 μm and the nominal pulse width is approximately 150 fs. The device-under-test (DUT) was fixed on an automated precision linear stage with a resolution of 0.1 μm. The stage jitter is about 0.2 μm. The optical pulses were focused onto the DUT using a 100× (NA 0.5) microscope objective. The spot diameter of the laser beam is 1.6 μm. The photon energy of the laser is 0.98

eV, which is greater than the bandgap of the channel BP materials (0.3 eV) but smaller than the surrounding oxide. There is no metal layer from the top of the device to the channel region, and the laser pulses strike the top of the device. As a result, single-photon excitation occurs and free carriers are generated in the BP channel materials. After each laser irradiation scan, the DC $I_D - V_G$ sweep is conducted to ensure no significant changes occur due to heating or degradations.

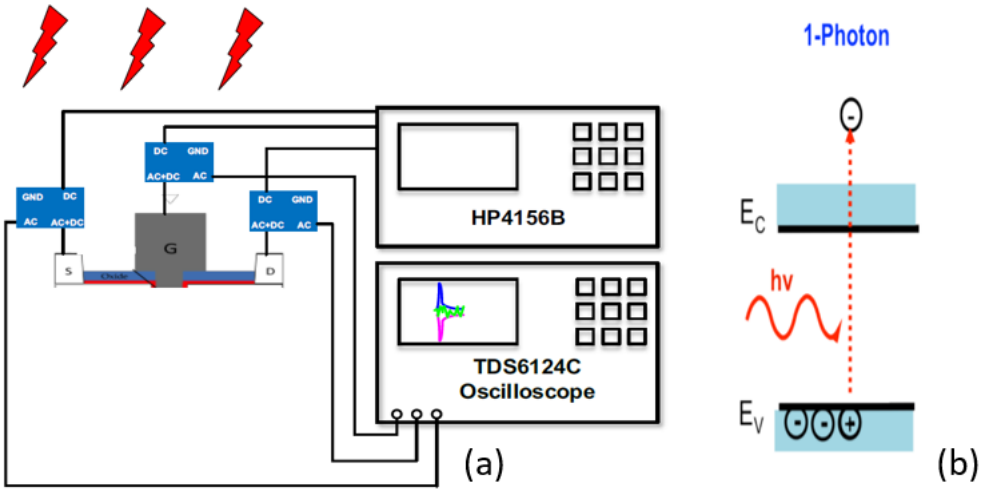


Fig. 6.2. (a) Schematic diagram of the laser setup; (b) Energy band diagram illustrating the single photon absorption. hv is the energy of the incident photon.

6.2 Experimental results and analysis

6.2.1 Signature of The Laser-induced SET Pulses in BP MOSFETs

Fig. 6.3 illustrates the recorded current transients at the source, drain and gate terminals when the laser (2.23 nJ) spot center is in the middle of the source and the drain electrodes. V_G is biased at V_{th}= -0.18 V, the source is grounded, and the drain is biased at a DC voltage of -1 V.

The measured source and drain transients have nearly the same magnitude but opposite polarity, which suggests that the transient current comes from the channel conduction. This is different from the traditional junction collection in Si devices [47]. The gate transients, if any, are indistinguishable from the background noise. The gate oxide effectively suppresses the gate transients because the barrier between semiconductor and HfO_2 for both types of carriers in these devices is large enough. The peak of the SET is 80 μA with full width at half maximum (FWHM) around 100 ps. The collected charge is about 4 fC. The rise time of the measured pulse is about 35 ps and the fall time is about 75 ps. There is no obvious long term charge collection. This suggests that diffusion-related charge collection is suppressed in these BP MOSFETs, which is likely due to the lack of a bulk region for carrier generation and collection in this device structure. In addition, the thickness of the channel BP materials is no more than 10 nm. Thus, collection volumes are much smaller than those of the planar bulk Si transistors. The small charge-collection region contributes to the relatively small magnitude of the SET peaks.

The laser-induced SETs of the BP MOSFETs are relatively fast transients with small peak current, and it is important to consider the limitations of the measurement setup discussed in section 6.1. First, the trigger level of the oscilloscope is preset to just above the background noise (1.75 mV in this case, which is equivalent to current magnitude of 35 μA) during the test for differentiation. Second, because all the terminals of the device are connected to analogous passive elements in the actual experiments, the capability to capture fast SETs is limited not only by the bandwidth of the oscilloscope, but also the external circuit and parasitic elements present

including bond pads, bond wires, coaxial cables, bias tees, and oscilloscope input impedance [130]. It's reported the narrow current spikes occurring within the first 20 ps of SETs are typically filtered out by parasitics [130], [131] in a similar measurement setup.

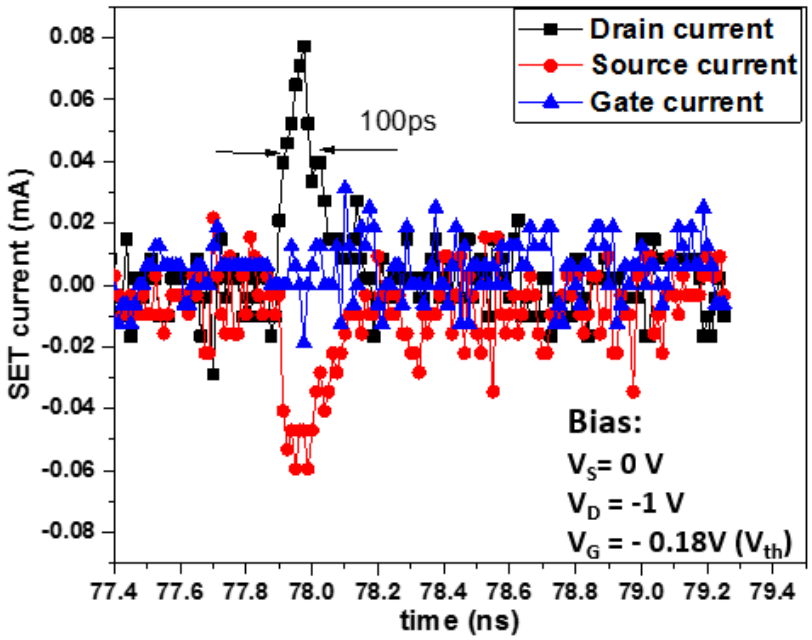


Fig. 6.3. Representative current transients recorded at the three terminals of the device when the laser spot center is at the center of the transistor. The laser wavelength is 1260 nm. The laser energy is 2.23 nJ.

6.2.2 Bias-dependence of The Laser-induced SET pulses

The bias dependence of the measured peak drain current was also investigated. First, V_D was fixed at −1 V, while V_G was varied. The laser pulses are at the center of the device. The error bars in Fig. 6.4 reflect the standard deviations among the 50 transients recorded.

Fig. 6.4 (a) shows the measured peak source current versus gate bias. The SET magnitude shows negligible dependence on the overdrive voltage**.** Next, V_G was fixed at –0.18 V and V_D was varied. The other conditions are the same as those in the gate bias dependence study. The data shown in Fig. 6.4 (b) imply that the SET magnitude increases slightly when V_D changes

from -0.6 V to -1 V. This is because the larger drain bias will induce a larger horizontal electric field. For the free carriers generated in the channel, larger horizontal electric field results in larger peak current between the source and drain.

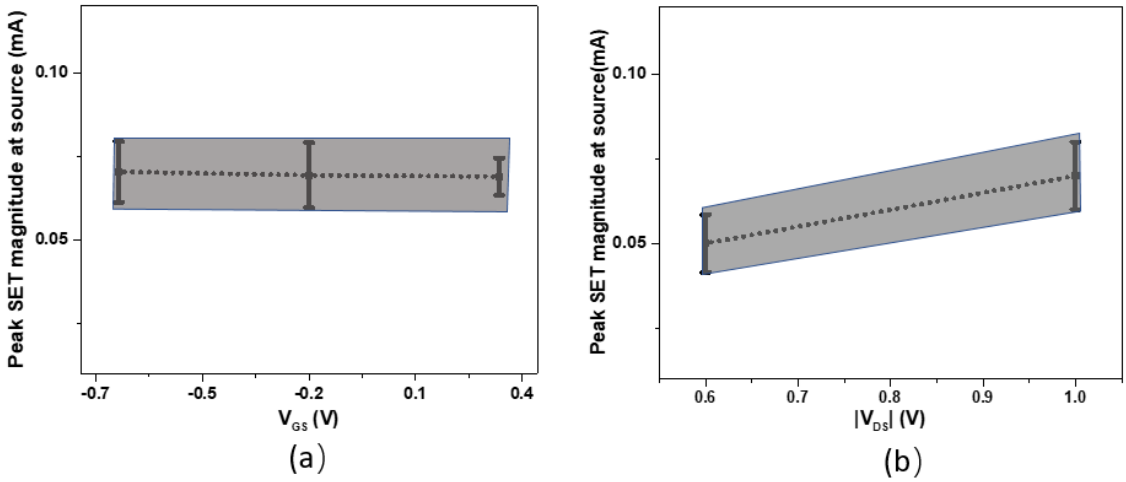


Fig. 6.4. Peak SET current magnitude at source for different (a) V_G and (b) $|V_D|$. The laser wavelength is 1260 nm and the center of the laser is at the center of the device. The laser energy is 2.23 nJ. The error bars are the standard deviations among the 50 transients recorded for each bias condition.

6.2.3 Position Dependence of The Laser-induced SET pulses

Line scans were performed to study the position dependence of the induced transients. A line scan of the laser spot from drain to source, parallel to the channel, was performed at the same bias conditions at V_G = –0.18 V and V_D = –1.0 V. The laser energy is 2.23 nJ. The center of the laser spot moves from x = –12 μm to x = +12 μm in the direction of drain to source. The center of the gate metal finger is set to x = 0. For each location at each bias condition, 50 SETs are captured and recorded to calculate the statistics of the transients. The measured SET peak current at the source is shown in Fig. 6.5 as a function of horizontal position. The maximum measured SET peak current and the longest SET current pulse are observed approximately at the

center of the channel. The sensitive region is ~ 2 μm in size. The laser spot size is ~ 1 μm in diameter and the channel length is 0.5 μm, which suggests carriers are generated and observed as SETs only when the laser pulse is incident on the channel.

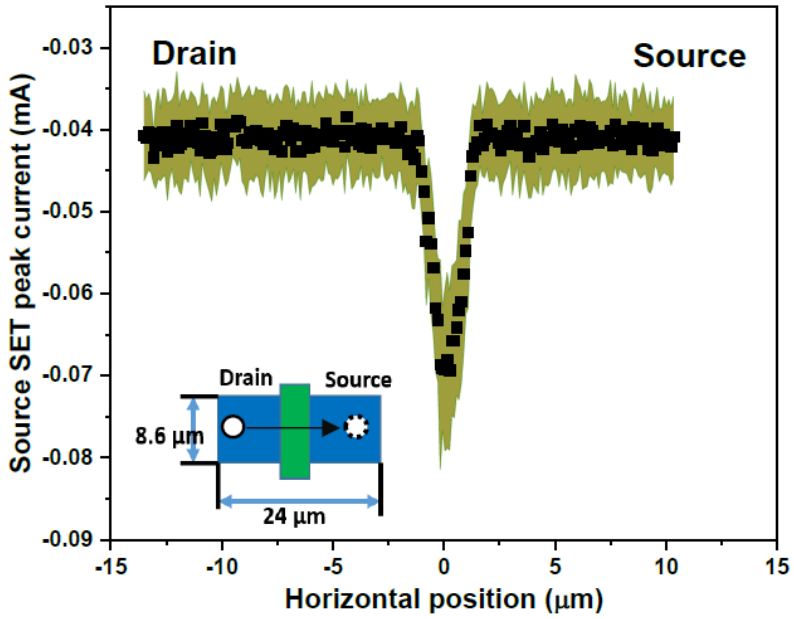


Fig. 6.5. Peak SET current at source along a line scan. The laser wavelength is 1260 nm. The shadow and error bars represent the standard deviation among the 50 transients recorded at each position. The bias conditions are V_G = –0.18 V and V_D = –1.0 V. The arrow indicates the movement direction of the laser spot during the line scan.

6.2.4 Laser Energy Dependence of measured SET pulses

Fig. 6.6 show the measured SET magnitude and FWHM dependence on the laser energy. When the laser energy increases, more free carriers are generated at the same bias condition, which results in a larger SET current. The result also shows the slight increase of the laser energy induces an increase of the measured FWHMs.

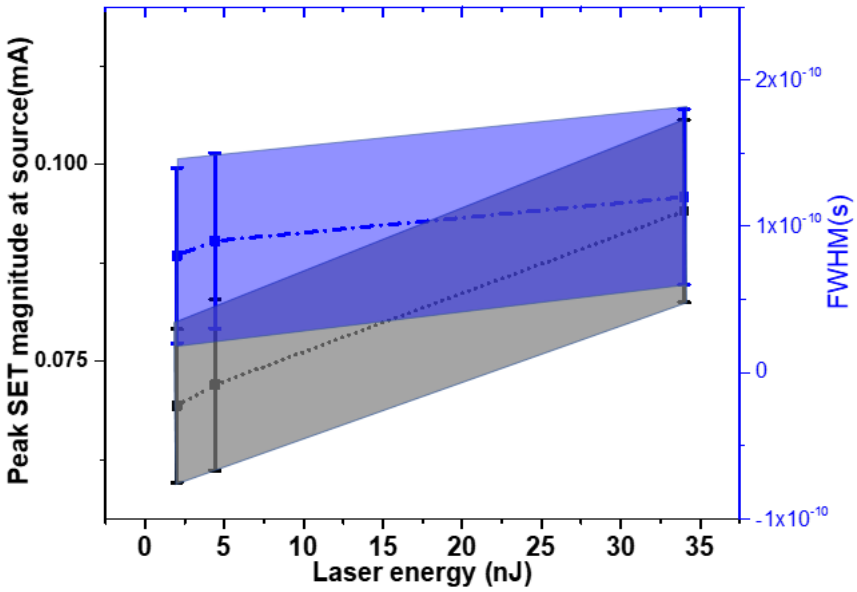


Fig. 6.6. Measured peak SET magnitude and FWHM as a function of laser energy. The laser wavelength is 1260 nm and the center of the laser is at the center of the device. The laser energy is 2.23 nJ. V_G = -0.18 V, V_D = -1 V and V_S =0 V. The error bar is the standard deviation among the 50 transients recorded at laser energy condition.

6.3 Discussion

Laser-induced SETs in HfO_2-passivated BP transistors are measured using pulsed-laser irradiation. At the center of the gate, the peak drain SET current is maximum. This laser-shunt mechanism is similar to the ion-shunt mechanism observed in Si devices [132], [133]. When an ion track size is comparable to the device gate length, the high density of electron-hole pairs will transiently short the source and drain [132], contributing to a large prompt current. In our laser system, the laser spot size is approximately 1.2 μm, which is larger than the effective gate length of 0.5 μm. Therefore, the peak drain current is maximum around the center of the channel region. Also, the result is consistent with the negligible dependence of the SETs on the overdrive voltage. When a large number of electron-hole pairs is generated by the laser over the entire channel

length, the varying gate bias changes the electric field in the gate oxide, but has limited impact on the number of carrier in the channel. For the laser-shunt effect, the drain-to-source current depends primarily on the applied drain-to-source bias [134]. The peak drain-to-source current appears to increase slightly when $|V_{DS}|$ increases from 0.6 V to 1 V. Such an increase would be consistent with the increase in channel electric field with increasing drain bias. SETs are relatively small when compared with conventional planar MOSFETs with similar geometries [135], due to the relatively thin channel material. With the development of BP technology, it is expected the collected charge will decrease when the thickness of the channel material scales down (becoming closer to a true 2D layer), but the dependence of position and bias will likely be consistent with the results discussed above.

Chapter 7 . Conclusions

This work focuses on the characterization of TID effects, low frequency 1/*f* noise, and SETs in passivated BP MOSFETs with HfO_2 gate dielectrics. Excellent stability of these structures is observed under bias stress before irradiation in ambient environments. Negative threshold voltage shifts and mobility degradation are overserved in TID experiment because of the buildup of net positive oxide-trap charges, with shifts similar to those expected for Si MOS transistors with similar dielectric/passivation layer. Reversibility of the DC parameters during switched-bias annealing after irradiation is similar to that observed in MOS transistors with SiO_2 gate dielectrics, and is associated with trapping of compensating electrons during positive-bias annealing, and detrapping of electrons during negative-bias annealing. Scaling the thickness of the HfO_2 dielectric layer in BP MOSFETs decreases the net positive oxide-trap charge build up.

Low frequency 1/*f* noise of BP MOSFETs increases with irradiation because of these irradiations-induced traps. During the switch-bias annealing after irradiation, the magnitude of the noise at room temperature consistently increases during positive bias annealing and decreases during negative-bias annealing, due to the effects of filled and empty border traps in the HfO_2 dielectric layer. Temperature-dependent low frequency noise measurements provide new insights into the nature of the defects that dominate the degradation in BP MOSFETs. During irradiation, O vacancies in the HfO_2 are the main sources responsible for the overall hole trapping. Density function theory calculations suggests fully-passivated O vacancies are the main contributors to the broad increase in the noise spectrum during irradiation. In addition, Hydrogen movement

also contributes to the noise spectra shifts. When a device is irradiated, hydrogen is released and transports to the near-interfacial region as a proton under positive gate bias. When bias is removed, a fraction of the H^+ is thermally released and migrates to the HfO_2 interface. The application of positive bias in post-irradiation annealing causes the H^+ to return to the BP side of the interface, and negative bias in post-irradiation annealing causes H^+ to return to the HfO_2 side of the interface. When the H^+ is moving, it can contribute strongly to noise, leading to the observed noise peaks in the post-annealing processes for irradiated BP MOSFETs.

Laser-induced SETs are observed in BP MOSFETs. The magnitude of the measured SET pulses are small because the thin thickness of the channel region. Peak SET transients are observed when the laser is at the center of the gate. Increasing the drain bias will induce an increase of the SET peak current. The magnitude dependence of the SETs on the drain bias dominates over the overdrive voltage, which can be explained by shunt effect.

In summary, we have used radiation and switch bias annealing to understand the TID-induced degradations in passivated BP MOSFETs with HfO_2 as gate oxide. The low frequency $1/f$ noise and density functional theory calculations helped to identify the defects that limit the performance of the devices. Also, we used the pulsed laser to study the laser-induced SETs in BP MOSFETs. The dependence of the laser-induced SETs on bias, position and laser energy are investigated.

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